A Low Power 8-Bit Current-Steering DAC Using CMOS Technology

P.Ramakrishna, M. Nagarani, K. Hari Kishore

Abstract: Design of 8-bit current-steering DAC is proposed in this paper. The800 MHz conversion rate has been obtained by a fully custom designed new architecture. With the operating voltage of 1V and 180nm CMOS technology this DAC is designed. The power dissipation is of 42.92uw which is very low. The DAC will thus create a "stair stepping" analog output until digital input is met or the voltage supply is reached. The measured integral non linearity (INL) is less than ±0.31LSB and the static differential non-linearity error (DNL) is ±0.418 LSB.

Keywords: DAC, current steering, Current mirror, cascade.

I. INTRODUCTION

The digital to analog converter is a system to convert digital signal to analog signal. It is widely used in digital signal processors. DAC'S are often used to convert finite-precision time series to a varying physical data. These are mainly used in different applications like audio amplifier, video amplifier, display electronics, data acquisition systems, data distribution systems. Current steering DAC's are the more commonly used architectures because of their small size and simplicity, high resolution and high speed. The architecture diagram of current steering DAC(CS-DAC) is shown in figure1.

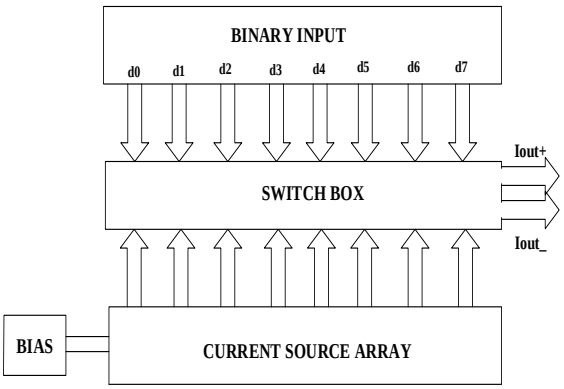

Fig. 1 Proposed CS-DAC architecture

8-bits binary weighted are the inputs of architecture. Based on the binary principle current sources are scaled. Here the i^{th} current source output current is equal to the 2^i.I,

Where $I=I_{LSB}$, i.e., least significant bit(LSB)current.

N-bit binary weighted CS-DAC output voltage in ideal case is given by

$$V_{out} = -V_{ref} \sum_{i=0}^{n} b_i \frac{1}{2^{i+1}} \quad (1)$$

For the design of DAC the best way is to associate the CMOS switches in place of current sources weighted. Here for N-bit converter, the N current sources are used, those are represented as: I_0, $2I_0$, $4I_0$ and $(2^{N-1})I_0$.The switches designed with CMOS technology acts as a current sources weighted are shown in figure 2.

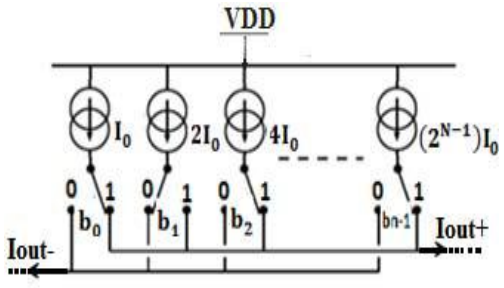

Fig. 2 DAC at switched current source

The output current is:

$$I_{out+} = (B_0 + 2B_1 + 4B_2 + \cdots + 2^{N-1} B_{N-1})I_0 \quad (2)$$
$$I_{out+} = KI_0 \quad (3)$$

And, its complementary":

$$I_{out-} = (B_0 + 2B_1 + 4B_2 + \cdots + 2^{N-1} B_{N-1})I_0 \quad (4)$$
$$I_{out-} = (2^N\text{-}1\text{-}K)I_0 \quad (5)$$

The total I_{tot}current drawn by the converter is:

$$I_{tot} = I_{out-} - I_{out+} = (2^N\text{-}1)I_0 \quad (6)$$

II. ARCHITECTURE OF CS-DAC

The architecture which is proposed in this paper explains the low power CS-DAC which is based on the two blocks in that one is current mirror circuit and the other is switches, where all the widths of all MSB'S and LSB'S are same for current source transistors. The complete schematic of proposed design CS-DAC is shown below figure 3.

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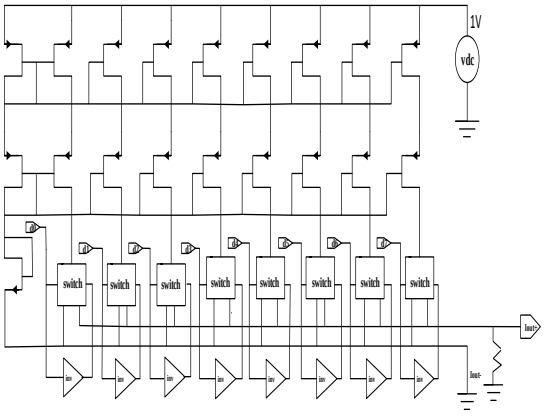

Fig. 3 Proposed CS-DAC schematic

The blocks used in this proposed architecture are:

Binary inputs, the block switches, current array sources, biasing voltages and filter.

1. Inputs

Here the binary inputs are used to control the switchers by using the PMOS logic signals d0, d1, d2, d3, d4, d5, d6 and d7 and also with their components d0b,d1b, d2b, d3b, d4b, d5b, d6b and d7b.

2. Switches

In this design the current coming from all the eight array sources are aligned by using this block switches as the output iout+ and iout-. And also controls the signals coming from the binary input. The ON/OFF characteristics at the branches of the DAC can be controlled by using this block switches as shown in figure 4. The dynamic characteristics are improved by keeping the switching times are equal to the current passing through the branches. The MOS transistor size is inversely proportional to the switching time. MOS switch corresponding to LSB is minimum and for MSB is maximum which is 128 times greater.

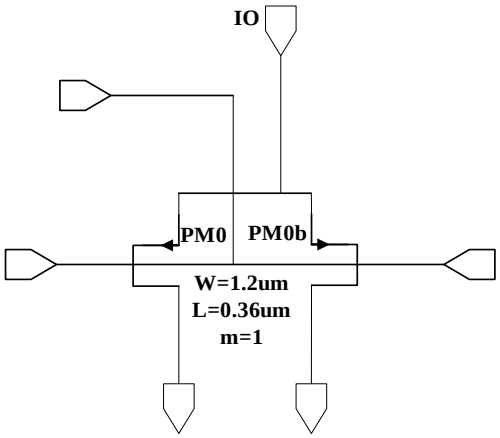

Fig. 4 schematic of the switch

Here the switches are designed simply by using PMOS transistors as shown in the below figure. These switches can be designed as pairs to form a differential pairs. The power source cutting is completely restricted by using this differential pair. Here the DAC output iout+ is mainly concentrated by connecting iout- to the ground as shown in figure 5.

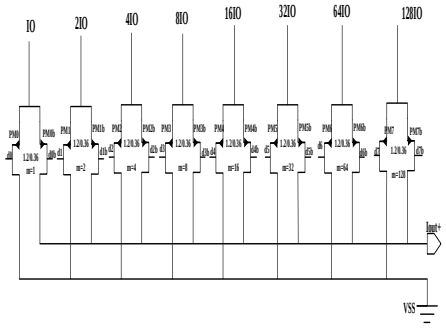

Fig. 5 the switches used in CS-DAC

3. Array of current sources

The current array sources are used to deliver the currents at 8 orders of switches which is equal in value. The design of these weighted current sources is easy technology using CMOS process. If the sources of units are combined with 2,4,8,… then easily avoid the noise.. The unitary sources are shown in figure 6.

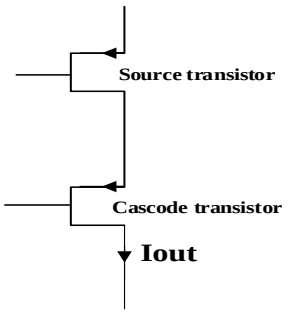

Fig. 6 Current Source

The current sources used in the DAC with the cascade sources are shown in below figure 7. Where the output is improved compared to the current mirror.

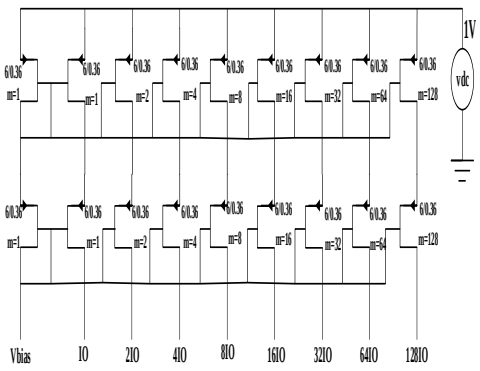

Fig. 7 The current source used in CS-DAC

4. Biasing voltages

The reference voltage is generated by using this block, which is represented as Vbias to polarize the PMOS current mirror cascades. The binary input signals d0 to d7 and their complements d0b to d7b control these PMOS switches. Here the D0 is the least significant bit (LSB) and D7 is the most significant bit.

5. With Filter

The CS-DAC with filter circuit is shown in below figure 8.

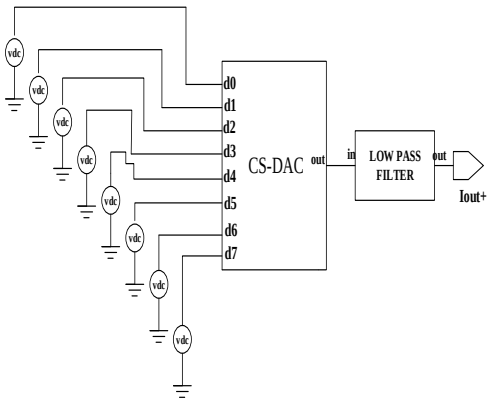

Fig. 8 The CS-DAC with filter circuit

The main purpose of the filter is to remove the some unwanted components from the signals. There are different kinds of filters are present. Here the low pass filter is used to smoothen the resulted signal output.

III. RESULT

Figure 9 shows the binary inputs (d0, to d7) of DAC from 8'b00000000 to 8'b11111111.

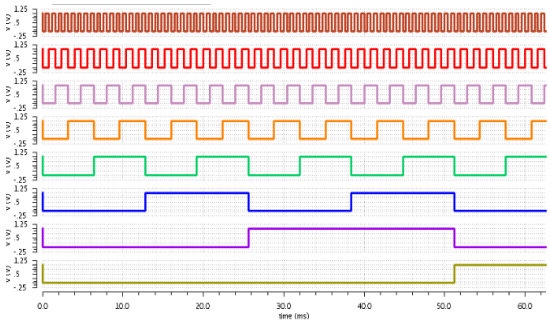

Fig. 9 inputs of CS-DAC 1LSB = $\frac{1V}{256\ bits} = 3.9V$

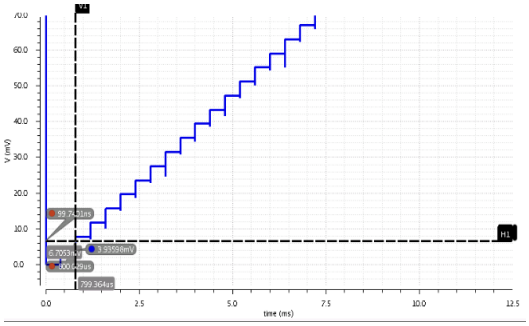

Fig. 10 Stair case output of CS-DAC Results

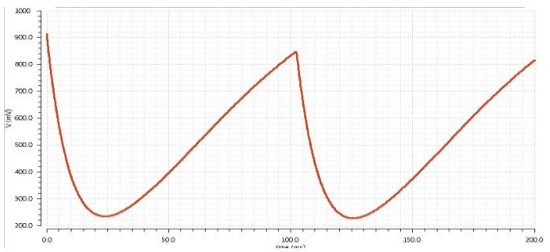

Fig. 11 simulation results of 8-bit CS-DAC after filter with 800MHz

The offset, gain error and DNL and INL calculations are described below.

INL/DNL: The integral non linearity is the one which is used to measure the performance of the DAC's and ADC's after the offset and gain errors are compensated. The differential non-linearity is the one which is also used to measure the performance by measuring the real and ideal widths at each level of the converter. INL/DNL plot is illustrated in figure 12.

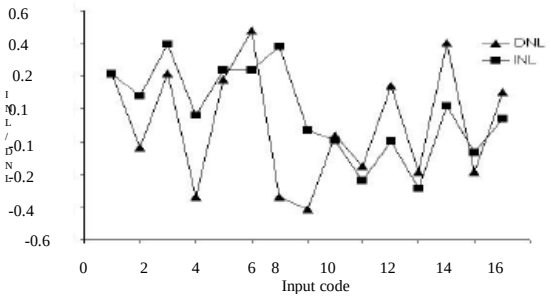

Fig. 12 INL/DNL plot at 800MHz

The transistors of source are selected by adjusting the lengths and widths to meet the specifications those are INL and DNL. Here the saturation voltage is closer to the transistor voltage VDs.

DAC Specifications

Table. 1

PARAMETERS	CS-DAC (PROPOSED)
Process	GPDK 0.18um
Supply voltage	1V
Resolution	8-bit
Full scale current	31.252mA
LSB size	246.594µA (1LSB)
Conversion rate	800MHz
Power dissipation	42.92uW
INL (LSB)	±0.3 (LSB)
DNL (LSB)	±0.718 (LSB)

IV. CONCLUSION

In this paper the design of low power 8-bit current steering DAC by using CMOS technology is presented. The test results are obtained with low power with high performance with frequency of 800MHz.The DAC's are mainly used in wide range of applications like digital audio applications, data communication applications and other types of applications.

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