Implementation of Asynchronous FIFO using Low Power DFT

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Abstract: An Asynchronous FIFO or First-in-First-out is a digital circuit to store data and to synchronize data transfers between two different clock domains. When data transfer happens between two different clock domains, it is very important to ensure that data is properly synchronized between the transmitter and the receiver so that no data is lost during the transfer. In any Asynchronous FIFO Design, data is written sequentially into the FIFO buffer in one clock domain and then the data values are read sequentially from the same FIFO buffer using another clock domain, where the two clock domains are asynchronous to each other. Asynchronous FIFO's are one of the most important building blocks for any System-on-Chip (SOC) Designs as they are the most widely used IP Blocks in multi-clock domain designs. In any SoC, low power has been the biggest challenge for any designer. Many low power techniques have come up at different phases of the design viz., Register Transfer Logic (RTL), Functional Verification, Logic Synthesis, Design for Test (DFT)and Physical Design. The two main areas in DFT where power has been a challenge is during the Scan Insertion Phase and during the Automated Test Patter Generation (ATPG) phase. Due to the additional scan circuitry being inserted during the testing phase, the power utilization has increased. Hence, the need for Low Power DFT techniques has arisen in all the SoC's that are being designed. In this paper, the primary focus has been on reducing the power for an Asynchronous FIFO at the DFT phase. The RTL Code is written in Verilog and synthesized using Synopsys Design Compiler. The aim of the experiment is to perform the low power DFT on the Asynchronous FIFO Net list and to compare the power reduction after applying the low power DFT technique and before applying the low power DFT technique. The Scan clock frequency is halved to reduce the power in the circuit without affecting any timing violations. As the Scan Clock frequency is low, it can be further reduced within permissible limits of the specifications to ensure that dynamic power is reduced without affecting the testing process of the chip.

Keywords: Low power DFT (Design for Test); UPF; CPF; Asynchronous FIFO; Scan Circuitry; Clock Gating; ATPG (Automatic Test Pattern Generation); Scan Clock; Net list; Pointers; SoC

I. INTRODUCTION

Most System-On-Chip (SoC) designers consider power as one of their top design concerns. With the technology shrinking and the complexity of the design increasing, the power has become a major challenge for most of the SoC designers.

The power related issues in the lower technology nodes have become a huge challenge for the ASIC Designers. Design for Testability (DFT) and Low Power issues are very much related to each other. SoC's with high complexity require huge test time and random data patterns thereby increasing the time for testing and the tester memory. The two most popular advantages of low power designs are:

a) Battery Life-time
b) Reliability of design

Hence, it becomes important to save power in parts of the chip that are unused. There are multiple IP's integrated in any SoC. These IP's typically are bought from Third-Party vendors like Synopsys or Cadence, or they are created the designers themselves. Every IP comes with its own specifications, standards and other requirements like Power, Voltage and Temperature (PVT). If the power management system of the complete SoC is not planned properly, there is every chance of the failure of the entire chip. In order to tackle the power management system for any SoC, each of the IP is moved into different power modes like power-on, power-off or sleep mode. Power consumption can be of two types, (i) Peak Power and (ii) Average Power. The Average Power can be further classified into:

(a) Dynamic Power Consumption
(b) Short-Circuit Power Consumption
(c) Leakage Power Consumption
(d) Static Power Consumption

This paper primarily focusses on reducing the Dynamic Power Consumption for an Asynchronous FIFO using Low Power DFT Technique.

The technique applied in this paper is a novel technique by the authors who are doing research on Low Power Design Techniques on Design for Testability methodology. This technique is scan clock reduction technique which is reducing the scan clock frequency for testability purpose without affecting any functionality or performance of the chip. Reducing the scan clock does not affect the performance of the chip because; the scan clock is used only for testing the manufacturing defects and it does not affect the functionality of the design. In every Design for Test methodology, every functional flop is replaced by an equivalent scan flop which is controlled by a signal scan enable. When scan enable is set to logic '1', then the test path is enabled and the functional path is disabled so that the functionality and the performance of the design is not affected.

Asynchronous FIFO Design

A typical asynchronous FIFO is used to synchronize data between two different clock domains. The read and write

operations happen at different clocks viz. write happens in the write clock domain and read happens in the read clock domain. Both the clock domains and asynchronous to each other. The Asynchronous FIFO design used in this paper is architected using a novel implementation, where, a signal last operation is used to detect the fifo full and fifo empty flags. When the write pointer is equal to the read pointer and the last operation is a write, then the fifo full flag is asserted and when the write pointer is equal to the read pointer and the last operation is a read, the fifo empty flag is asserted. This is how the fifo full and fifo empty flags are generated in this novel architecture of asynchronous FIFO Design.

Scan Design Phase

Scan synthesis is the process of converting a testable design into a scan design without affecting the functionality of the original design. As shown in fig 2: the different steps involved in the Scan Design Flow are as follows:

(i) Scan Configuration
- Number of scan chains used
- Type of scan cells used to implement these scan chains
- Types of storage elements to exclude from the process
- Arranging the scan cells

(ii) Scan Replacement
- Replaces all original flip flops with their equivalent scan flip flops.

(iii) Scan Reordering
- The process of reordering the scan chains based on the physical scan cell locations, in order to minimize the amount of interconnect wires used to implement the scan chains.

(iv) Scan Stitching
- Stitch all scan cells together to form scan chains.

During the ATPG Simulations phase, the following steps take place: [11]
a) Read Synthesis Net list from Design
b) Read ATPG Library Files, test procedure files and do files
c) Build ATPG Model
d) ATPG DRC Checking
e) Generate Fault List
f) Generate Test Vectors
g) Validate Test Patterns Using Simulations

Low Power Specification Formats

The two common formats used in the Industry for Power savings are:
i.   Unified Power Format(UPF)
ii. Common Power Format(CPF)

While UPF Design flow is implemented with the help of Synopsys electronic design automation tools and tested on Synopsys generic 90nm and 32/28nm libraries, CPF Design flow was designed by Cadence Design Systems and then contributed to Si2. UPF has been driven mainly by Synopsys, Mentor Graphics and Magma. There is very subtle difference between the two flows. Most of the companies follow both the flows. Either of these flows are used to reduce power consumption at various levels of the ASIC Design Flow. [12]

II. LOW POWER DFT TECHNIQUES

Some of the commonly used low power techniques for

DFT used in the industry are:

a) Clock Gating Circuitry

It is a technique used for reduction of power consumption in power-on domain by blocking the clock dynamically before reaching a set of flip flops or latches. It is like switching off the clock when it is not being used functionally. Since continuous switching consumes lot of dynamic power, this technique helps to save power when clock is not being used. [13]

b) Power Domains

Separating the whole design into different power domains will ensure that each one of the block can powered down or powered up individually by controlling the power switches utilized for gating the power supply connection to every power domain block. [14]

c) Low Power Cell

While testing the design, the capacity of the State preservation registers to keep hold of their state needs to be verified when the power domain is powered off. Isolation cells are located at the limit of two power domains keeping in mind to isolate the power-on and power-off domains.

d) Multiple Supply Voltages

Based upon the operating conditions, different power domain blocks are subject to different supply voltages, and each power domain block is connected to other power domain block with the help of level shifters.

e) Power Aware DFT

Once the Scan synthesis starts, the functional flops are replaced by their scan equivalent flops. During the scan stitching process, the power aware DFT is applied by the respective power domain after the partitioning of scan chains under the condition that there are adequate scan I/O's in every power domain and they can have their dedicated scan I/O's, control signals and test clocks.

This guarantees that every power domain is having dedicated scan chains which are active in the power domain which in ON. [15][16]

f) Power Switches

In order to minimize the power dissipation, particularly leakage power dissipation caused by the shrinking power technologies, power switches are generally employed in modern low power design circuits. One or more power switches are equipped at different parts of the design to facilitate the functionality of power gating.

III. IMPLEMENTATION OF THE LOW POWER DFT TECHNIQUE

In the current implementation in this paper, for the Low power DFT, we have adjusted the frequency of the SCAN Clock in such a way that it meets the design specification and also directly resulted in reducing the power consumption on the circuit.

The input design is a PLL with multiple clocks. The gate level net list is taken as input for doing the DFT process and implementing the low power DFT technique of decreasing the SCAN Clock frequency and dividing it into multiple power domains. Here the emphasis is on reducing the dynamic power.

The general representation of CMOS logic gate for Switching Power Calculation is shown in fig3:

$$P_{avg} = \frac{1}{T}[\int_0^{T/2} Vout \quad (-C_{out}\frac{dV_{out}}{dt})dt + \int_{T/2}^{T}(V_{DD} - V_{out})(C_{load}\frac{dV_{out}}{dt})dt]$$

------- (1)

The average power consumption can be expressed as

$$P_{avg} = \frac{1}{T}C_{load}V_{DD}^2 = C_{load}V_{DD}^2 f_{CLK}$$

---------- (2)

The transition rate of the nodes can be slower than that of the clock rate. For better representation of this behavior, a node transition factor ($\propto'$) must be introduced

$$P_{avg} = \propto_T C_{load}V_{DD}^2 f_{CLK}$$

– -------- (3)

The generalized expression for the average power dissipation can be rewritten as

$$P_{avg} = (\sum_{i=0}^{\#of nodes} \propto_{Ti} C_l V_i)V_{DD}F_{CLK}$$

----------- (4)

As we can see from Equation 4, Power is directly proportional to the clock frequency. Hence, reducing the clock frequency such that it falls between the specification ranges, the power can be reduced without affecting the timing violations there by.

IV. RESULTS

The results of this experiment at the Scan Synthesis level, after varying the scan clock frequency is tabulated in Table 1 As can be seen from the table.1 it is evident that the power has reduced by approximately 50%.

By reducing the scan clock frequency by half, the power also has reduced by 50% which is compliant to the equation 2. This is the reduction technique for dynamic power which is also the switching power in any SoC. Here, the reduction in the scan clock frequency does not affect the functionality of the design and neither the performance of the design, The scan enable of the scan flip flop ensures that only the test path of the chip is enabled and not the functional path. The functional path is disabled during the DFT phase.

From the fig 4, we can observe the decrease in power after applying the low power technique in Design for Test methodology as discussed in section3.

V. CONCLUSION

As, we can see from the above results, when the clock frequency is reduced from 50 MHz to 25 MHz, the power is also reduced by nearly 50%. What is important here, is that these results have been calibrated by ensuring that there are no setup or hold violations in the circuit after varying the clock frequency. The equation 3 clearly is henceforth proved that power is directly proportional to frequency. One of the next techniques which will be applied in the next version of the paper will be dividing the SCAN Clock for even and odd chains and thereby reducing the power consumption in the scan chain.
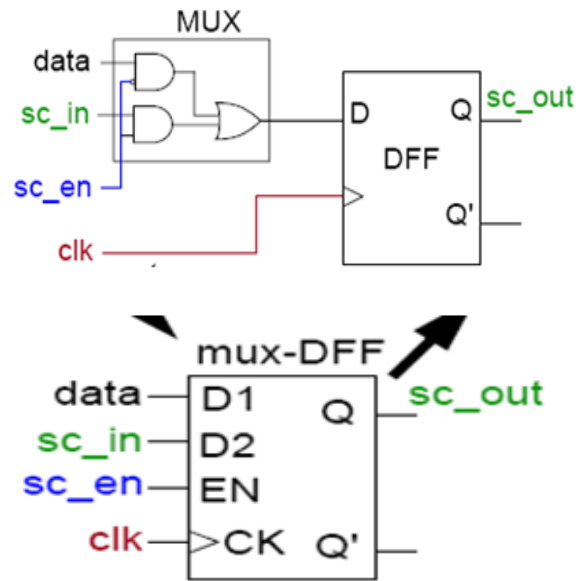
Tables and Diagrams
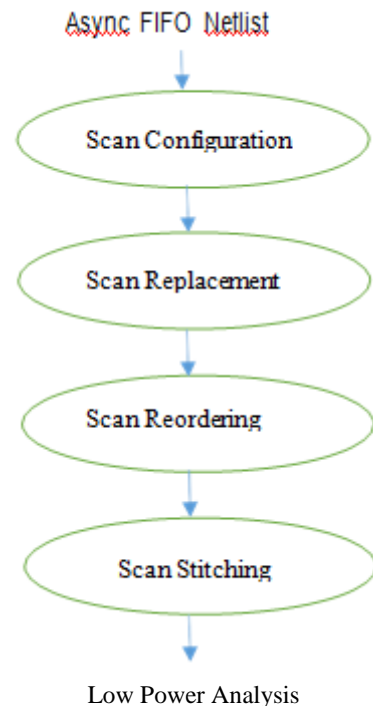

Fig. 1 A Typical Scan Flip Flop
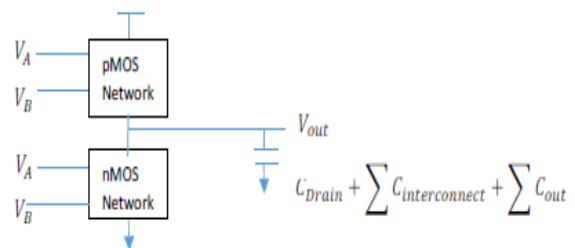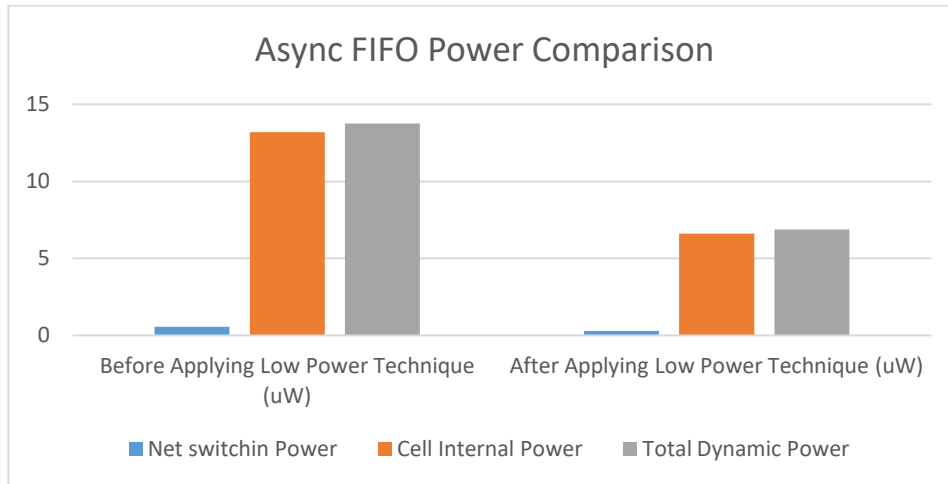

Fig. 2 Scan Design Flow

Fig. 3 CMOS Logic Circuit foe power calculation

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Async FIFO Power Comparison

Legend: ■ Net switchin Power ■ Cell Internal Power ■ Total Dynamic Power

Fig. 4 Graphical representation of power comparison for the Asynchronous FIFO Design

Table. 1 Comparison table showing the power values before and after applying Low power technique for Asynchronous FIFO

Parameter	Before Applying Low Power Technique	After Applying Low Power Technique
Global Operating Voltage	0.95	0.95
Power-specific unit information		
Voltage Units Capacitance Units Time Units Dynamic Power Units Leakage Power Units	1V 1.000000ff 1ns 1uW (derived from V,C,T units) 1pW	1V 1.000000ff 1ns 1uW (derived from V,C,T units) 1pW
Cell Internal Power	13.1903 uW (96%)	6.5952 uW (96%)
Net Switching Power	559.9319 nW (4%)	279.9659 nW (4%)
Total Dynamic Power	**13.7503 uW (100%)**	**6.8751 uW (100%)**

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