Electrical Characteristics of Double Gate FINFET Under Different Modes of Operation

K.Sarath Chandra, K Hari Kishore

Abstract: ***CMOS scaling has provided the enhancement of VLSI industry for its miniaturization of devices as well as increase in the operating speed at the expense of power dissipation. The three metrics of VLSI industry speed, area and power are interlinked to each other such that one metric has to be compromised for another metric to have better value depending on which particular application to be targeted. Furthur sclaing of cmos is not possible because of material and process technology limits. Because of second order effects prevailing in CMOS researchers are looking for alternative replacement for CMOS which overcomes the second order effects existing in CMOS scaling and provide very less power dissipation. Now a day's power dissipation is very crucial parameter because of miniaturization of devices a feature called portability came in to picture where battery is essential requirement. The battery technology has not evolved as much as the VLSI technology as evolved over the years which has left no option for the designers to design the devices which consume less power and give more battery life which is the most primary requirement from customer point of view. In this regard FINFET is found to be one of the right substitute for CMOS to design the applications which are targeted to have low power delay product. FINFET electrical characteristics are plotted under different modes of operation and leakage currents are compared for N-Type and P-type FINFETs, and concluded that back gate biasing reduces leakage currents.***

Keywords: FinFET, MOSFET, 32 nm Technology, Power, Speed

I. INTRODUCTION

In the VLSI industry, both Arithmetic and Logic low-power circuits have become very important. Due to the rapid increase in the usage of the portable electronic devices, the VLSI design efforts are mainly focused on low-power circuits with high-speed computation. In various DSP processors, Multiplier and Adder circuits are the main building blocks of the Arithmetic Unit. In such processors, certain parameters like power, area, delay-time, etc. have to be given due consideration for efficiency. The designers are thus forced to concentrate on addressing the constraints like high speed, small area, high throughput, and low power consumption [1-3]. As innovation downsizes to 32nm and beneath, the present Complementary Metal-Oxide semiconductor (CMOS) innovation has confronting as far as possible.

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This issue is because of the expanded leekage control dispersal, the expanded short-channel impacts, extreme process varieties, high power thickness, etc. To beat this scaling limit, the specialists are probed different innovations. Among which FinFET innovation has been assessed as one of the promising substitution to MOSFET of CMOS innovation.

The power dissemination in CMOS incorporates dynamic and static segments. The power dissemination is because of leekage current in stand by mode. The dynamic power dissipation is mainly due to because of switching power which arises because of charging and discharging capacitance and another is because of short circuit power which arises because of non zero rise time and fall times.

Decrease of supply voltage diminishes control dispersal, this is on the grounds that the power dissemination has quadratic association with the supply voltage. Be that as it may, decreasing supply voltage corrupts the execution. With the end goal to fulfill the superior necessities, VTH must be scaled. Woefully, such scaling prompts significantly increment in spillage current, which turns into another real worry for low power and superior circuit plans [4]. Prior in micrometer innovations the dynamic power is the prevailing part of aggregate power yet in nanometre advances spillage control is the predominant segment. Beginning at 70nm semiconductor innovation, spillage power will contribute with 50 % to add up to circuit's capacity [5].

II. FINFET TECHNOLOGY

Two fold entryway FinFETs, can conquer the scaling deterrents [6] [7]. the front and back entryways might be made autonomous and one-sided to control the current and the gadget edge voltage The most essential element of FinFETs is that [8]. The capacity to control limit voltage varieties offers an adaptability to diminish reserve control dispersal. FinFET is viewed as promising innovation that can affect the prompt future because of its low spillage control utilization, superior.[6].

FinFETs ability to configure the back gates to provide greater speed and greater leakage control gives the scope for the designers to use FinFET to have low power delay product.

III. MODES OF OPERATION

FinFET's can be worked in three methods of activity i.e. hamper, low power mode and autonomous door mode. The geometry of FinFET permit less spillage current in light of their solid power over the channel.

This transistor design is of shorted door (SG) and is delineated in Figure 1.(a). In the low-control (LP) working mode, exhibited in Figure 1.(b), use of turn around predisposition on the back door lessens spillage current incredibly (Ioff). Having a back-entryway inclination of -0.2V on a n-type FinFET diminishes Ioff by 85% of a tantamount SG FinFET [7]. A pivot tendency unfavorably impacts the on current (Ion) of the transistor. Molecule diminishes by about 60% in the LP mode when the pivot tendency is set to - 0.2V for a n-type transistor [7]. Littler turn around predispositions effectsly affect Ioff and Ion, yet to a lesser degree [7]. The back-door can be fixing to another info, prompting autonomous entryway (IG) working mode, imagined in Figure 1.(c). In any case, the FinFET's entryways might be made free (additionally alluded to as a MIGFET, or different autonomous door FET) to consider separate authority over the front-and back-doors [5].The electrical properties are plotted for sc door and low power method of activity for forward and switch predisposition.

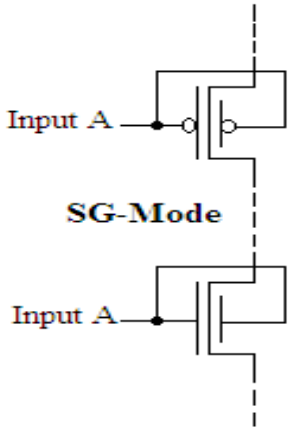

Fig. 1 (a) Shorted-gate (SG) mode FinFETs

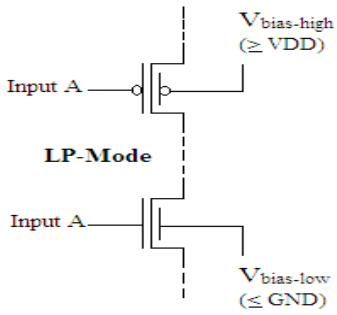

Fig. 1 (b) Low-power (LP) mode FinFETs

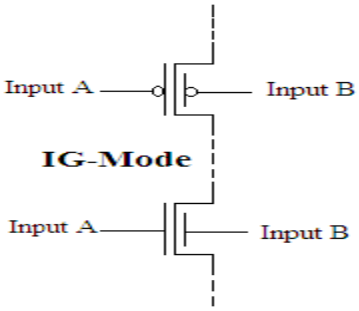

Fig. 1 (c) Independent-gate (IG) mode FinFETs

Table. 1 FinFET Technology Model

Parameter	Value
Fin height (Hfin)	70 nm
Fin thickness (TSI)	14 nm
Oxide thickness (Tox)	1.1 nm
N-Channel Surface Orientation	<105>
Length of gate (LG)	25 nm
Source to gate /drain underlap (LSD)	10 nm
Gate thickness (TG)	20 nm
Gate work function (ΦG)	4.4 eV (n-type) 4.8 eV (p-type)
Mobility	560 cm2/(V-s) (n-type)
	200 cm2/(V-s) (p-type)
Doping of Fin body (N Body)	1014 cm-3
Drain/ Source resistance (RSD)	180 Ω-µm
Voltage Supply (VDD)	1 V
Source/drain doping (NDS)	1020 cm-3

IV. SIMULATION RESULTS

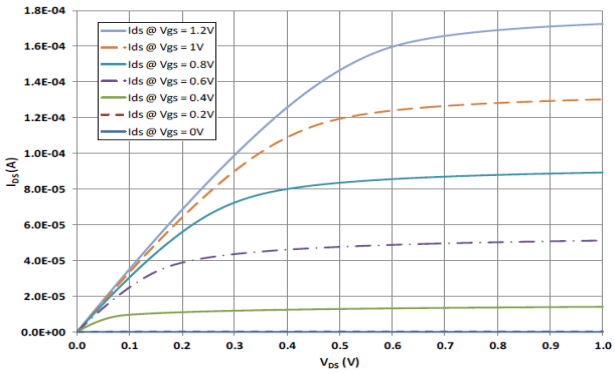

Fig. 1.1 n-type SG-mode

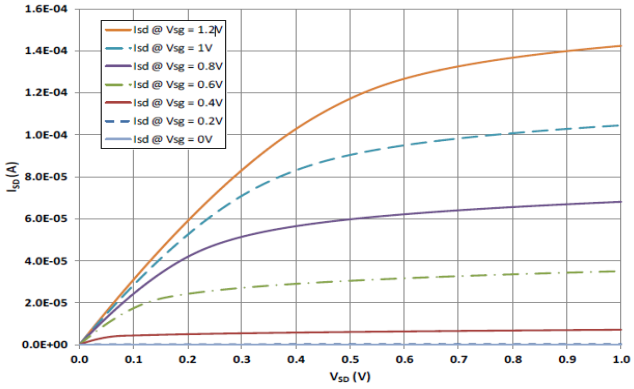

Fig. 1.2 p-type in SG-mode

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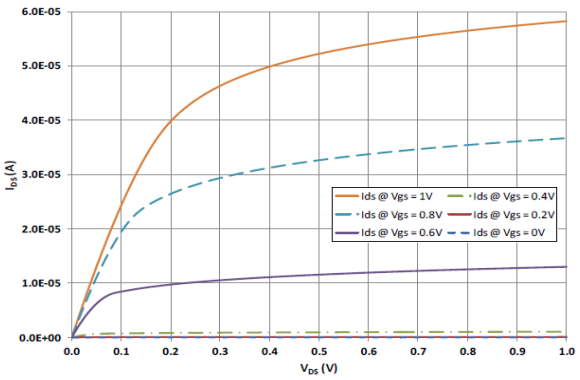

Fig. 1.3 waveform for 0 V back-gate bias in LP mode

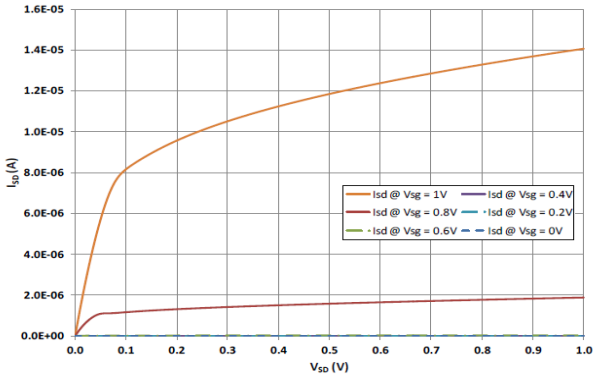

Fig. 1.4 waveform for VDD back-gate bias in p-type with LP-mode

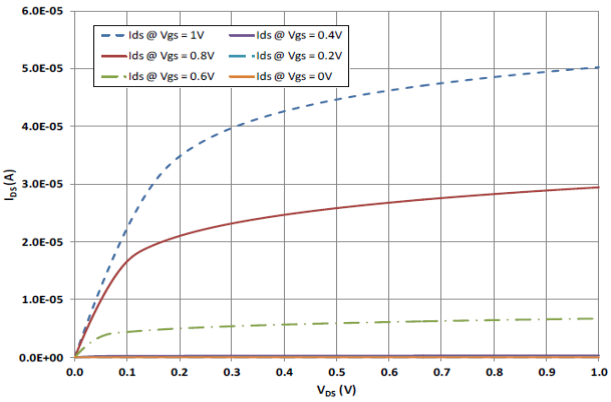

Fig. 1.5 waveform for -0.4V back-gate bias in n-Type with LP-mode

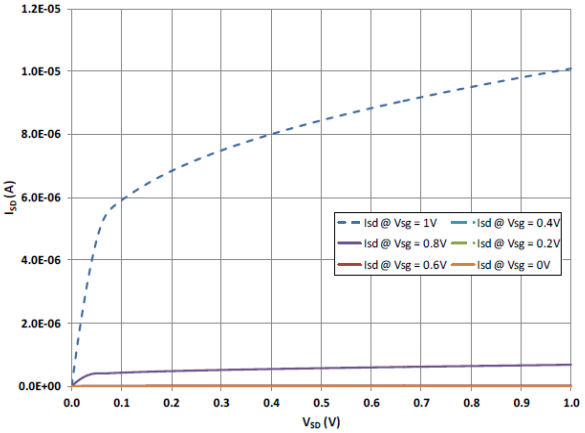

Fig. 1.6 waveform for 1.4 back-gate bias in p-type with LP-mode

Table. 2 LP-mode FinFET Ion and Ioff currents for various back-gate bias voltage

N-TYPE FinFET			P-TYPE FinFET		
Back-Gate Bias(V)	Current		Back-Gate Bias (V)	Current	
	I_{on} (μA)	I_{off} (pA)		I_{on} (μA)	I_{off} (pA)
-0.4	41.6	1	1.4	27.9	0.2
-0.3	45.3	2	1.3	29.7	0.8
-0.2	49.3	15	1.2	32.7	3
-0.1	53.2	65	1.1	35.7	12
0.0	57.2	360	1.0	38.8	70
0.1	61.3	2560	0.9	42.0	490
0.2	65.6	14600	0.8	45.1	3600
0.3	68.7	22400	0.7	47	7900
0.4	72.7	30300	0.6	49.6	13570

Table. 3 FinFET leakage current for LP configuration (pA)

CONFIGURATION		Leakage Current (pA)	
N -TYPE(V)	P-TYPE(V)	N-TYPE	P-TYPE
-0.2	+1.2	15.6	3.2
0	V_{dd}	372	75

V. CONCLUSION

We have observed that when we make forward bias on the back gate then on current increases lightly where as Ioff current increases exponentially. When we apply reverse bias to back gate there is slight linear increase in Ion where as the off current decreases exponentially giving a better Ion: Ioff ratio. Further it is investigated that in low power shorted gate configuration back gate biasing will reduce leakage currents. we also conclude that solitary balance n-type FinFET has around 5X more spillage current than a solitary balance p-type FinFET; explicitly 4.91X if in LP design with inclinations at - 0.2 V for n-type and 1.2 V (VDD+0.2V) for p-type, 4.96X if in LP setup with predispositions at 0 V for n-type and 1V VDD for p-type. FinFETs capacity to arrange the back gate to give more prominent speed and more prominent leakage control gives the scope for the designers to use FinFET to have low power delay product.

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