RF Front-End Design of Inductorless CMOS LNA Circuit with Noise Cancellation Method for IoT Applications

Mahesh Mudavath, K Hari Kishore

Abstract- This manuscript deals the RF Front-End Design of Inductorless CMOS LNA Circuit with Noise Cancellation method for IoT Applications. A reconfigurable, Inductorless, wideband, LNA for multi-standard wireless applications among a less-area, single-chip, and RF front-end are presented in this manuscript. In this context the proposed LNA approaches two paths in parallel: CS (common-source) path and CG (common-gate) path. Here CS path is liable for providing adequate gain, at the same time the CG path achieved as the matching of input impedance. In this CG path the noise involvement can be removed by noise cancellation technique consequently, on the whole Noise Figure is enhanced. The mismatch of phase among the 2 different paths is moreover quantitatively investigated with analyze to its effect on NF and gain. The methodical values agreed to fit with their simulation values. The considered LNA designed in a CMOS 45nm technology process. The simulated result with the frequency range of 1.04GHz with bandwidth of 3dB gain has achieved 22 dB gain and a low NF of 1.9 dB. The obtained 1dB compression point (IP_{1dB}) is -22.4dBm and also LNA consumes only 6.5mA with 1.2V power supply.

Keywords: Low Noise Amplifier, CMOS Technology, Inductorless, noise cancellation method, Noise Figure, IoT, WSN, common gate path and common source path.

I. INTRODUCTION

The speedy expansion of wireless sensors in favor of Internet of Things [8] led to massive enhance by compression of chip area and less consumption of power [1]. The emerging standard of the Internet of Things (IoT) [2] and the rising interest for wireless sensor networks (WSN) [6] push towards the implementation of large networks of wireless systems and sensors. The representation of Internet of Things [8] is as an international network of things/objects interconnecting. In an IoT area the technologies of wireless were important due to the suitable and less cost wireless connections among IoT nodes. Wireless technologies are frequently deployed in inaccessible locations or remote area. [8]. Wireless Sensor Network standards like family of IEEE 802.15.4 [4,18] entail significantly low power consumption (P_{dc}) for inaccessible locations or remote applications by way of long lifetime battery.

The particular case of WSN standards [16] the 1.04 GHz industrial, scientific and medical (ISM) band typically leads to RFICs [13] using LNA's circuit design with multiple inductors. For that reason these bulky spiral inductors result in costly RFIC [10]. So avoiding them is absolutely a cost effectual approach. On the contrary, low P_{dc} inductor less CMOS LNAs can't offer the less NF of those inductor components based counterparts. Such less cost Receiver circuits are very challenging to Designing. To be significant for a WSN application, an inductorless CMOS LNAs should offer a high voltage gain, as well as significantly reduced silicon chip area [4]. Moreover, RFIC SoC structures should handle the amplified NF and Inductorless LNA for inherent wideband nature [9].

An Inductorless device of RF front-end circuits been broadly studied in modern days in both educational and engineering fields [1].The intention behind is to meet these necessities. An Inductorless circuit resides in very smaller area chip [4], [5] when compared with the long-established RF circuits, with regards to having inductive devices on-chip [1].

The Design of Inductorless CMOS LNA Circuit with Noise Cancellation method for IoT Applications is highlighted in this paper. The proposed LNA includes a CS & CG path [7,19] [Fig. 1-3 follows]. To stability the parameters such as linearity, gain and the consumption of power, the CS topology is used to offer sufficient power gain, although the CG is functional to matching I/P impedance. The method of noise cancelling technique is adopted to decrease the noise involvement of the path CG Fig.2 shows. Compared with CS, in the interim, the power gain & the total NF performances are also improved further. It has been experiential that the proposed LNA's linearity has little effect on the CG path [3]. Consequently, the bias voltage of the circuit and power consumption is optimized to reduce in the CG path. The different noise cancellation of paths for CMOS LNAs goes during bring in a phase mismatch among the 2 parallel paths. This phase mismatch harmfully impacts the system noise cancellation & gain [20]. For that reason, its cause on performance of NF and gain is furthermore quantitatively with analyzed in this paper [1].

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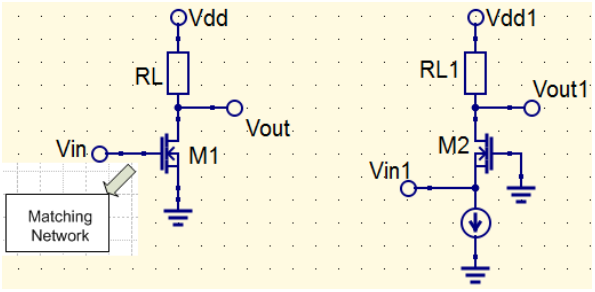

Fig. 1 Simplified CS and CG amplifier

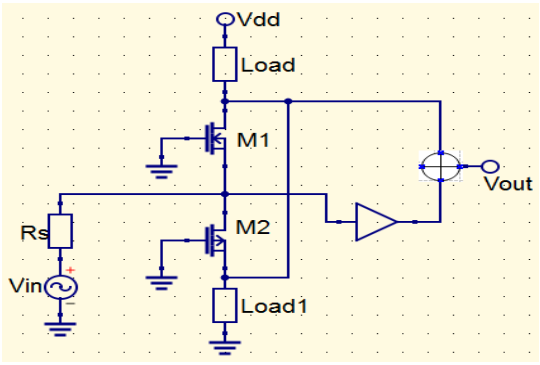

Fig. 2 Simplified circuit of noise cancellation CMOS LNA

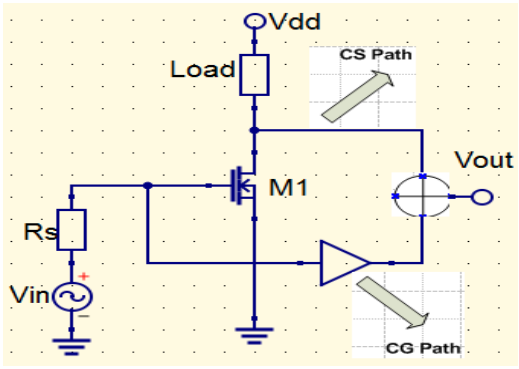

Fig. 3 The CS & CG path LNA

The remainder of the paper is organized as follows: Section II presents the literature of inductorless CMOS LNA; Section III presents the design of LNA with parallel path approach with allowing for the phase mismatch; and also section IV deals the achievement and measurement values; Finally, Section V concludes the work.

II. LITERATURE OF INDUCTORLESS CMOS LNA

An Inductorless CMOS LNA structure is essentially based on circuit techniques for low impedance of input even as maintaining excellent performance of gain and noise. The generation of primarily real input impedance whilst a CMOS exhibits usually capacitive large input impedance is difficult to occur [17]. A clear-cut solution might be discrete matching using 50Ω input impedance bounding the NF to less than 2 dB in argument with low noise goals shown in Fig.2. A more sensitive approach key points to circuits whichever based on common source (CS) and/or common gate (CG) amplifiers [9]. Schematics circuit diagram of these architectures are shown (Fig. 1-3)[4].

The signal received at the antenna terminal of the receiver is reasonably weak so good gain and noise performances are essential requirements for LNA. Its most important function is to offer adequate gain to beat the noise of the subsequent stages. LNA design involves the tradeoff between gain, linearity, NF and power consumption [11,12]. The LNA design optimization technique is used to build tradeoff between gain and linearity [4].

Fig. 4 Tradeoff between parameters

III. DESIGN OF LNA WITH PARALLEL APPROACH

1. CS PATH

The path of CS is realized by a 2 stage amplifier as shown in Fig. 5. The 1st stage consist a transistor M_1 & resistor R_1. The 2nd stage, consisting of transistors M_2 and M_3 resp., to drive 50Ω load of measurement, then the component size of M_3 has so optimized as to attain nearly 20mS $gm3$. The equivalent small ac signal model is exposed in Fig. 6. Ignoring the components of parasitic capacitors i.e., C_{gs}, C_{gd}, *etc*. of the MOS transistors and presumptuous the input impedance (Z_{in}) is matched with R_s, then the voltage gain of CS path's is given by [1]

$$A_V^{CS} \approx \frac{1}{2} g_{m1} R_1 \frac{g_{m2}}{g_{m3}} \quad (1)$$

Where g_{mi} denotes the transconductance of transistor *Mi*.

2. CG PATH

The CG amplifier which consists of transistor M_4, resistor R_2, and a current (dc source) I_1 is adopted to schematic design circuit with CG path in favor of achieving the perfect matching input impedance as depicted in Fig. 7. The input impedance of the LNA design is conquered generally by the transconductance [1,14] of transistor M_4 (gm_4) thus, gm_4 of roughly 20mS has elected to match with R_S. According to the equivalent small signal ac model as Fig. 5 shows, so the voltage gain of the selected CG among the adder is described as [1]:

$$A_V^{CG} \approx \frac{1}{2} g_{m4} \beta R_2 \quad (2)$$

Where β is the small signal transfer function starting the gate of M_3 to the source of M_3 and is specified by

$$\beta = \frac{g_{m3}(r_{o2}\|r_{o3})}{1+g_{m3}(r_{o2}\|r_{o3})} \quad (3)$$

Where r_{oi} refers the drain output side impedance of M_i transistor. In fact $g_{m3}(r_{o2}\|r_{o3}) \gg 1$ for the advanced CMOS technology [15] and β value is approx taken as 1[1].

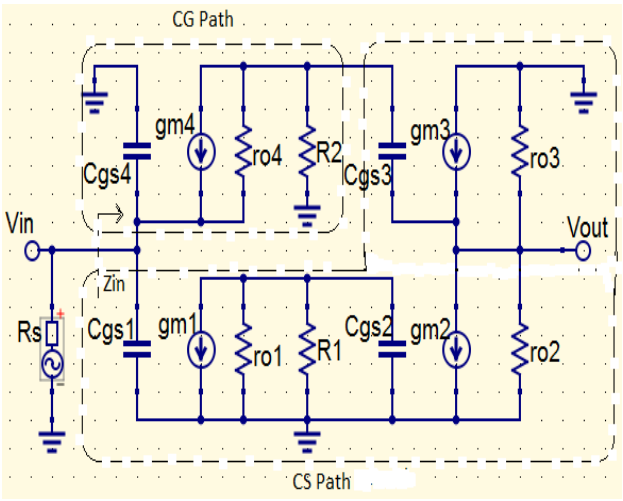

Fig. 5 an Equivalent small signal model of the CMOS LNA

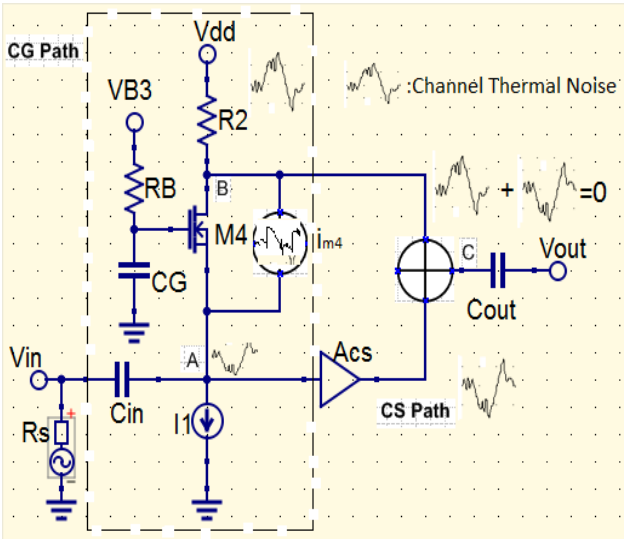

Fig. 6 noise cancellation technique

Unlike the input impedance matching N/W's associated with inductors or/and transmission lines, and the component of active components generate plenty of noise power. Consequently, a scheme of noise cancellation technique is implemented to diminish the noise of M_4 $(\overline{i_{M4}^2})$ which is the primary noise generator within the path of CG. As illustrated in Fig. 6, $\overline{i_{M4}^2}$ causes two immediate voltage responses, one each at node A & B, by opposite signs, exposed as shown beneath [1]:

$$v_{A,M4} = i_{M4}(Z_{in}\|R_s) \approx i_{M4}\frac{1}{2g_{m4}} \quad (4)$$

$$v_{B,M4} = -i_{M4}(1 - g_{m4}R_s/2)R_2 \quad (5)$$

At node A the noise voltage $v_{A,M4}$ is amplified by using CS path. By the side of the output node 'C', having noise voltage (v) transferred by $v_{A,M4}$ is given by

$$v_{A,M4}^o = 2A_V^{CS}v_{A,M4} = i_{M4}A_V^{CS}/g_{m4} \quad (6)$$

In view of the phase mismatch between the CG & CS paths is (Δθ), the output of the noise voltage (v) transferred by $v_{B,M4}$ is revised thus:

$$v_{B,M4}^o = \beta v_{B,M4}e^{j\Delta\theta} = -i_{M4}(1 - g_{m4}R_s/2)\beta R_2 e^{j\Delta\theta} \quad (7)$$

By the side of output node 'C', the total noise voltage accumulated by *M*4 is calculated thus:

$$v_{C,M4} = v_{A,M4}^o + v_{B,M4}^o$$

$$= i_{M4}\left[\frac{A_V^{CS}}{g_{m4}} - \left(1 - \frac{g_{m4}R_s}{2}\right)\beta R_2 e^{j\Delta\theta}\right] \quad (8)$$

To reduce the noise contribution of M_4, the circuit needs to be satisfied thus:

$$\left(1 - \frac{g_{m4}R_s}{2}\right)\beta R_2\cos(\Delta\theta) = \frac{1}{g_{m4}}A_V^{CS} \quad (9)$$

As already mentioned, $g_{m4} = 1/R_s$. Substituting (9) for (2), the relationship between A_V^{CS} and A_V^{CG} for the best noise cancelation is obtained by

$$|A_V^{CG}| = \frac{1}{\cos(\Delta\theta)}|A_V^{CS}| \quad (10)$$

Taking into consideration the phase mismatch among CS & CG paths have been aggregated in adder. Then on the whole voltage gain is revised as:

$$A_V^T = A_V^{CG} + A_V^{CS}(\Delta\theta) = \frac{1}{2}\left(g_{m1}R_1\frac{g_{m2}}{g_{m3}} + g_{m4}\beta R_2 e^{j\Delta\theta}\right) \quad (11)$$

To attain optimally revoke the noise power of M_4, the ratio

of A_V^{CG} *and* $A_V^{CS}(\varphi)$ can be calculated thus:

$$\varphi = \frac{A_V^{CG}}{A_V^{CS}} = 1 + jtan(\Delta\theta) \quad (12)$$

IV. SIMULATION RESULTS

In the design of proposed inductorless LNA, the generated simulations were carried out using Spectre RF from Cadence design suite. These selected LNA structure working at the frequency of 1.04 GHz and design was using CMOS 45nm technology process. Fig. 8-13 shows simulated results and S-parameters result of CMOS LNA [22]. The LNA achieved to acquire a voltage gain (S_{21}) of 22dB and Fig.9 shows the NF 1.9 dB. The input return loss, S_{11} is -12.5 dB & output return loss S_{22} is -11.3 dB. The attained value of NF is supposed to be good as it exceeds the constraint which is normally less than 2 dB without having to tradeoff the power gain which also satisfies the prerequisite and, also obtained Simulated 1dB compression point (IP_{1dB})=-22.9dBm shown in Fig.13 [22].

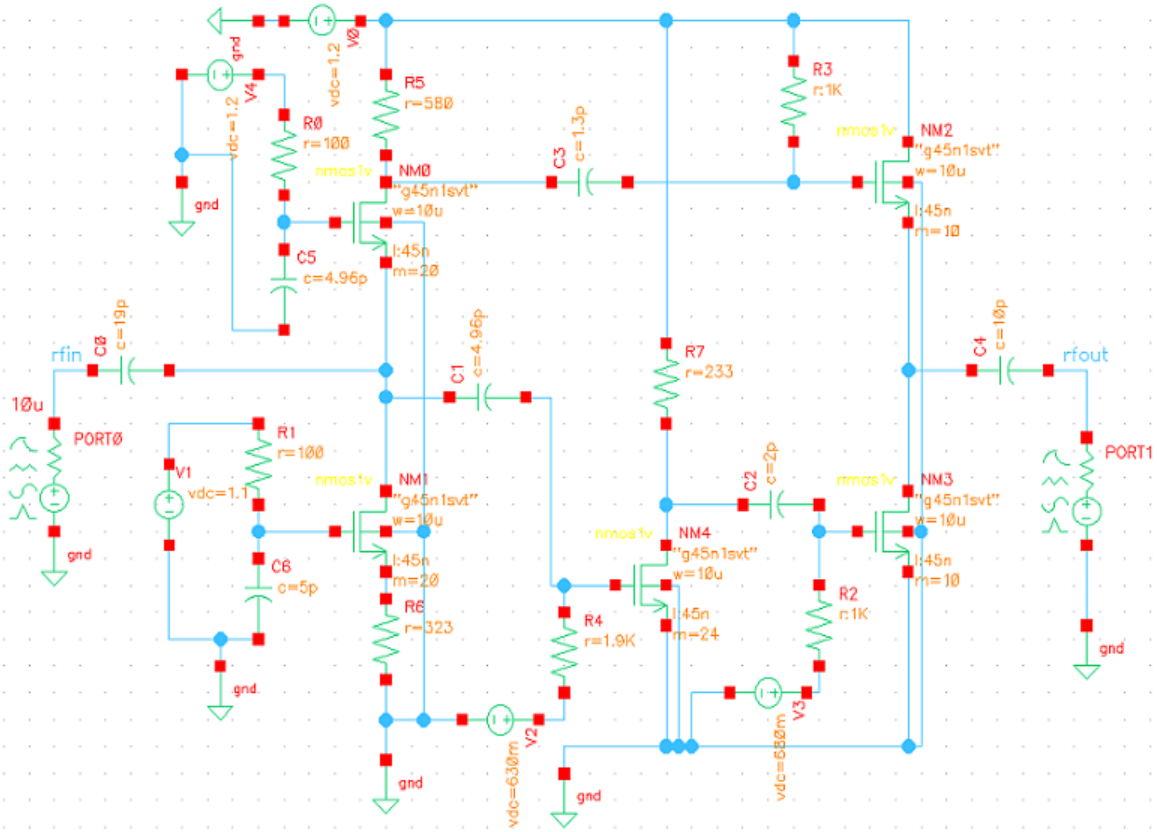

Fig. 7 The Schematic of the proposed LNA

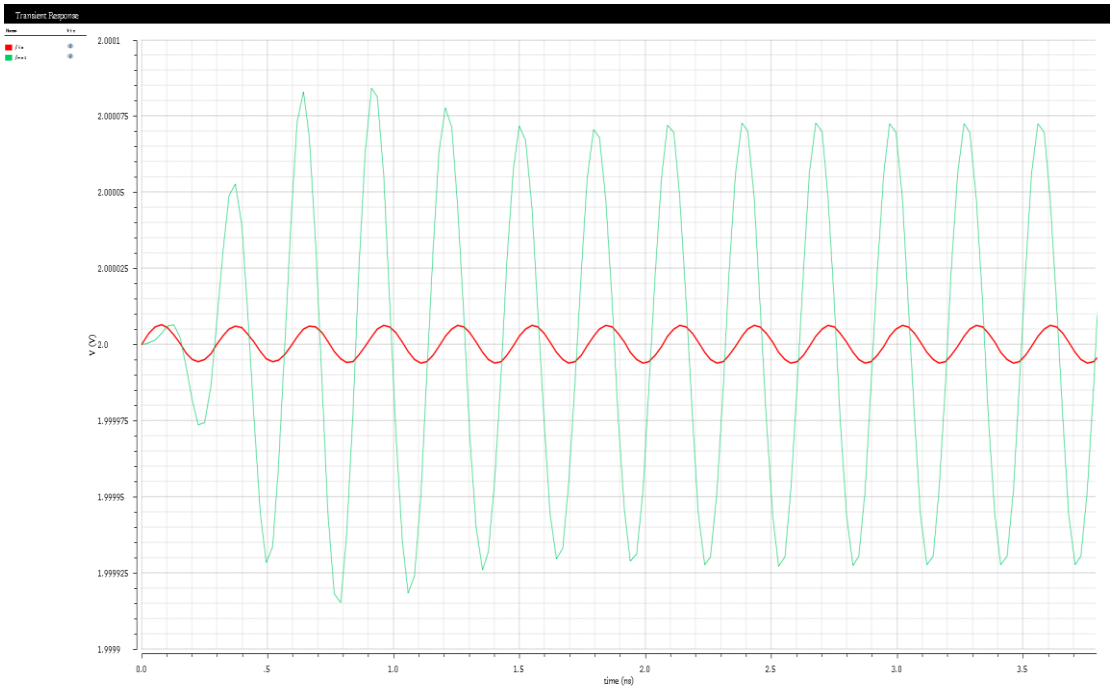

Fig. 8 Input (red signal) and amplified output (green signal)

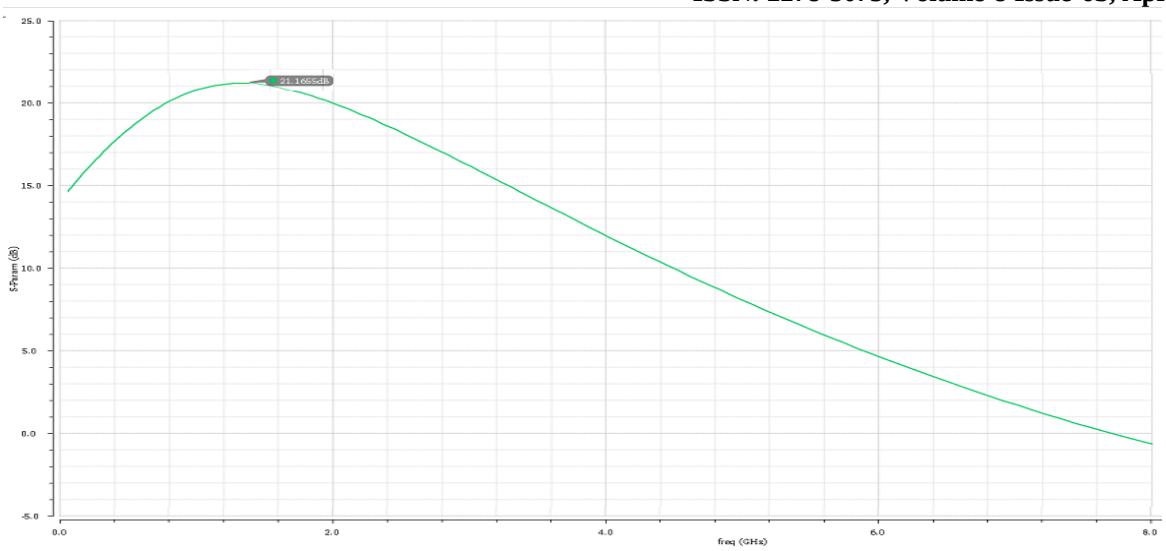

Fig. 9 Simulated voltage gain S_{21}=21.66dB @ 1.04GHz center frequency

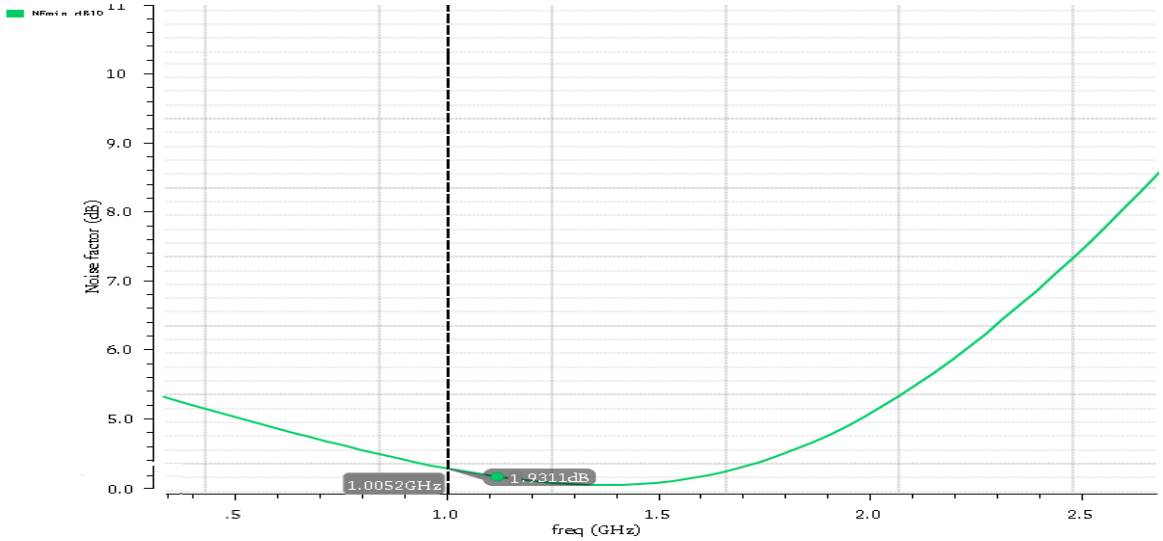

Fig. 10 Simulated Noise Figure (NF) =1.9dB @ 1.04GHz center frequency

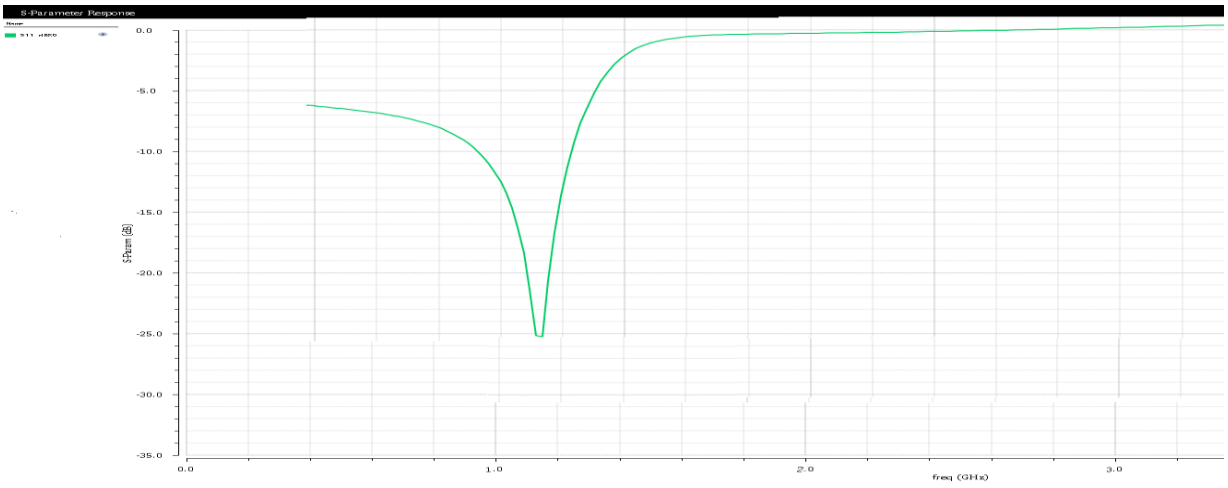

Fig. 11 Simulated input return loss S_{11}= -12.5dB @ 1.04GHz center frequency

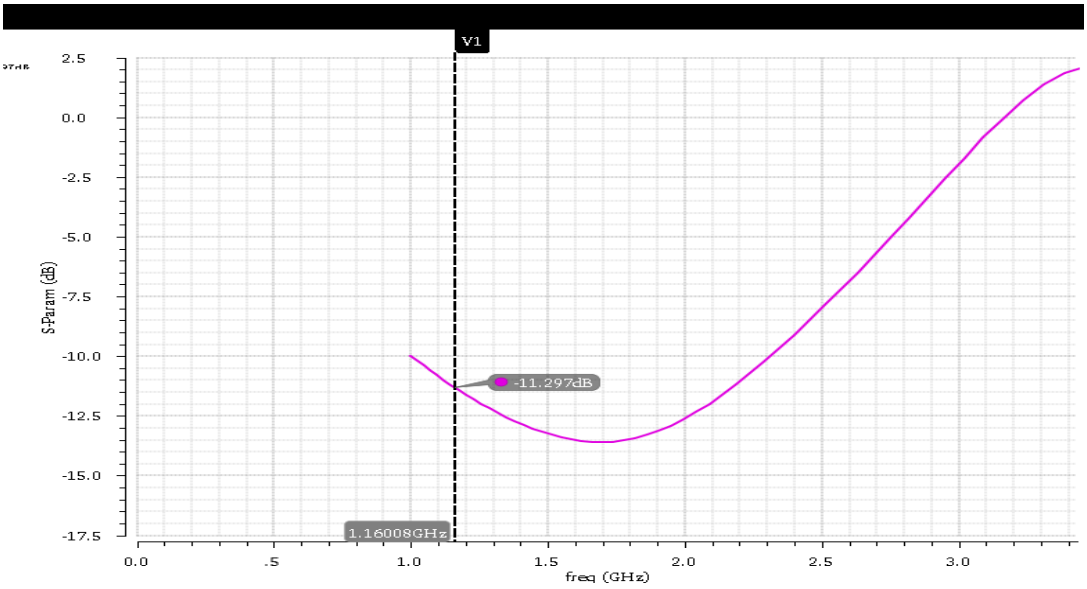

Fig. 12 Simulated output return loss S_{22}= -11.3dB @ 1.16GHz center frequency

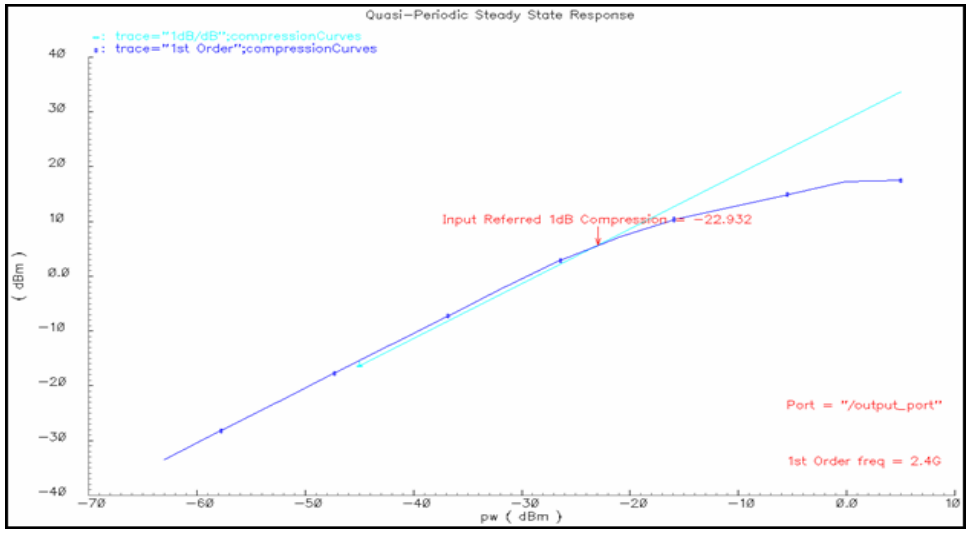

Fig. 13 Simulated 1dB compression point (IP_{1dB})=-22.9dBm

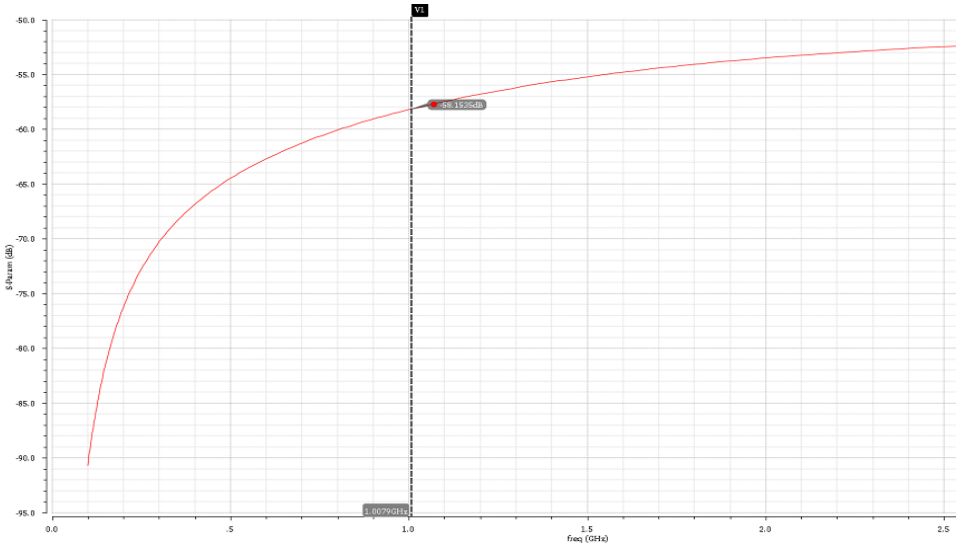

Fig. 14 Simulated S_{12}= -58.15dB @ 1.01GHz center frequency

V. CONCLUSION

This manuscript concludes the proposed LNA approaches two paths in parallel: CS path and CG path. Here CS path is liable for provided adequate gain of 22.5dB, and due to the CG path the perfect input and output impedance matching is 50Ω achieved. In the CG path, the noise involvement can be removed by noise cancellation technique; consequently, on the whole noise figure of 1.9dB is enhanced. The mismatch of phase among the 2 different paths is moreover quantitatively investigated with analyze to its effect on NF and gain. The methodical values agreed to fit with simulated results. Also this LNA provided the 1-dB compression point (IP_{1dB}) as -22.9dBm and the 3rd-order input intercept point (IIP_3) as -4.48dBm and the LNA consumes 6.7mW power with 1.2V power supply.

REFERENCES

1. YIMING YU, KAI KANG, YIMING FAN, CHENXI ZHAO, HUIHUA LIU, YUNQIU WU, YONG-LING BAN, AND WEN-YAN YIN, “Analysis and Design of Inductorless Wideband Low-Noise Amplifier With Noise Cancellation Technique”, IEEE Access, VOLUME 5, 2017, PP: 9389-9397.
2. R. Van Kranenburg, E. Anzelmo, A. Bassi, D. Caprio, S. Dodson, M. Ratto, "The Internet of Things, " 1 Berlin Symposium on Internet and Society, Berlin, Germany, October 25-28, 2011.
3. Marcelo De Souza and André Mariano, “Reconfigurable Inductorless Wideband CMOS LNA for Wireless Communications” IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS–I: REGULAR PAPERS, VOL. 64, No. 3, pp: 675-685, MARCH 2017.
4. F. Belmas, F. Hameau, and J.-M. Fournier, ``A low power inductorless LNA with double G*m* enhancement in 130 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 47, no. 5, pp. 1094_1103, May 2012.
5. E. A. Sobhy, A. A. Helmy, S. Hoyos, K. Entesari, E. Sanchez-Sinencio, ``A 2.8-mW sub-2-dB noise-_gure inductorless wideband CMOS LNA employing multiple feedback," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 12, pp. 3154_3161, Dec. 2011.
6. P. Harrop and R. Das, "Wireless Sensor Networks 2011-2021: The new market for Ubiquitous Sensor Networks (USN), " www.IDTechEx.com.
7. Vikram Singh, Sandeep Kumar Arya and Manoj Kumar, “Gm-boosted current-reuse inductive-peaking common source LNA for 3.1–10.6 GHz UWB wireless applications in 32 nm CMOS”, Analog Integrated Circuits and Signal Processing, Springer Science+Business Media, LLC, part of Springer Nature 2018, https://doi.org/10.1007/s10470-018-1290-6.(0123456789().,-volV)(0123456789().,-volV)
8. Fanzhen Meng; Hong Liu; Ke Zhang; Kai Kang; Tong Tian, “ A 780-MHz low power transceiver for wireless nodes applications in Internet of Things” 2013 IEEE 56th International Midwest Symposium on Circuits and Systems (MWSCAS) 4-7 Aug. 2013
9. François Belmas, Frédéric Hameau, and Jean-Michel Fournier “A Low Power Inductorless LNA With Double Gm Enhancement in 130 nm CMOS” in IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 47, NO. 5, MAY 2012,pp 1094-1103.
10. T. Taris, A. Mabrouki, H. Kraimia, Y. Deval, and J.-B. Begueret, “Reconfigurable ultra low power LNA for 2.4 GHz wireless sensor networks,” in Proc. IEEE ICECS, Dec. 2010, pp. 74–77.
11. Mahesh Mudavath and K. HariKishore “CMOS Front-End of Low Noise Amplifier for GPS and GSM wireless Applications” in International Journal of Engineering and Technology (UAE), 2018, Vol. No. 7(1.5), ISSN:2227-524X, pages 1-6. DOI: 10.14419/ijet.v7i1.5.9069.
12. Mahesh Mudavath, K.HariKishore, “Design of CMOS RF Front-End of Low Noise Amplifier for LTE System Applications” Asian Journal of Information Technology, Medwell Journal, Vol. No. 15, Issue No.20, pp:4040-4047, 2016.
13. John W.M. Rogers, Calvin plett. Radio Frequency Integrated Circuit Design, Artech House, London, ch.7, page.171.
14. Razavi. B, 1999. CMOS technology characterization for analog and RF design IEEE J. Solid State Circuits, 34: 268-276.
15. Razavi. B, 1998. RF Microelectronics Prentice Hall Publisher, New Jersey, USA, Pages.180.
16. Bosco Leung, 2011, “VLSI for Wireless Communications”, second edition, Springer, Page(s):62-162.
17. T.Lee, The Design of CMOS Radio Frequency circuits, second edition ed. Prentice Hall, 2003.
18. Jan Magne Tjensvold, “Comparison of the IEEE 802.11, 802.15.1, 802.15.4 and 802.15.6 wireless standards.”
19. Mahesh Mudavath and K. HariKishore “Design of RF Front-End CMOS Cascade CS Low Noise Amplifier on 65nm Technology Process” in International Journal of Pure and Applied Mathematics, 2017, Vol. No. 115 and Issue No. 7, ISSN:1314-3395, pages 417-422.
20. H. Wang, L. Zhang, and Z. Yu, ``A wideband inductorless LNA with local feedback and noise cancelling for low-power low-voltage applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 8, pp. 1993_2005, Aug. 2010.
21. A. Surendar, K. H. Kishore, M. Kavitha, A. Z. Ibatova, V. Samavatian“Effects of Thermo-Mechanical Fatigue and Low Cycle Fatigue Interaction on Performance of Solder Joints” IEEE Transactions on Device and Materials Reliability, E-ISSN: 1558-2574, Print ISSN: 1530-4388, Page No: 1-7, November-2018.
22. M. Muhamad, N. Soin, H. Ramiah, N.M. Noh, W.K Chong. "Design of CMOS differential LNA at 2.4GHz", 2013 IEEE International Conference of Electron Devices and Solid-state Circuits, 2013
23. Yadlapati, A., Kakarla, H.K. An Advanced AXI Protocol Verification using Verilog HDL (2015) Wulfenia, 22 (4), pp. 307-314.
24. Bindu Bhargavi, K., Hari Kishore, K. Low Power Bist on Memory Interface Logic (2015) International Journal of Applied Engineering Research, 10 (8), pp. 21079-21090.
25. Charan, N.S., Kishore, K.H. Recognization of delay faults in cluster based FPGA using BIST (2016) Indian Journal of Science and Technology, 9 (28).
26. Hari Kishore, K., Aswin Kumar, C.V.R.N., Vijay Srinivas, T., Govardhan, G.V., Pavan Kumar, C.N., Venkatesh, R.V. Design and analysis of high efficient UART on spartan-6 and virtex-7 devices (2015) International Journal of Applied Engineering Research, 10 (9), pp. 23043-23052.
27. Kante, S., Kakarla, H.K., Yadlapati, A. Design and verification of AMBA AHB-lite protocol using Verilog HDL (2016) International Journal of Engineering and Technology, 8 (2), pp. 734-741.
28. Bandlamoodi, S., Hari Kishore, K. An FPGA implementation of phase-locked loop (PLL) with self-healing VCO (2015) International Journal of Applied Engineering Research, 10 (14), pp. 34137-34139.
29. Murali, A., Hari Kishore, K., Rama Krishna, C.P., Kumar, S., Trinadha Rao, A. Integrating the reconfigurable devices using slow-changing key technique to achieve high performance (2017) Proceedings - 7th IEEE International Advanced Computing Conference, IACC 2017, art. no. 7976849, pp. 530-534.
30. A. Surendar, K. H. Kishore, M. Kavitha, A. Z. Ibatova, V. Samavatian “Effects of Thermo-Mechanical Fatigue and Low Cycle Fatigue Interaction on Performance of Solder Joints” IEEE Transactions on Device and Materials Reliability, P-ISSN: 1530-4388, E-ISSN: 1558-2574, Vol No: 18, Issue No: 4, Page No: 606-612, December-2018.
31. N Bala Dastagiri K Hari Kishore “A 14-bit 10kS/s Power Efficient 65nm SAR ADC for Cardiac Implantable Medical Devices” International Journal of Engineering and Technology (UAE), ISSN No: 2227-524X, Vol No: 7, Issue No: 2.8, Page No: 34-39, March 2018.
32. N Bala Dastagiri, Kakarla Hari Kishore "Reduction of Kickback Noise in Latched Comparators for Cardiac IMDs” Indian Journal of Science and Technology, ISSN No: 0974-6846, Vol No.9, Issue No.43, Page: 1-6, November 2016.
33. N Bala Dastagiri, K Hari Kishore "Analysis of Low Power Low Kickback Noise in Dynamic Comparators in Pacemakers” Indian Journal of Science and Technology, ISSN No: 0974-6846, Vol No.9, Issue No.44, page: 1-4, November 2016.
34. Avinash Yadlapati, Hari Kishore Kakarla “Design and Verification of Asynchronous FIFO with Novel Architecture Using Verilog HDL” Journal of Engineering and Applied Sciences, ISSN No: 1816-949X, Vol No: 14, Issue No: 1, Page No: 159-163, January 2019.
35. G. Vijaya Padma, K. Hari Kishore and S. Jaya Sindura, “Controlling the Traffic Interactions with High Mobility and Constant Network Connectivity by Vanets”, Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetic and Telecommunications, Lecture Notes in Electrical Engineering (Publisher: Springer Nature

Singapore Pte Ltd), ISSN No: 1876-1100, E-ISSN: 1876-1119, pp. 593-601, 29th March 2017.

36. K.Sarath Chandra, K Hari Kishore “Physical Design Implementation of High Performance CMOS Dynamic Latch Comparator” Journal of Advanced Research in Dynamical and Control Systems, ISSN No: 1943-023X, Vol No: 10, Special Issue No: 9, Page No: 323-332, June 2018.
37. Mahesh Mudavath and K. HariKishore “Design and Analysis of Receiver Front-End of CMOS cascode common source stage with inductive degeneration Low Noise Amplifier on 65nm technology process ” in Journal of Computational and Theoretical Nanoscience, 2019, Vol. No. 16, ISSN:1546-1955, pages 1-7. DOI: 10.1166/jctn.2019.7942.
38. Meka Bharadwaj, Hari Kishore "Enhanced Launch-Off-Capture Testing Using BIST Designs” Journal of Engineering and Applied Sciences, ISSN No: 1816-949X, Vol No.12, Issue No.3, page: 636-643, April 2017.
39. Dr. Seetaiah Kilaru, Hari Kishore K, Sravani T, Anvesh Chowdary L, Balaji T “Review and Analysis of Promising Technologies with Respect to fifth Generation Networks”, 2014 First International Conference on Networks and Soft Computing,ISSN:978-1-4799-3486-7/14,pp.248-251,August 2014.
40. P Bala Gopal, K Hari Kishore, R.R Kalyan Venkatesh, P Harinath Mandalapu “An FPGA Implementation of On Chip UART Testing with BIST Techniques”, International Journal of Applied Engineering Research, ISSN 0973-4562, Volume 10, Number 14 , pp. 34047-34051, August 2015.