Design and Analysis of Power Efficient Single-Phase Clocking Master Slave Flip-flops for Sequential Circuits

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Abstract: The basic element in sequential circuit design is flip-flop and flip-flops are widely used in memories. This paper outlines the design of Single-Phase Clocking flip-flop using various methods like pass transistor and the transmission gate logic. The main scope of this paper is to design a flip-flop with optimized power. The optimization of power and the reduction in transistor count is achieved by using transmission gates and pass transistor logic. 45nm CMOS based design technology chosen for the implementation technology. The performance metrics of Flip-flop designs were compared with different sequential circuits using transmission gate and pass transistor logic techniques. Pre-layout analysis results indicated that, proposed designs excelled in optimizing the average power. When compared with the other designs, the proposed flip-flop is designed using only 11-transistors and the average power consumption of the proposed flip-flop is bring downed to 108.9 nW. All the designs are simulated and verified with PYXIS tool running on 3.41 GHz processor. These flip-flop designs are best suited for low power and high performance applications.

Keywords: Transmission Gate, Flip-flop, Low Power, Single Phase Clocking (SPC)

I. INTRODUCTION

In digital sequential system designs, the most robust and common technique to build a sequential circuit involves the use of transmission gates and pass transistors. The scaling of supply voltage is critical for low power operation. Certain sequential circuits don't function at reduced supply voltages without scaling of device thresholds. Many solutions are being explored to address the problems, the shaded inverters and transmission gates are implemented in low-threshold devices. In digital sequential system designs, flip-flops are fundamental building blocks and they are used storage elements extensively. Flip-flops employ several modules such as register files, andshift registers, and FIFO. This paper describes the comparison of existing flip-flop design technologies and are designed by using transmission gate and pass transistor based logic.

The comparison of performance of average power and the transistor count is being played a key role in design of proposed flip flop. They adopt intensive pipelining techniques to improve the performance of sequential systems. If flip-flops were not optimized then IC manufacturing industry has several effects. In any digital circuits Very Large Scale Integration (VLSI) technology is used and the objective of the VLSI technology is to increase the density of transistors in single chip area. Optimization of flip-flops in terms of transistor count is very much needed for VLSI circuit designs [6].The flip-flop is highest power consuming component in clock distribution network. The power consumption of flip-flops play critical role and they impact the chip area flip-flop is the most commonly used element, an extensive segment of the most computerized circuits are use clock [1] for their synchronous operation. A conventional Single Edge-activated (SET) flip-flop [7] commonly latches information either on the rising or the trailing edge of the clock cycle. These flip-flops (SET) are generally designed as master slave flip-flops, [3] for example a sequential structure utilizing two latches, called master and slave respectively. The wide use of sequential logic and memory storage systems in modern electronics results in the implementation of low power and high speed design of basic D- Flip-flop [4]. In the new process technology flip-flop designs undergo continuous improvement and evolution of new design methodologies. The new flip-flop design for specific application needs such as high speed, low power and low voltage. However, while the execution increments because of scaling, the power thickness increments considerably every generation due to higher integration density. Moreover, the interest for power-sensitive structure has developed essentially because of the enormous development importable applications. The transmission gate flip flop most widely used flip flop. The design suffers from high capacity clock loading problem, it causes power consumption. Hence the optimized flip flop shows low power consumption the other advantage of the proposed flip flop will achieve power reduction in sequential circuits [2].The organization of the paper described as follows, the related work of various flip-flop designs with their flip designs is presented in section II, section III outlines the design of proposed flip-flop, and various flip-flop designs are described in section IV. Section V describes the simulation results and the paper is concluded in section VI.

II. RELATED WORK

The design proposed designs in [1] abide from the power leakage problem, so to hold off this problem, the design can be optimized by considering out the common terms. For two pull down devices (nMOS), one CK-controlled transistor is shares the two discharging paths. The transistor count is decreased from 28 to 21 and just resto the transistors are directly driven by the clock signal [13].The configuration follows topologically compressed scheme, every one of these transistors aids to more power consumption. The TCFF configuration depends on the following improvement standards. They are, utilize single phase clock, number of clock driven transistors and reduction in density of transistors. In spite the basic improvement in the power, the arranging execution of the TCFF [11] configuration is extended. In particular, the design experiences a more extended setup time in view of two pMOS transistors are connected to VDD directly, and the power consumption is negatively impacted[8].To avoid from this issue the proposed structure of Fig. 1 using Logic Structure Reduction (LRFF), can be considered as an upgrade of the TCFF design in various execution aspects. This configuration is accomplished by different improvement measures. The primary measure is the logic to decrease for a shorter setup time, the second one is circuit improvement for bringing down the power, and the third one is the end of the node drifting case to maintain a strategic distance from the static power leaking issue. The advantage of this logic structure decrease is twofold. It simplifies the circuit for power saving. The circuit schematic application of the two logic structure reduction schemes is presented in Fig. 1. In this structure just 19 transistors are utilized and one single period of the clock is required, and the fan-out for the clock signal is four (one pMOS and three nMOS transistors). The proposed LRFF is completely static and can maintain a impermanent yield node drifting. In spite of the fact that the check signal fan out of the LRFF configuration is one transistor higher than that of the TCFF design. As far as circuit multifaceted nature, the LRFF utilizes minimal number of transistors.

This can be credited to a much improved logic structure and a decreased clock signal stacking of the LRFF plan. The power advantage of the LRFF configuration limited but was still significant as the switching activity decreased. At the point when the probability of information changing decreased to 12.5%, the power savings for the two plans wound up 24% and 7%, separately [9].A logic structure decrease conspire is utilized to lessen the quantity of transistors which intends to diminish the zone for accomplishing high power and delay performance. The advantages of this logic structure reduction schemes are it simplifies the circuit for power saving and other one is low delay. Finally, the performance metrics like delay, power and number of transistors are compared with proposed flip-flop and optimized flip-flop [14].
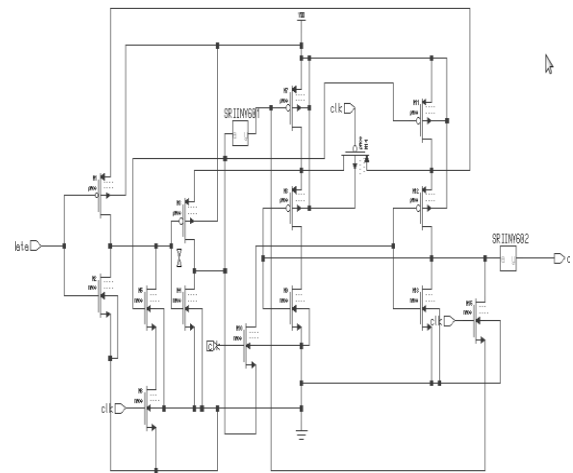

Fig. 1 LRFF (19 – Transistors)

III. WORK PROPOSED

The work proposed is the design of Flip-flop based on the transmission gates and the pass transistor logic. The key objective is to this design is to improve the performance metrics like power and the no. of transistors are used in the design and can be considered as an improvement in various design aspects. Optimization of the mentioned parameters is achieved by various measures. The former is to measure is the voltage drop problem and the latter is simplifying the design for least power consumption and it improves the feedback path. The reduction in density results in the reduction in parasitic capacitances at internal nodes of the flip-flop, this results in improved power dissipation. The feedback path in figure 2 indicates that, some of the drive current is directed in the same path, whereas rest of the drive current is directed off, the path giving rise to internal fan-out within the FF, accordingly the branching effort is given by the following expression

$$b= C_{off\text{-}path}\text{-}C_{on\text{ }-path/}\ C_{on\text{ }-path} \qquad (1)$$

Where, $C_{on\text{-}path}$ is the load capacitance along the path under analysis, while $C_{off\text{-}path}$ is the capacitance of the interconnections which leads to off path. To provide a basis comparison, some flip-flop designs are considered[5],The TGFF is shown in Fig. 2, indicating that it is designed by using two Transmission gate based latches[2]. The design depicted in fig. 2 suffers from High loading problem(number of elements directed through clock), it causes sustained power consumption. To overcome this problem,two optimized flip-flop designs have been proposed. Fig. 3. shows passtransistor logic based master slave D flipflop shows low power consumption. It uses pass transistors which reduce the power consumption. The flipflop have high speed of operation.
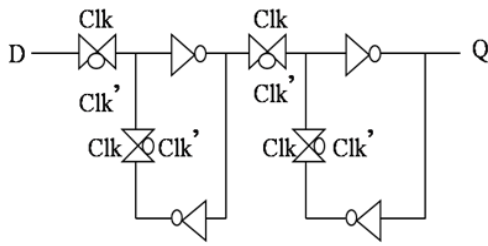
Fig. 2 Transmission Gate Flip-flop

It solves voltage drop problem Which occured in transmission gates. The internal and external nodes have less capacitance, which leads to reduction of power consumption and propagation delay. The optimized flip-flop has improved feedback path compared to Conventional FF designs.
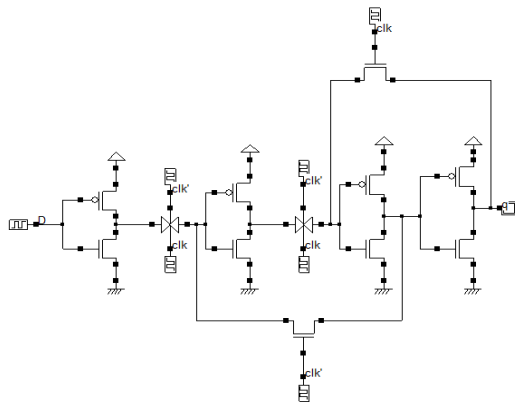
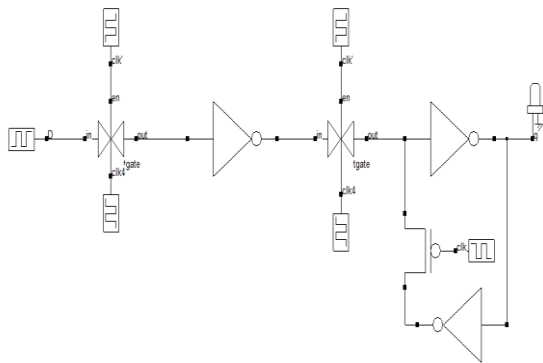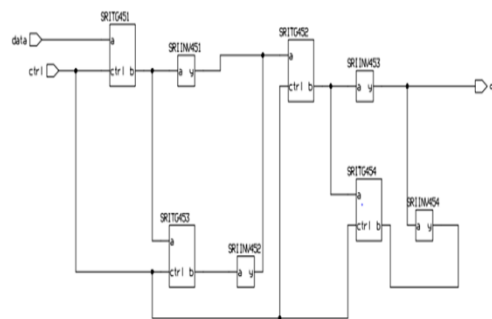

Fig. 3 Pass Transistor logic FF

Fig. 4 Proposed FF

Fig. 4.shows optimized flip-flop which results in less power consumption compared with previous flip-flop designs. It uses transmission gates for both master and slave flip-flops and the number of transistors were bringing down to 11, which means the area, delay and power are optimized [4].As shown in fig. 4. The NMOS output will only a voltage level of $<V_{dd}$when it is at logic high state, power may not be optimized. The transmission gated are utilized in both master and slave design, this reduces the power dissipation. The improved feedback loop is seen in the proposed design, the majority of the traditional static structures utilize two feedback loops one each in the master and the slave. These rise in the parasitic capacitance at the internal flip-flop nodes, prompting higher dynamic power and performance degradation. This results in area overhead because of increase in transistor density. This is a low area

flip- flop and has the smallest power dissipation. Master slave flip-flops generally utilize l ow power systems. In CMOS technology D-FF is implemented with transmission gates. D type flip-flops are popular because they have fewer input signal paths and circuits using them are simpler to design. A transmission gate is formed by parallel connection of an n- channel transistor and p-channel transistor. Transmission gates have symmetric noise margins in either direction of transmission and support bidirectional signal transmission. The optimized FF exhibits better power dissipation. For low supply voltages optimized FF shows the highest delay but as the supply voltage increases its delay improves, while the delay of Proposed FF increases with increment of supply voltage as compared to other flip-flops. Optimized FF has the high delay and lowest power consumption. Optimized FF has only eleven transistors but this flip-flop has the highest delay and low power consumption, So the proposed FF is suited for low power or high performance applications. In the event that there is decrease in the quantity of timed transistors, the clock load capacitance is decreased, prompting low control utilization in the clock circulation network[6]. Hence by transistors, the power dissipation of the proposed structure is decreased.

IV. FLIP-FLOP DESIGNS

A flip-flop shown in fig 6(a) widely used in all real time applications (TGFF) [16]. To overcome the problem of power consumption two FF designs are proposed. Pass transistor based FF and optimized Fifth Fig. 6(b), pass transistor based FF uses fourteen Transistors which reduces the power dissipation. The FF has high speed of operation. It has less capacitance of nodes which reduces the power consumption as well as propagation delay. CMOS pass transistor based logic can result in high-speed and high-density circuits [5]. The transistor count is being reduced and to generate different logic gates, by eliminating extra transistors. Transistors are used as switches to pass logic levels between nodes of circuit, rather than switches connected on to provide voltages. The advantage is that one pass-transistor arrangement is adequate to play out the logic activity, which results in fewer transistors and smaller input loads, especially when NMOS networks are used to solve voltage drop problem.
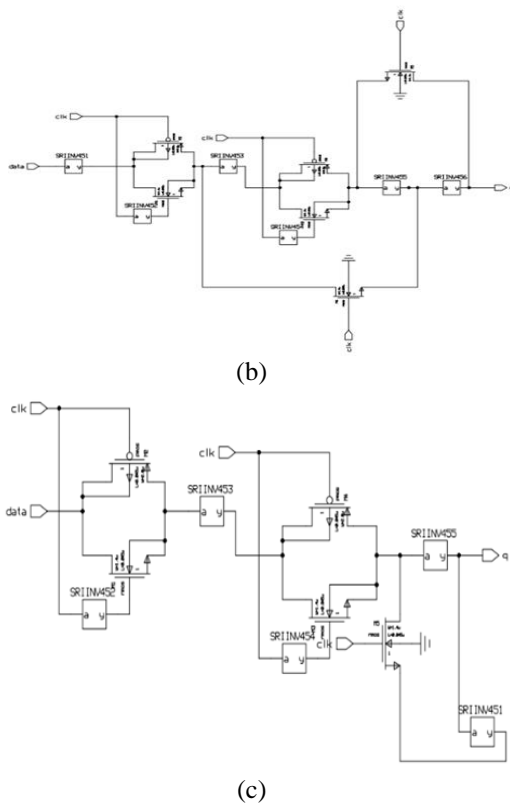

(a)

(b)

(c)

Fig. 6 Master Slave D – Flip-flop designs (a) TGFF (b) PTFF (c) Optimized flip-flop

Fig. 6(c) shows optimized flip-flop uses eleven transistors which reduces the power consumption. One technique to decrease the transistor check is to utilize a NMOS for clock input [9]. This reduces the power dissipation. Most of the conventional static designs utilize two feedback loops one each in the master as well as the slave stage. This builds the complete parasitic capacitance at the inner flip-flop nodes, prompting higher unique power dissipation and decreased execution. This likewise results in absolute chip area overhead because of expanded transistor count [15]. In the event that there is reduction in the density of transistors, the stray capacitance is reduced, prompting effective utilization of clock network [6]. Hence by transistors, the power dissipation of the proposed structure is further decreased. This flip-flop is negative edge activated flip-flop. In the proposed FF when clock level is 'HIGH', master latch is activated and reverse of the information is put away to a between internal node. At the point when clock goes to 'LOW', slave latch moves toward becoming capacity al and produces information at the yield Q.

Rise Time and Fall Time: Rise time is predominantly varied due to stray capacitance and inductance and cause a delay in the circuit and affect the device parameters.

$$V_{out} = V_{out}\left(1 - e^{-t/RC}\right) \qquad (2)$$

The above equation (2) represents parasitic capacitance, trace impedance.
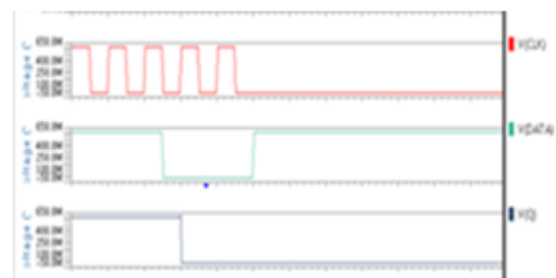
Observations: Rise and fall time is independent of the data signal switching frequency. Rise or fall time can be expanded by including arrangement resistor and parallel capacitor to the each yield phase of the FF (that is stick Q). If rise or fall time can be increased at output stage. The glitches are occurred at that time. Automatically it may

consume more power. Glitches are defined as intermediate values of gates. To avoid glitches the rise and fall time must be low.
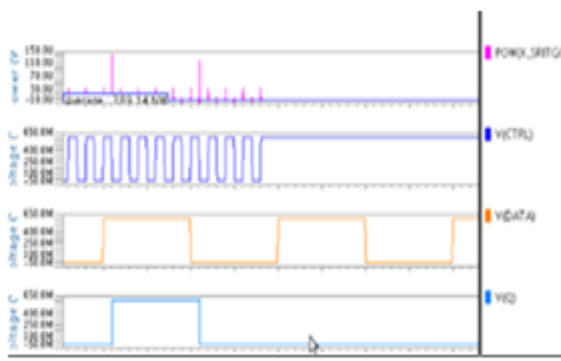
V. RESULT AND DISCUSSION

Fig. 7(a), (b), (c) & (d) represent the power consumption in nW at 0.6V supply voltage for 100 MHz clock frequency. So power dissipation rapidly reduces with reduction in the supply voltage.[15]. These figures show that rise in power with in clock frequency and decrease in supply voltage [8]. The power consumption of synchronizers is compared with master slave D flip-flop and LRFF. The optimized flip-flop consumes low power. Design and comparative analysis of Master slave D flip-flop with different techniques was done [15].Among previous flip-flops the proposed FF shows the lowest power consumption for supply voltage 0.6V and clock frequency 100 MHZ. Increase in clock frequency results in highest power consumption. Low supply voltages FF shows the highest delay but as the supply voltage increases its delay improves of Proposed FF . [14]. Table I indicates the power consumption in nW.at supply voltage 0.6V and 100MHz clock frequency. The previously proposed flip-flop shows lowest power consumption. Proposed FF has some improvement in average power consumption [13].
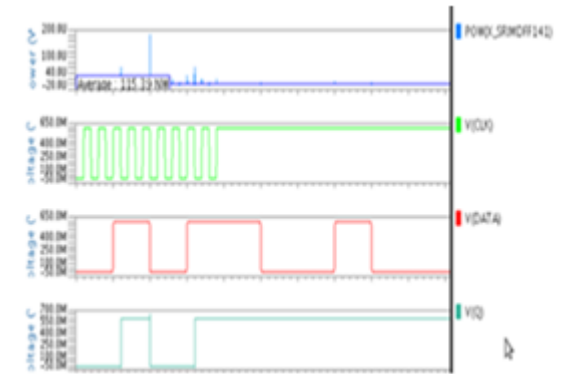
The proposed flip-flops discussed in section V consume least power for 0.6v supply voltage [10].low supply voltages FF shows the highest delay but as the supply voltage increases its delay improves of Proposed FF.There is always a trade-off between power dissipation and propagation delay of a circuit. A flip-flop can be reduced for either high performance or low power, but in this work, the designs are simulated to achieve low power dissipation. The simulation results indicate that the proposed FF has the least average power dissipation among all the designs for supply voltage .For fair comparison, the average power consumption when compared to the previously proposed flip-flop shows lowest power consumption. Proposed FF has some improvement in average power consumption.
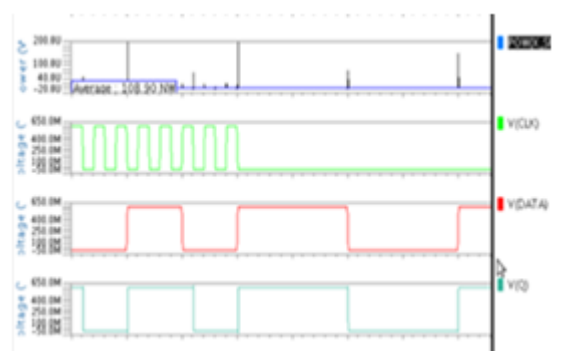

(a)

(b)

(c)

(d)

Fig. 7 Simulation Results of proposed FF designs (a) LRFF (b) TGFF (c) PTFF (d) Proposed FF

Fig.8 provides through analysis of the clock to Q delay under different supply voltages (from 0.6 to 1.0V). The working frequency was lowered to 100 MHz to ensure that all designs function properly in low supply voltage. In the delay analysis the proposed flip-flop shows highest delay.Fig.9 (a) and (b) provides through analysis of power under different supply voltages (0.6 to 1.0V).the proposed flip-flop shows least power consumption when compared to PTFF and TGFF.

The design and analysis of Master Slave DFlip-flopshave been done. Optimized flip-flop shows the lowest power consumption for 0.6V supply voltage and clock frequency at 100 MHz, at this frequency optimized flip-flop shows the better power consumption. Optimized flip-flop failed at 1v. As clock frequency is increased, power consumption of flip-flop increases and near 1 GHz clock frequency flip-flop consumes the highest power.
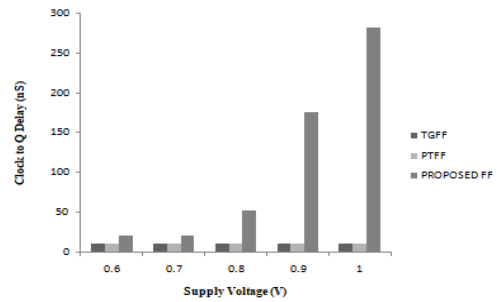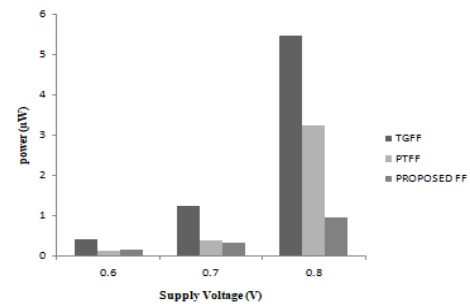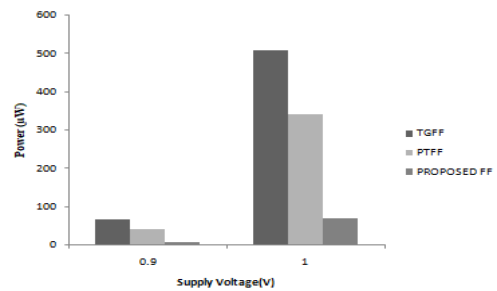

Fig. 8 Performance analysis of various flip-flop designs with respect to supply voltage and clock to Q delay

(a)

(b)

Fig. 9 (a) & (b) Performance analysis of various flip-flop designs with respect to supply voltage and power

VI. CONCLUSION

For low supply voltages power optimized shows the highest delay but as the supply voltage increases its delay improves, while the delay of optimized flip-flop increases with increment of supply voltage as compared to other flip-flops. Optimized FF has the high delay and low power. The proposed flip-flop is compared in terms of its average power consumption, delay and the density of the transistors being used to design, with the existing flip-flop structures. For 0.6V supply voltage and clock frequency at 100MHz the proposed has better power consumption and some improvement in average power consumption. The simulation results states that the proposed FF has the high delay and lowest power consumption than all the existing flip-flop structures. Among all flip-flops compared, the proposed FF is found to be the best energy efficient flip-flop and the second shortest delay. The proposed FF has up to some improvement in average power dissipation, improvement in delays. So, proposed is best suited for low power and high performance applications.

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