Optimization of Power in 8T SRAM Cell by using Transistor Stacking Effect

Saranya L, Aravinth R, Bhuvanesh Priya B, Sai Praveen Kumar S, Santhosh S

Abstract: ***In recent trends, optimization of power is the major challenge in VLSI Technologies. SRAM is a widely used component in cache memories, CPU registers and also in the design of Random Access Memories. Therefore, it is necessary to decrease the power consumption in SRAM. Because of the scaling of transistors, the leakage current plays a necessary role in the power consumption of the device. In this paper, we focus on enhancing the leakage current by using a Transistor stacking method.***

Keywords*: Power optimization, transistor stacking, 8T SRAM, leakage current*

I. INTRODUCTION

The advent of modern technology created handheld devices. In recent times, handheld devices are furthermore reducing in size for portability. However, the reduction in the size of the devices leads to a small battery pack, which forces us to minimize the power consumption of the internal devices for longer battery life. Among the essential power consuming internal devices, the memory device has the highest power dissipation[1]. The primary memory devices of portable devices are CPU registers, cache memories and the random access memory (RAM). SRAM memory cell is suitable for designing primary memory storage devices, due to their higher operation speed. SRAM cell is a one bit storage device which store the bits (0,1) in a cross-coupled inverter. The stored bit is maintained by using internal feedback.

The value is retained as long as the power is applied. The cross coupled-inverters are weak so that the newer data overwrites during the write operation and also strong enough to not modify the data during a read operation. SRAM cell requires lower area per bit than the counterpart DRAM which requires a larger area per bit.

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II. OPERATION OF SRAM

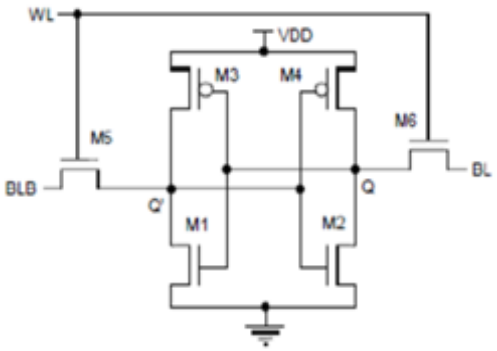

Fig. 1 SRAM Cell

The operation of a basic SRAM is based on the action of cross-coupled inverters.The basic SRAM Cell is shown in Figure 1.

The circuit which is connected to the stored bit is controlled by the word line S. The Bit Line C and Bit Line Cbar carries the data in and out the cell. The cross-coupled inverters form a feedback loop which is similar to a network of two inverters in feedback. The feedback loop stores the data. This forms a single cell which can store a bit of data. An Array of these cells are connected to form a memory array to store the multiple bits.

III. CONVENTIONAL 6T SRAM

A conventional 6T SRAM cell is shown in Figure 2. The Transistors M5 and M6 are access transistors. They provide access to the data which is stored inside the cell. By asserting the Word Line (WL) ON and OFF, the access transistors are controlled.

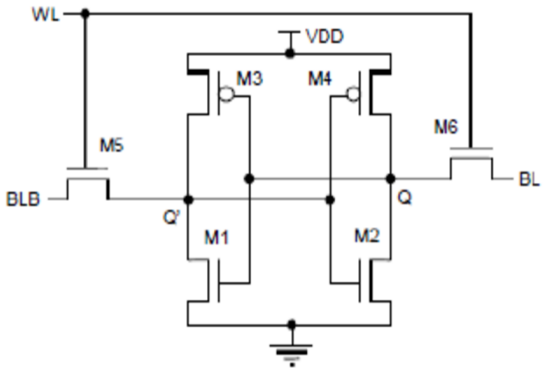

Fig. 2 Conventional 6T SRAM

The transistors M2, M4, M1 and M3 forms the cross-coupled inverter and the feedback loop stores the data. The 6T SRAM cell uses a single port for both the read and write operations. The write operation is performed by previously charging the Bit Lines to corresponding values and asserting the Word Line to 1.

Write '1' Operation: To write bit 1 into the cell, the Bit Line is asserted as 1 and the Bit Bar is asserted as 0. When the word Line is high, the access transistors overwrites the data in the cell.

Write '0' Operation: To write bit 0 into the cell, the Bit Line is asserted 0 and the Bit Bar is asserted 1. When the Word Line is high, the access transistors overwrite the data in the cell.

Read Operation: During reading operation both the bit lines are precharged to high. When the Word Line becomes 1, the Bit lines will be pulled down or remains constant based on the values in the node A and node B.

For eg: When Q = 0 and Qbar = 1, bit 0 is stored inside the cell. The Bit line will be discharged through M5 – M1. For node Q to not flip, the M1 should be stronger than M5, but M5 >> M2. Similarly, when Q = 1 and Qbar = 0, the bit 1 is stored inside the cell. The Bit Bar line will be discharged through M6-M3. For Qbar to not flip, the M3 should be stronger than M6, but M6 >> M4.

IV. CONVENTIONAL 8T SRAM

The conventional 8T SRAM cell is shown in Figure 3. It uses separate ports for write and read operations.

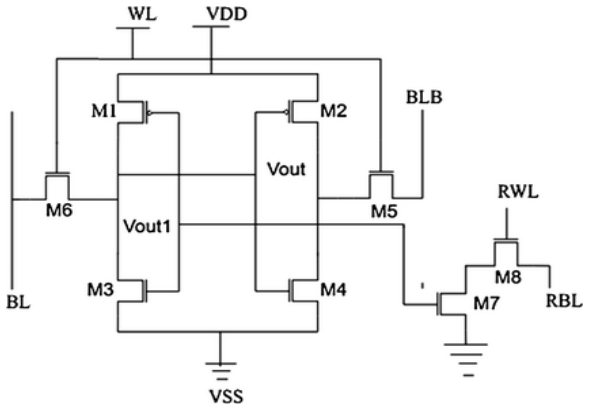

Fig. 3 Conventional 8T SRAM

The transistors M7 and M8 are used for the read operations. The read operation is carried out by using the Read Word Line(RWL). The write operation in the 6T SRAM is similar to the normal write operation. The strength of the transistors is in order

M3 >> M5 >> M1

And also

M4 >> M6 >> M2.

Read Operation: The Read operation is carried out by using the Read Bit Line(RBL). The Read Word Line is charged up to 1 for performing the read Operation. The read operations are as follows:

Read 1 Operation: The QB will be 0 when the value stored inside the cell is 1 and Q = 1. When RWL is high, the transistor M8 will be turned OFF.

V. MODIFIED 8T SRAM

The proposed 8T SRAM cell reduces the leakage current by using the transistor stacking method is shown in Figure 4.[3]. Stacking the transistors leads to an increased threshold voltage which in turn reduces the sub-threshold leakage current. Minimizing the sub-threshold leakage current will reduce the power consumption of the device. The Fig.4 shows the power optimized 8T SRAM cell. The transistors MN6 and MN7 are used to produce the stack effect which in turn reduces the subthreshold leakage current.

The leakage power is highly reduced in the write operation, whereas during the read operation the power used is less than the write operation[2][6].During the write "0" and write "1" operation,the power discharge from any single bit line which is prevented by properly selecting the control line WS(Word Select), by turning OFF either the transistor MN6 or MN7. The timely assertion of WS is necessary for maintaining the functionality of the SRAM cell.

Write 1 mode: The node BL must be set to "0" and the WL is asserted to high.

Case I:Since the nodes B and BL are at zero potential writing cell state from 1 to 1 will not be possible.

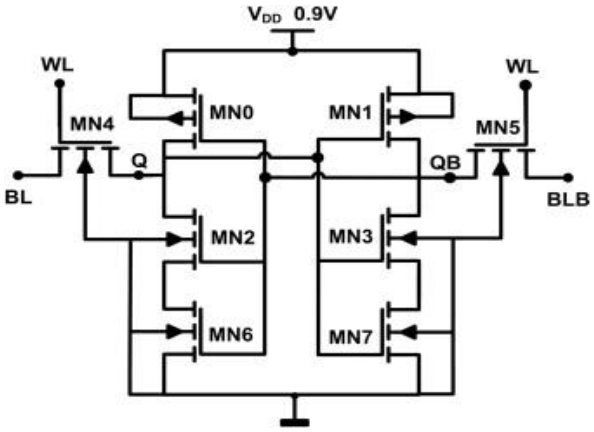

Fig. 4 Power Optimized 8T SRAM

Case II: Writing the cell state from "0" to one (0-1). By setting WS as high before asserting WL, it is easy to flip the cell states from 0 to 1 in low power SRAM cell. It shows that the discharging path which makes Q=0 and QB as 1 is through the transistors MN2 and MN6.

Write 0 mode: The WL is made "0" and the node BL must be set to "1".

Case I: Since BL is intially high writing cell state from 0 to 0 is not posiible.

Case II: By writing cell state from 1 to 0 8T SRAM cell can be easily performed by setting WS low, It makes BL bar disconnected. The desired write pattern can be performed by setting WL high. It shows the Discharging path which makes Q=1 and QB is 0.

The WS signal is used to ensure the correct operation in our low power circuit.The transition from 1-0 and 0-1 can also be easily allowed by selecting the proper value of WS before asserting WL.

The pull-down transistors MN6 and MN7 reduces the subthreshold current, which is flowing in the circuit when the transistor is in Cut Off region[5]. This leakage current is dependent on Threshold Voltage. As the threshold voltage decreases, the subthreshold current increases.

VI. TRANSISTOR STACKING EFFECT

The leakage current in the single off transistor is higher than the two off transistors stacked together. This is due to the increased Vt, threshold voltage[6].

The leakage of transistors depends on the number of transistors and the input pattern[5]. The threshold voltage is increased when the Vbs of the lower transistor is negative. This is due to the negative gate-source voltage in the upper transistor. The reduction in the leakage current leads to the lowering of the drain-source voltage.

VII. SINGLE CELL POWER ANALYSIS

The power analysis is performed using the Tanner EDA tool and t-spice tool. The power consumption across each SRAM's varies significantly.

The power analysis of each SRAM shows different power consumption according to the Vdd provided [7]. Obviously, the power consumption in the 6T SRAM is higher than the power consumption in the 8T SRAM.

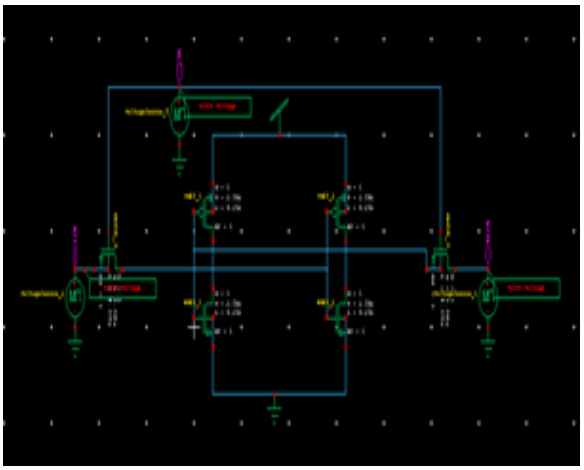

Fig. 5 Conventional 6T SRAM

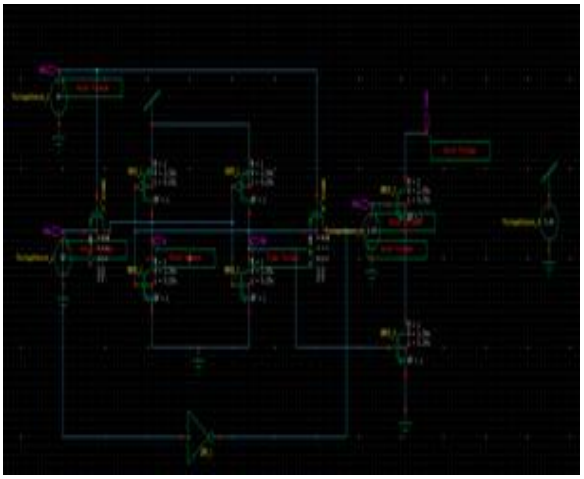

Fig. 6 Conventional 8T SRAM

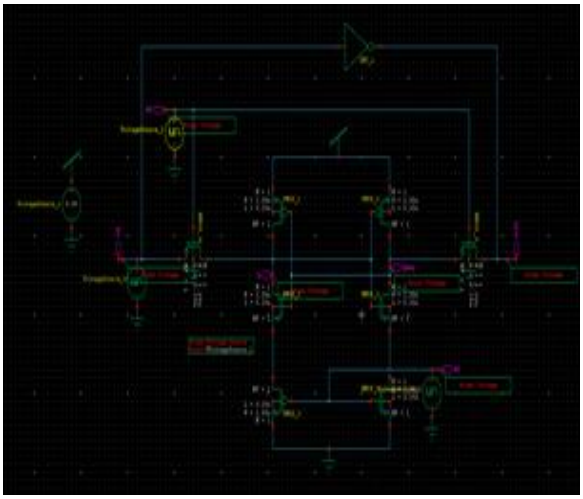

Fig. 7 Power Optimized 8T SRAM

The output waveform for the SRAM cells is produced as follows

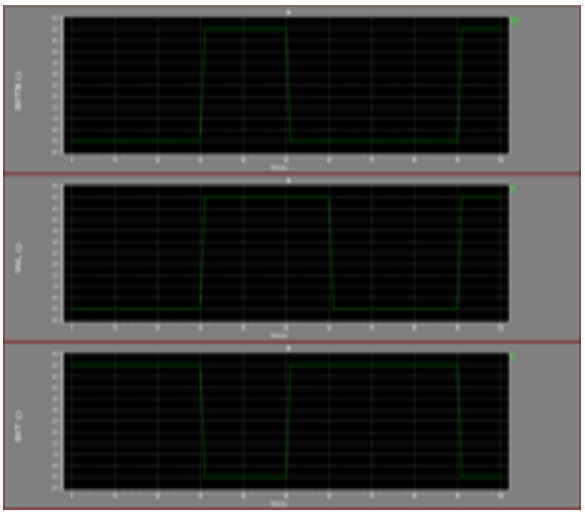

Fig. 8 Output of Conventional 6T SRAM

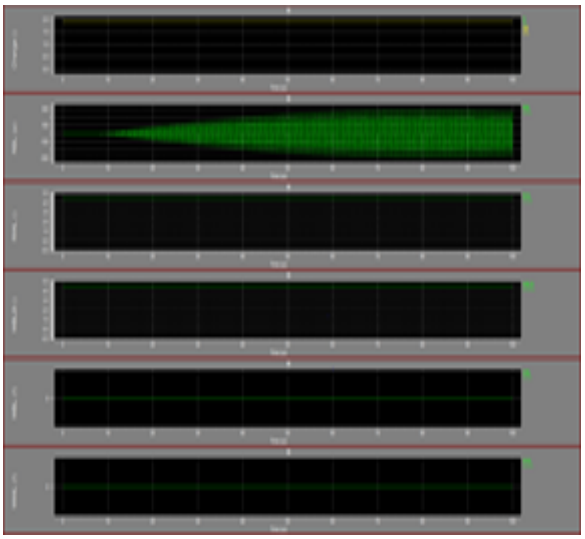

Fig. 9 Output of Conventional 8T SRAM

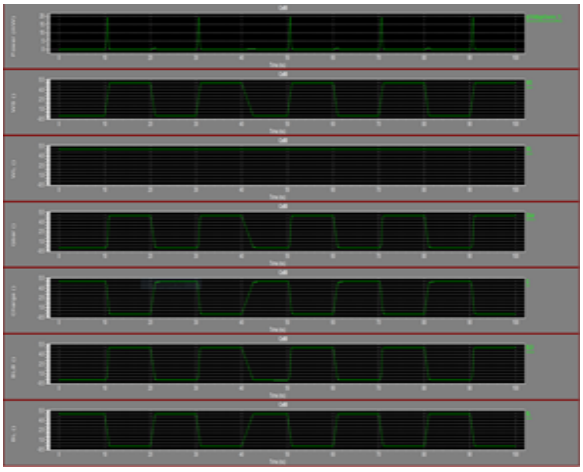

Fig. 11 Power Output waveform at Vdd = 5V

VIII. POWER COMPARISON IN SRAM CELLS

The power comparison in SRAM Cells is shown in Table 1.

Table. 1 Power Comparison in SRAM Cells

SRAM Cell	Power Comparison (Vdd = 5v)
6T SRAM	217Uw
8T SRAM	30Uw
Transistor Stacked 8T SRAM	2.9Nw

IX. CONCLUSION

The power consumption of the 6T, 8T and optimized 8T SRAM has been analyzed. The 6T SRAM cell's high power consumption is high due to the sub-threshold leakage current. The efforts to reduce the subthreshold leakage current in the 8T SRAM is successfully executed. Also, it is inferred that the stacking of transistors is helpful in reducing the leakage current, due to the increase in threshold voltage.

REFERENCES

1. Kaushik Roy, Saibal Mukhopadhyay and Hamid Mahmoodi-Meimand "Leakage Current Mechanisms and Leakage Reduction Techniques in Deep-Submicrometer CMOS Circuits" proceedings of the IEEE, Vol.91, No. 2, February 2003.
2. A. Goel, R.K. Sharma, A.K. Gupta "Process variations aware area efficient negative bit line voltage scheme for improving writeability of SRAM in nanometer technologies" IET Circuits Devices Syst., 2012, Vol. 6, Iss. 1, pp. 45–51.
3. C. Ik Joon et al., "A 32 kb 10T subthreshold SRAM array with bit interleaving and differential read scheme in 90 nm CMOS," IEEE J. Solid-State Circuits,vol.44,no.2,pp.650– 658,Feb.2009.
4. L. Wang, J.H. Wang, Z.Z. Yang, L.G. Hou, N. Gong: A Low Power CMOS Technology Compatible Non-volatile SRAM Cell. IEEE 12th International Conference on Solid-State and Integrated Circuit Technology (ICSICT), pp. 1-3, (2014)
5. P.Raikwal, V. Neema, A. Verma: High-Speed 8T SRAM Cell Design with Improved Read Stability at 180nm Technology. IEEE 12th International Conference on Electronics, Communication and Aerospace Technology, vol44, no.2 pp.748-754, Oct -17.
6. Akshay Bhaskar: Design and Analysis of Low Power SRAM Cells. IEEE 12th International Conference on Innovations in Power and Advanced Computing Technologies. Vol. 121, No.2 I-PACT2017.
7. C.B. Kushwah, and S.K. Vishvakarma: "A Sub-threshold Eight Transistor(8T) SRAM Cell Design for Stability Improvement." IEE 2014