Power Optimization in 10T Full Adder for 4 Bit Array Multiplier

Saranya L, Aarsha Nath, Kavitha M, Karthika K

Abstract: A 10T full adder is a low power consumption circuit. It is an eminent circuit with minimum transistor count. The modified CMOS 10T full adder is designed based on low power delay product and it is implemented in array multiplier. Array Multiplier is a circuit used to multiply two four bit binary numbers. When a multiplicand is multiplied by an array multiplier it generates a partial product and they are shifted according to their bits and then added. It reduces the number of partial products generated while multiplying the values. The modified CMOS 10T full adder circuit increases the performance of the multiplier. To analyze the performance of modified adder, CMOS 10T adder is simulated using tanner EDA tools with 130 nm technology.

Keywords: Adder, Array multiplier, delay, partial products.

I. INTRODUCTION

The fundamental blocks of any arithmetic circuit is the adder. The reduction in power or delay leads to improved performance of the circuit with optimal power saving [9]. The power of the system can be widely optimized by decreasing the power consumption in adder. Several researchers had designed low power adder techniques using minimum number of transistors in various logics design [3]. The adder consists of three inputs X, Y, Zin and the outputs sum and carries respectively. The 10T full adder consumes low power with minimum area. To produce a full swing output using minimum number of transistor with low power consumption without affecting the performance is very hard. The modified 10T full adder circuit optimizes the power, and also results in low power degradation.

In this paper, a design of array multiplier using full adders, half adders, AND gates and transistors is proposed. Multiplication is the major root function used in arithmetic logic operation [5].

The main goal of a good multiplier is to offer a physically firm. It requires many hardware resources and action time than addition and subtraction. There are three types of multipliers. They are array multiplier, sequential multiplier and booth multiplier. Array multiplier is a basic model and fast.

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The advantage of array multiplier when compared to other multipliers is that, it has a well organised formation [2]. The Sequential multiplier carries a copy of partial products i.e. if a new partial is produced it is added to old products.

The flip-flop is used in sequential multiplier which is a memory element to store 1 bit of information. Booth multiplier is optimized multiplier and it is generally faster than sequential multiplier. Using booth multiplier we can reduce the number of partial products generated during multiplication. To make the process fast booth multiplier undergoes many steps of multiplication at the same time [2]. This is the major problem in other multipliers when compared to array multiplier. The modified design is done by using 130nm technology to meet the objective of our design. The low power consumption is achieved by reducing the size of transistors.

II. 14T CMOS FULLADDER DESIGN

In 10T full adder circuit, power consumption and area utilization are the major problems. The 10T full adder circuit consumes high power due to small load capacitance. Comparing CMOS 14Tfull adder with the modified CMOS 10T full adder circuits, 14T full adder is efficient in power than 10T full adder. By reducing the number of transistors, 10T full adder is designed more efficiently with low power consumption. The 14T full adder circuit gives a new stable power efficient 10T full adder circuit. The reduction in number of transistors in the conventional full adder's results in the development of 10T full adder [9].The modified 10T full adder assures low power consumption when compared with other full adder circuits. These adders results in higher performance in application with multipliers. The modified design is suitable for energy constraint applications like portable and wearable devices where ultralow power consumption is the primary design goal.

III. 10T CMOS FULLADDER DESIGN

In 10T full adder design, there exists degradation in output. Therefore, it becomes a necessity to produce a full output swing with ultralow power consumption. The modified design, 10T 1-bit full adder is shown in Figure 1. It consists of sum and the carry blocks [3] .The 10T Full Adder has a pair of XOR gates and a multiplexer.

The Sum operation is based on pair of XOR gates. A, B are the inputs to the XOR gate which produces X as the output.

The resulted output X is given as input to the second XOR gate consisting of four MOSFETs with input C [7]. This XOR gate produces Y as output which is the output of Sum. Carry block is formed from the selector circuit that has two MOSFETs. The selection line of carry block is the output for the first XOR gate, which is the carry block output (ZOUT) that depends on "X Y". If "A B" = "0", then carry block output is "Z". If "A B" = "1", the result is "ZCOUT".

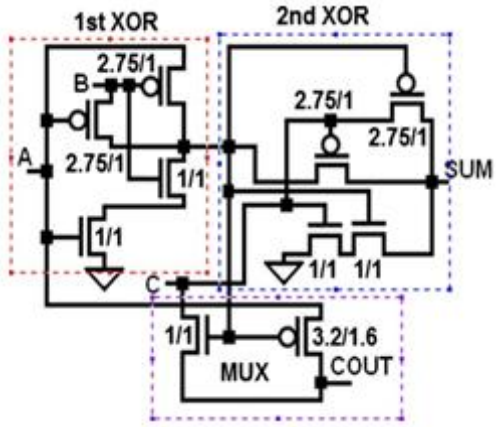

Fig. 1 10T 1 Bit Full Adder

The CMOS 10T full adder shows optimized results in power. The W/L ratio for all nMOS transistors is 1/1 and for pMOS transistors is 2.5/1 respectively. The transient simulation shows that the power consumed by the circuit is limited to 38.4 nW at a supply voltage of 1 V.

IV. POWER DELAY

Power delay can be obtained from the product of power dissipation and propagation delay. It can be estimated from carry input to carry output for every circuit [7]. The power delay in 10T full adder is large because of multiple levels in the design. A 4T XOR gate is used to eliminate the power delay problem and hence it increases the speed and also reduces the power consumption by using minimum number of transistors. The Power Delay versus Supply Power is shown in Figure 2

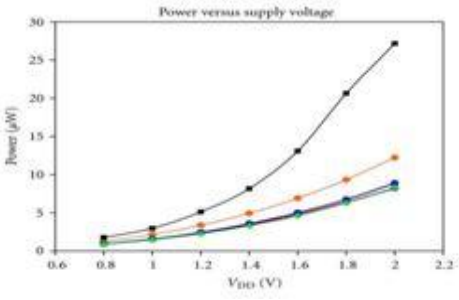

Fig. 2 Power Delay versus Supply Power

V. ARRAY MULTIPLIER

The Array multiplier uses combinational multiplier circuit [4]. Initially let us consider a normal multiplication. For example assume 1011 and 1101 as two inputs which are non signed numbers .The value of 1011 is 11 and 1101 is 13.While Multiplying 11 and 13 we get 143, where 11 is the multiplicand and 13 is multiplier .consider the first bit of multiplier and perform the multiplication and similarly carry the same process for second, third, fourth bit of multiplier. Now four rows are created which are called as partial products. After obtaining the partial products, sum all the partial product values and convert the answer into decimal. On simplification, the resultant output is 143. So, it is clear that the value obtained by binary multiplication is the same as which results from normal multiplication. The same process of multiplication is now implemented in the array multiplier circuit. A simple Binary multiplication is shown in Figure 3.

```
  1 1 0 1  (1 3)
x 1 0 1 1  (1 1)
-----------------
      1 0 1 1
+   0 0 0 0
    1 0 1 1
  1 0 1 1
-----------------
1 0 0 0 1 1 1 1 (1 4 3)
```

Fig. 3 Binary Multiplier

VI. WORKING OF ARRAY MULTIPLIER

The first bit and second bit of multiplier is multiplied with the multiplicands respectively. The sum of the multiplicants produces the partial sum [4]. Consider the third bit of multiplier and perform the multiplication. The partial products are added with the previous partial sum .Similarly perform the same process for the fourth bit of the multiplier.

As a result we get 10001111 as the answer. Convert these values into decimal and the values obtained will be same as normal binary multiplication. The basic block diagram for Array multiplier is shown in Figure4. Comparing with the normal binary multiplication, these multiplications are difficult.

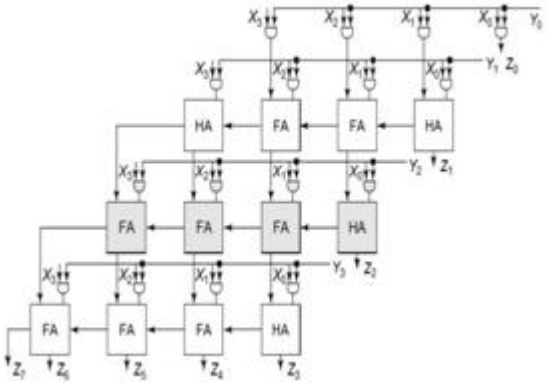

Fig. 4 Block Diagram of Array Multiplier

The multiplicands of AND gates are denoted as a0, a1, a2, a3 .The first and second bit of multiplier is m0 and m1 respectively. The full adders are used to add the two partial products. The half adders are not used because, while summing the partial products, carry occurs and it is propagated to the next level and there will be inclusion of third digit.

The half adders are used only at the initial stage and the rest of the stages uses full adder design. The schematic diagram of array multiplier is shown in the figure 5. Here aj is one of the multiplicand and similarly mi is the multiplier. The AND gate is used to multiply the multiplicand, multiplier (aj, mi).

The carry in is used to denote carry n number of blocks are required to complete the process and it depends on the full adder, AND gate. The time complexity of the circuit with respective number of gate delays depends on path length.

VII. RESULTS AND DISCUSSIONS

In the given waveform of modified 10T full adder, the relationship between the inputs A, B and C and the outputs SUM and COUT are in equation given below,

SUM= A ⊕ B ⊕ C

COUT= AB + C (A ⊕ B)

These output results can be expressed in various logic expressions. In the given Figure 7, A, B, C is considered as inputs. Carry and sum are the outputs. The three input values in A, B and C, i.e., 01010101(85), 00110011(51) and 00001111(15). In the output waveform if the voltage is above 3.5v then it is considered as one. Power consumption of the full adder circuit will be reduced.

A. Schematic Diagram of Modified CMOS 10tfull Adder

The schematic diagram for Modified 10T Full Adder is shown in Figure 5.

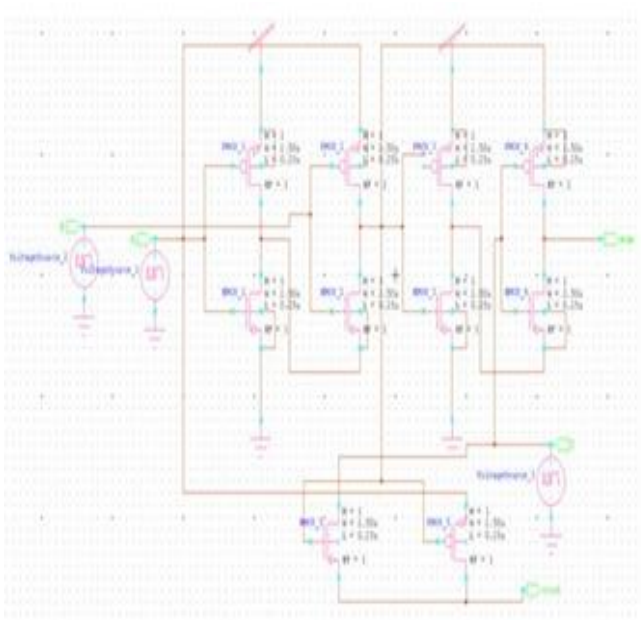

Fig. 5 Schematic diagram of CMOS 10T Full adder

B. Output Waveform of Modified CMOS 10tfull Adder

The output waveform of modified CMOS 10T Full Adder is shown in Figure 6.

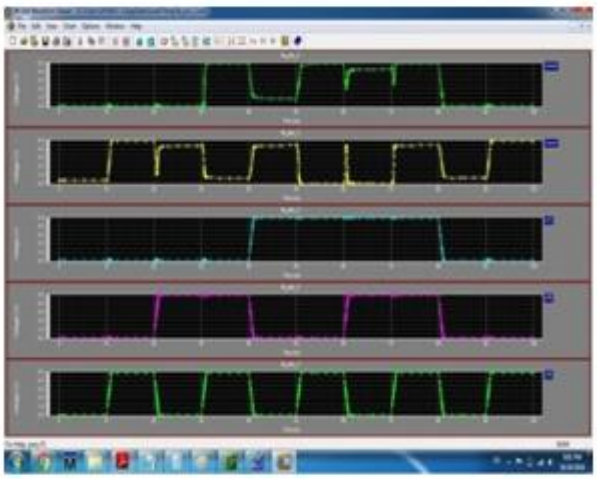

Fig. 6 Simulation of 10T full adder

C. Schematic Diagram of Modified CMOS 10tfull Adder in 4 Bit Array Multiplier

The four bit array multiplier is implemented which uses two inputs i.e., multiplicands and multipliers whose input is 1011(11) and 1101(13) and they are multiplied by using array multiplication method. In the given Figure 8, micro volts and mill volts are considered as zero and the voltage above 3.5v is considered as one. The final result of the waveform is obtained as 10001111(143).

The proposed 4-bit array multiplier is validated by simulating using Tanner tool. Simulation waveform of array multiplier using proposed 10T full adder using 4-bits is shown in the Figure 7. Simulation results show an average power reduction, minimum area is obtained when compared to the existing designs.

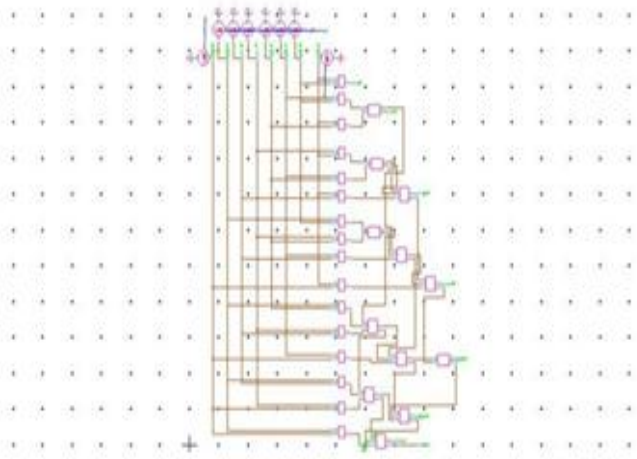

Fig. 7 Schematic Diagram of Array Multiplier

D. Output Waveform of Modified CMOS 10tfull Adder in Array Multiplier

The output waveform of modified CMOS 10T Full Adder is implemented in 4 bit Array multiplier shown in Figure 8.

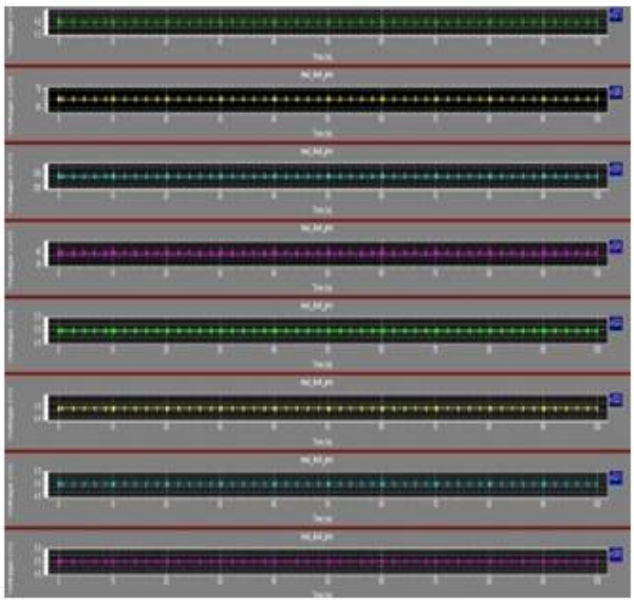

Fig. 8 Output Waveform of 4 bit Array Multiplier

VIII. POWER COMPARISON IN FULL ADDER CIRCUITS

The optimum supply voltage of 145 mV helps to obtain minimum power consumption from the proposed design. It consumes less power when compared to that of the conventional 1-bit full adder and it is shown in the table1.

Table. 1 Power Comparison Table of Adder Circuit

S.no	Parameter	14T Adder	10T Adder
1.	Technology	130 nm	130 nm
2.	Supply	1 V	1 V
3.	Power	78.21 nW	38.4 nW

IX. CONCLUSION

In this paper, the proposed full adder results in the improvement in power reduction that is obtained by 130nm technology. The 10T full adder consumes low power when compared to the existing designs. The Full adder circuit is implemented in array multiplier which can be used in real time applications.

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