Optimization of Power and Area in Hybrid Radix Encoding Signed Multipliers

Saranya.L, Gurusandar.M, PradeepKumar.K, Balaji.S, Uthaya kumar.P

Abstract: ***The power optimization has become a great concern due to the increased usage of multimedia devices. The Design alternative is formed by the inexact computing the exploits the error occurrence in various applications and this makes the circuits to reduce energy consumption with small correctness loss. In this paper, we proposed a Hybrid radix Encoding Signed Multipliers that encodes the most significant bits with the accurate radix-4 encoding and the least significant bits with radix-4096. The approximation of radix is performed by rounding the higher radix values to their nearest power of two. Compare with radix- 4 multiplier, the proposed multipliers consumes less energy and the area is reduced. The proposed multipliers in Radix-4096 operations are compared with new incorrect multipliers, and the obtained results are underperforming them in energy consumption. The proposed Hybrid radix Encoding Signed Multiplier is simulated using ModelSim SE6.3f.***

Keywords: Radix, Inexact multipliers, Gaussian distribution, ModelSim.

I. INTRODUCTION

Multipliers are usually used in arithmetic units of microprocessors, multimedia and digital signal processors. High performance and the reduction of power in multipliers are in demand for embedded systems. Nowadays, it is very hard to increase the performance of the multipliers and also to reduce the power utilization under the condition of full accuracy. However, the requirements of high accuracy and exactness are not so strict for many applications related to human view, such as multimedia, digital signal processing and machine learning. High accuracy and exactness in the operations of digital logic circuits are related to accuracy of information processing, performance and power consumption [2]. This design principle is known as near or inexact computing. The hybrid radix-4096 multiplier uses a combination of Radix-4 and Radix-4096 which results in inexact multiplier.

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Multipliers are the main sources of power consumption in the generation of the partial products in the RADIX. Multipliers based on Wallace decrease tree provide an area-efficient strategy for high speed multiplication. The adder circuit is used as a main module in the multiplier circuits. In this paper, the proposed technique deals with the optimized area of the Wallace tree.

A Wallace tree multiplier is a fast multiplier, which utilizes full and half adder in the decrease stage. The range and power of XOR-XNOR gates and MUX are effective. The proposed method Wallace tree multiplier is far improved when compare to traditional method.

Digital Signal Processing (DSP) is the numerical direction of signals, usually to measure, filter, produce or reduce from analog signal into a digital signal. The digital signals are used to represent these signals as separate time, part frequency, or other separate domain signals in the form of symbols or numbers to allow the digital signal processing.

II. INEXACT MULTIPLIERS

The Booth encoding technique is commonly used in signed multipliers. It performs fast multiplication operation, but still the number of the partial products is not reduced in many of the things. The partial product [3] generation is a technique which is used for designing an approximate multiplication by producing and neglecting some of the partial products based on the method of Booth encoding. An approximate radix-8 booth multiplier uses an approximate adder for producing Radix-k terms, and combining the technique with the truncation method. Recently, approximate modified Booth encoder was developed by modifying its Karnaugh Map, and combining them with an approximate multiplier. The below table 1and 2 shows the positive and negative partial product values respectively for the corresponding Radix.

Table. 1 Positive Partial product per Radix encoding

RADIX ENCODING	PARTIAL PRODUCT
Radix-4	0,+A,+2A
Radix-64	0,+4A,+8A,16A,+32A
Radix-256	0,+16A,+32,+64,+128A
Radix-1024	0,+64A,+128A,+256A,+512A
Radix-4096	0,+256A,+512A,+1024A,+2048 A

Table. 2 Negative Partial product per Radix encoding

RADIX ENCODING	PARTIAL PRODUCT
Radix-4	0,-A,-2A
Radix-64	0,-4A,-8A,-16A,-32A
Radix-256	0,-16A,-32,-64,-128A
Radix-1024	0,-64A,-128A,-256A,-512A
Radix-4096	0,-256A,-512A,-1024A,-2048A

The Approximation Radix 2^K encoding logic is shown in Table 3. It presents the Radix Encoding Technique for 16-bit signed numbers which is used in Radix-4, Radix -64, Radix -256, Radix -1024.

Table. 3 Approximate Radix 2^K Encoding

$R2^k$ Digit		Output				
$y_0^{R2^k}$	$\hat{y}_0^{R2^k}$	$sign$	$\times 2^{k-1}$	$\times 2^{k-2}$	$\times 2^{k-3}$	$\times 2^{k-4}$
$[0, 2^{k-5})$	0	0	0	0	0	0
$[2^{k-5}, 2^{k-4}+2^{k-5})$	2^{k-4}	0	0	0	0	1
$[2^{k-4}+2^{k-5}, 2^{k-3}+2^{k-4})$	2^{k-3}	0	0	0	1	0
$[2^{k-3}+2^{k-4}, 2^{k-2}+2^{k-3})$	2^{k-2}	0	0	1	0	0
$[2^{k-2}+2^{k-3}, 2^{k-1})$	2^{k-1}	0	1	0	0	0
$[-2^{k-1}, -2^{k-2}-2^{k-3})$	-2^{k-1}	1	1	0	0	0
$[-2^{k-2}-2^{k-3}, -2^{k-3}-2^{k-4})$	-2^{k-2}	1	0	1	0	0
$[-2^{k-3}-2^{k-4}, -2^{k-4}-2^{k-5})$	-2^{k-3}	1	0	0	1	0
$[-2^{k-4}-2^{k-5}, -2^{k-5})$	-2^{k-4}	1	0	0	0	1
$[-2^{k-5}, 0)$	0	1	0	0	0	0

III. PARTIAL PRODUCT GENERATORS (PPG)

An under-designed 16×16 multiplier using inaccurate 2 × 2 Partial Product Generators (PPG) is designed. Each PPG has fewer transistors compared with the accurate 2×2, reducing both dynamic and leakage energy at the cost of some accuracy loss.

A Booth multiplier algorithm uses two binary numbers which are multiplied to find the multiplication factor (2^K).There are many arithmetic calculations used for the execution of the results in digital multiplier. Many of the different methods are included for the computation and the summing of the partial products together.

IV. TRANSFORMATION TECHNIQUE IN GENERATION OF PARTIAL PRODUCTS

Fast Fourier Transform (FFT) and Discrete Fourier Transforms (DFT) are used for generating partial products. A fast Fourier transform (FFT) [1] is an algorithmic transform that computes the Discrete Fourier Transform (DFT) of a series. The inverse Discrete Fourier Transform (IDFT) converts a signal from its original domain in to frequency domain and vice versa. The DFT is obtained by decomposing the sequence into different frequencies. This operation is useful in the various forms of RADIX. As a result, it is used to find the partial products for radix. In the presence of any round off error, many Fast Fourier Transform algorithms are used which are more accurate than evaluating the Discrete Fourier Transform definition directly.

The designer will choose the values for the design of the partial product generation. Overall, the multiplication circuit contains many levels of approximation hybrid radix encoding, partial product generation, accumulation of the partial products and finally the addition of the partial products. The proposed approximate multipliers [4] is named as $RAD2^K$, showing the selected approximate high radix encoding, e.g., RAD 64, RAD 256, RAD 1024, RAD 4096.

V. WALLACE TREE OPERATION

The Wallace tree [4] operation plays an vital role in obtaining the generation of partial products, Accumulating the partial products and performing the arithmetic operation. The operation of Wallace tree is shown in the below Fig 1.

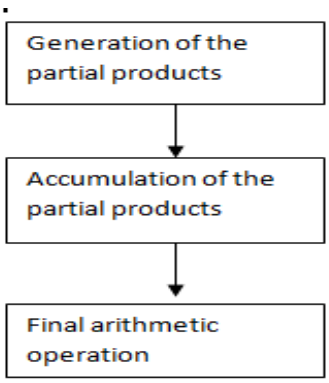

Fig. 1 Wallace tree

VI. PROPOSED HYBRID RADIX-4096 INEXACT MULTIPLIER

The accumulation of the partial product is done with the help of the Wallace tree. In the proposed method Radix-4096, we examine the scalability of Power, equivalent gate count and the error value is found .From the delivered energy savings the frequency gets increased as the multiplier size increases.

VII.RESULTS AND DISCUSSIONS

When the clock is initiated, the input value gets multiplied, and the corresponding output is obtained for Radix-4096 which is shown in figure2.The multiplication process in radix - 4096 results in better way of finding the multiplicand values.

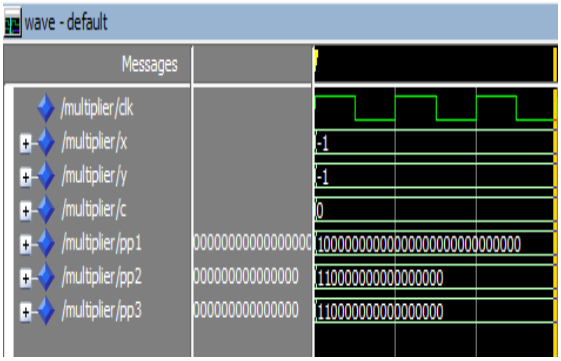

Fig. 2 Result for RADIX 4096

The total equivalent gate count for RADIX-4096 is shown in the figure3 .This total equivalent gate count is less when compared with the other Radix-k values.

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Design Summary
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Number of errors:      0
Number of warnings:    7
Logic Utilization:
  Number of Slice Latches:          100 out of  2,400    4%
  Number of 4 input LUTs:           359 out of  2,400   14%
Logic Distribution:
    Number of occupied Slices:                       189 out of  1,200   15%
    Number of Slices containing only related logic:  189 out of    189  100%
    Number of Slices containing unrelated logic:       0 out of    189    0%
       *See NOTES below for an explanation of the effects of unrelated logic
Total Number of 4 input LUTs:       359 out of  2,400   14%
   Number of bonded IOBs:            57 out of     98   58%
      IOB Latches:                                 21
   Number of GCLKs:                   1 out of      4   25%
   Number of GCLKIOBs:                1 out of      4   25%

Total equivalent gate count for design:  2,771
Additional JTAG gate count for IOBs:  2,784
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Fig. 3 Gate Count For RADIX 4096

At zero frequency level, the total power consumed for Radix-4096 is found to be 24.60mW, which is shown in figure4.

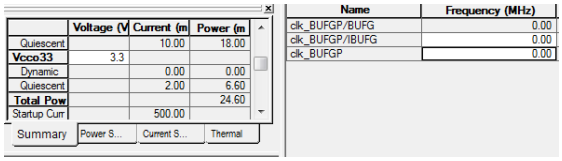

Fig. 4 At zero frequency, value for power in mW .

At 100Hz frequency level, the total power consumed for Radix-4096 is found to be 44.79mW, which is shown in figure5.

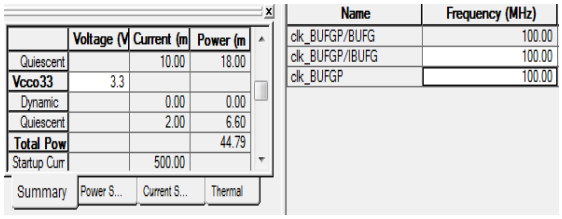

Fig. 5 At 100Hz frequency, value for power in mW

VIII. CONCLUSION

The proposed approximation of encoding for hybrid radix is designed for generation of the partial products for multiplier with small accuracy losses. Radix-4096 is energy saving, power efficient with effective gate count .The Most Significant Bit of the multiplicand are employed with accurate encoding Radix-4096 encoding with 'k'. The Least Significant Bits are encoded with approximate high radix-2^{12} encoding with 'k' .Outline factors adjusts to desirable gap among the power and energy consumption .Finally, proposed multipliers is good in efficiency which can be implemented in real time applications.

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