Sub-50nm Tri-layered Strained Si/SiGe/Si Channel nMOSFET

Lalthanpuii Khiangte, Rudra Sankar Dhar

Abstract— ***Development of a sub-50nm MOSFET on incorporating two strained silicon layers in the channel region has been carried out leading to the advent of 50nm and 100nm channel length devices. Further scalability and device analysis have been due, which has been now the focus of this paper. The effects of strained Silicon-Germanium thickness on the device leakage current have been analyzed and optimized using Synopsis TCAD simulations. The enriched device characteristics for the scaled 30nm device have also been examined in comparison to 40nm and 50nm channel length device MOSFET.***

Keywords—double strained Si layers, quantum confinement, SHOI, nanoscale regime, sMOSFET.

I. INTRODUCTION

Giving light to the scaling in the semiconductor industries, from the foundation of IC industries since the late 1960s, Moore's predictions (1965) and Dennard's scaling guidelines (1975), the growth of semiconductor industry amplified. This was marked as the First Era of scaling known as *Geometrical Scaling*. Thus, it was the foundation of National Technology Roadmap for Semiconductors (NTRS) initiated in 1991. The Second Era of scaling is the *Equivalent Scaling* - strained silicon, high-K/metal gate, multigate transistors, and use of non-silicon materials etc. was laid out by International Technology Roadmap for Semiconductors (ITRS) between 1998-2000 [1], [2] In addition ITRS also report the shrinkage of transistors beyond 2020 will have a steep cutting edge, at which point vertical scaling is suggested to be more economical.[3], [4]

The word technology 'boosters' have been coined many a time since scaling of device faces physical and economical limitations. The need of increasing circuit speed even in the ultra-low power technology mandated the inclusion of technology enhancers. Stress engineering being one of the boosters which have been successfully adopted for commercialized mass production by major semiconductor companies such as International Business Machines (IBM), AMD and Integrated Electronics (Intel) has been clubbed together with channel engineering and silicon on insulator (SOI) technology resulting in the inception of double strained silicon channel MOSFET. [5][6] Based on this inception novel double strained silicon technology MOSFET have been developed by Khiangte et al. [7] This novel device enhanced the drain current characteristics providing improvement for similar technology node device in comparison to the conventional single strained layer channel device. Further, the scalability was questionable where the physics are beyond the classical theories for nanoscale regime and as nano regime MOSFET devices have been the need in today's technological arena. Thus, in this paper sub-50nm channel devices in nanostructures have been investigated that leads to walk in to deep sub-microns and the extent of its scalability have been analyzed.

II. DEVICE STRUCTURE

The novel device have been designed and incorporated in the scientific world by Khiangte et al.[7] to have two strained silicon layers in the channel region as illustrated in Fig.1 unlike those which had been used by the current semiconductor industries [8][9][10]. These strained silicon layers have been kept to be ultra-thin of 2nm thick to accommodate the carrier confinement in both the layers. The buried oxide thickness has been varied and reduced from 100nm to 25nm for 50nm and 30 nm channel length respectively while scaling the device down to nanostructure of 30nm channel length. This specific structure induced biaxial strain in the channel layers: tensile and compressive strain for s-Si layers and s-SiGe layer, respectively.

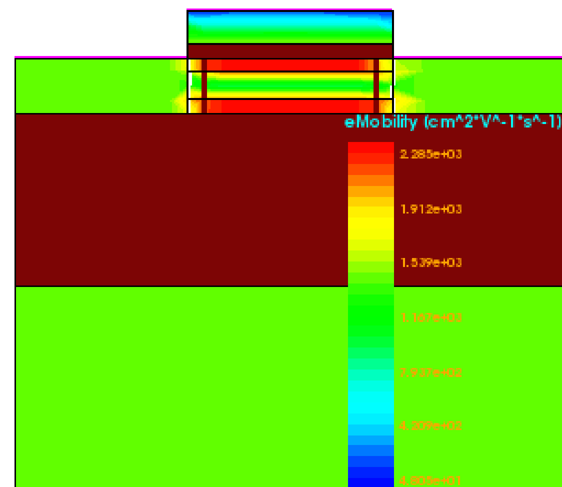

Fig. 1 Double strained silicon layer MOSFET

III. PHYSICS OF DOUBLE STRAIN LAYERS

Strained silicon technology used the well-known concept of strain inducement as in physics. Given a length 'L' and is subjected to tensile/compressive force 'F' and elongates/shrinks by length Δ, then the change in length is divided by the initial length and is termed as Strain (ε) [11][12]:

$$\varepsilon = \Delta / L \quad (1)$$

Revised Manuscript Received on April 15, 2019.
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Utilizing the lattice mismatch of silicon (L_1 = 0.54311nm) and silicon-germanium (L_2 = 0.565791nm) both uniaxial and biaxial strain can be introduced during the construction of devices in semiconductor industry. Thus, yields high speed with the same technology node. The main concept is the alteration of band structure [13][14][15] due to the strained induced in the channel layers forming a double strained silicon channel. Each energy level of Si is composed of six equal energy states [16][17] which have equal electron effective masses in all the directions: two perpendicular Δ_2 states and four Δ_4 states parallel to the plane. When biaxial stress is applied in both the silicon layers, the Δ_2 states and Δ_4 states are split up into lower and higher energy states respectively. Thus, electrons are repopulated in the lower energy states (Δ_2) and simultaneously the effective mass of electrons in the Δ_2 valley is reduced from 0.33m_o in unstrained silicon to 0.19m_o in strained silicon layers [18] causes a significant increase in carrier mobility. Also the electrons encounter less vibrational energy from the nucleus of the silicon atom as strain induced has large energy difference between Δ_2 and Δ_4, thus inter-valley phonon scattering is of the rate of 500 to 1000 times less than the relaxed silicon. These factors increase the device speed by ~35% while ~25% reduction in power consumption expected without further reduction of the device size [19]. The successful implementation of this strain technology was demonstrated first in the n-channel MOSFET with strained Si channel in 1992 exhibiting 70% higher carrier mobility and many more successful implementation of strain Si technology have emerge till date [16] Thus, in our device illustrated in Fig.1, with an additional layer of lower strained silicon in the channel region catalyzed the outstanding properties of strained-silicon-technology into manifold.

IV. RESULTS AND DISCUSSION

Based on the Multivalley model [16][17] appropriate computation of strained induced altered band structure is incorporated in the design of double s-Si heterostructure on insulator (SHOI) MOSFET for 30nm technology node in the device using Sentaurus TCAD [16] and Multivalley electron mobility model for carrier mobility. In each valley the stress effect is accounted separately. The strain induced density-of-mass (DOS), effective mass and dispersion of band structure are included in the piezo model corresponding to the k.p theory. The design optimization of 30nm device structure are exemplified by Fig. 2 with variation in the thickness of strained SiGe (s-SiGe). As depicted for 30nm device with the increase s-SiGe thickness there is a proportional increment of current leakage. The leakage current analysis as illustrated by Fig. 3 decipher 3nm SiGe thickness with both the strained Si (s-Si) thickness constant to be 1.5nm each to exhibited minimal leakage within the acceptable range. The buried oxide (BOX)

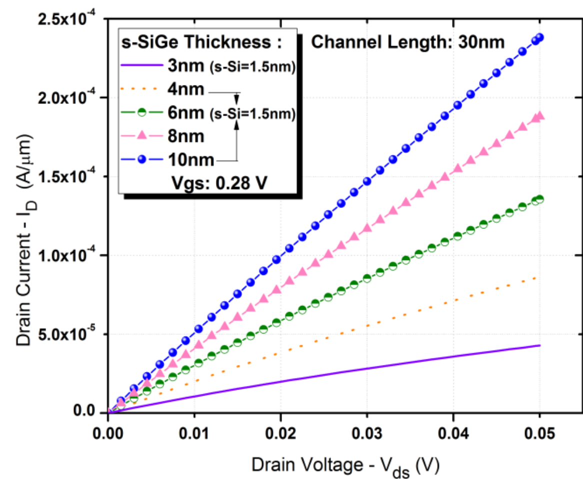

Fig. 2 Output Current-Voltage Characteristics of 30nm channel length Tri-layered HOI MOSFET with variable s-SiGe thickness

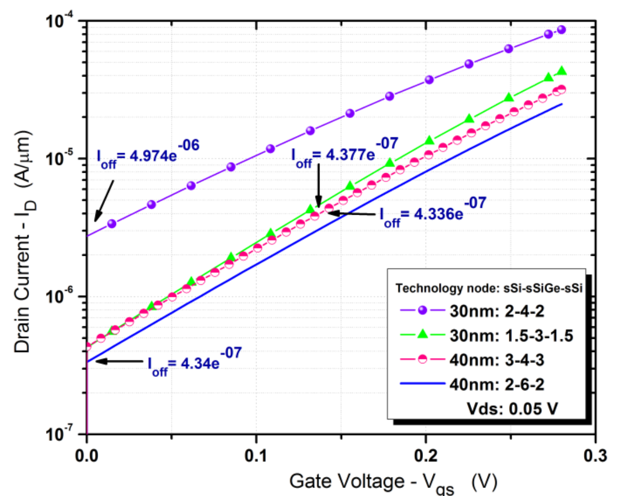

Fig. 3 Current-Voltage Characteristics indicating leakage current for different thickness of the tri layered channel region

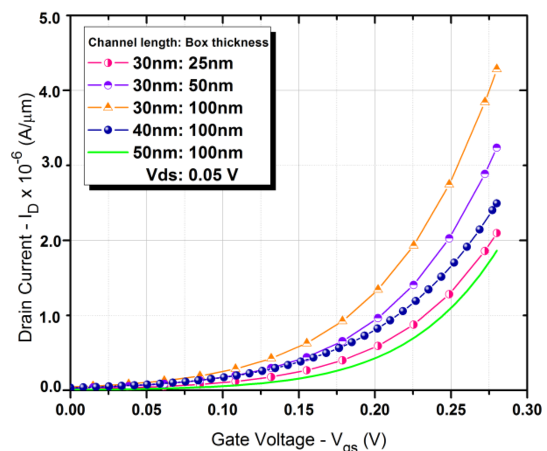

Fig. 4 Current-Voltage Characteristics for different channel length HOI MOSFET with variation of BOX thickness

thickness has also been varied and analyzed as depicted in Fig. 4 in which BOX variation for 30nm devices have been examined with respect to 40nm and 50nm which have BOX thickness of 100nm. It has been examined that for thinner BOX, the device drive current decreased gradually with minimum impact on current leakage. Thus, classifies the 100nm BOX thickness to be the optimized value for the particular HOI MOSFET device structure. The enrichment in the drive current of the optimized device for 30nm is ~27% in comparison to the 40nm channel length HOI MOSFET. Electric fringes in BOX layer is analyzed and studied in [20],[21] which has been the major issue in sub-100nm FD/SOI CMOS which could be the cause of mobility degradation. To study the effect of buried oxide (BOX) thickness variation, devices with 100nm and 25nm thick BOX double strained Si layer MOSFET have been developed on the 30nm technology node and the effect of variation in thickness on electron mobility is analyzed. Mobility of electron in lateral direction along the channel region for 100nm and 25nm thick BOX is depicted in Fig.5 (a) and Fig. 5(b). With the increased electric field in thinner BOX layer, electron mobility in the lower s-Si layer of the channel improved as shown in Fig.5 (a) compared to the thicker BOX layer (Fig.5 (b)) of the same technology node by ~2%. Also the overall electron mobility for thick and thin BOX layer are almost equal in both devices but, with further reduction of BOX thickness to less than 25nm, substantially high transverse electric field occurs, which could degrade the electron mobility in the device. Therefore, ~25nm

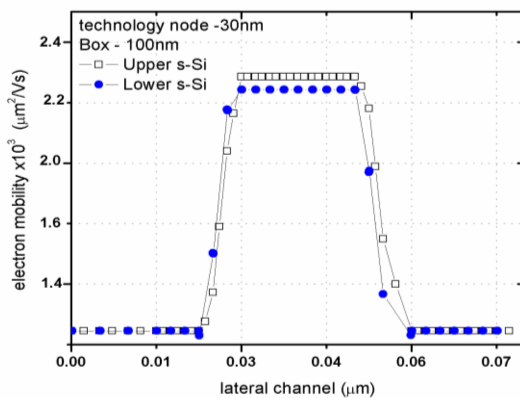

Figure 5(a): Illustration of different electron mobility for both s-Si layers in the channel region as an effect of thick BOX

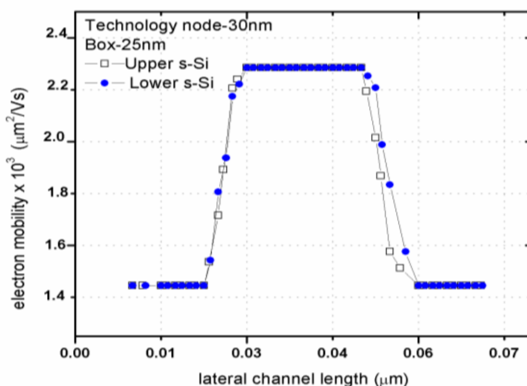

Figure 5(b): Electron mobility for both s-Si layers in the channel region (thin BOX)

thick BOX layer is optimized for acquiring maximum electron mobility through the channel.

V. CONCLUSION

Double strained silicon channel HOI MOSFET has been studied and analysis for deep sub-microns carried out. Development of 30nm channel length device is carried out, which is compared with the 50nm device and the former exhibited improved device performances of 88% in drive current enhancement on reducing the BOX thickness to 25nm. Hence, an effect of buried oxide thickness on the strain layers has also been analyzed, which indicated ~2% increment in carrier mobility on BOX thickness reduction from 100nm to 25nm in a 30nm channel length device.

ACKNOWLEDGMENT

The authors thank NIT Mizoram for providing blissful facilities to carry out this work and especially to the SMDP-C2SD project for providing the workstation for simulation with special gratitude to all the members of Department of Electronics & Communication Engineering, NIT Mizoram for their excellent support throughout the work.

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