

Design of Efficient Single Precision Floating Point Multiplier using Urdhva Triyagbhyam Sutra of Vedic Mathematics

Sai Venkatramana Prasada G S, G Seshikala, Niranjana S

Abstract--- Multiplication of floating point(FP) numbers is greatly significant in many DSP applications. The performance of the DSP's is substantially decided by the speed of the multipliers used. This paper proposes the design and implementation of IEEE 754 standard single precision FP multiplier using Verilog, synthesized and simulated in Xilinx ISE10.1. Urdhva Triyagbhyam Sutra of Vedic mathematics is used for the unsigned mantissa calculation. The design implements floating point multiplication with sign bit and exponent calculations. The proposed design is achieved high speed with minimum delay of 3.997ns.

Index Terms: Floating point numbers, Single precision, IEEE 754, Urdhva Triyagbhyam Sutra, Vedic mathematics.

I. INTRODUCTION

Multiplication of floating point binary numbers is the most important operation in DSP applications. IEEE 754 standard provides formats for the FP numbers. IEEE 754 standard format for single precision(32-bit) FP number consist of a Sign unit(1-bit), Exponent unit(8-bits) and Mantissa unit(23-bits) as shown in fig.1.

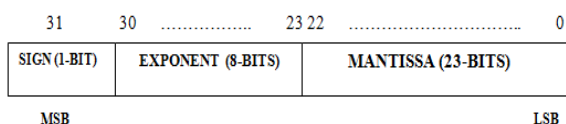


Fig.1: IEEE 754 Single Precision Format

MSB's of two 32-bit numbers are XORed to generate sign bit of the product. Exponent of the product is calculated by adding exponents of the inputs using Carry Look Ahead(CLA) adder and biasing to -127. Mantissa multiplication unit is designed using Urdhva Triyagbhyam Sutra of Vedic mathematics.

A. Urdhva Triyagbhyam Sutra

The exact meaning of Urdhva Tiryabyham sutra is "Vertically and Crosswise". Urdhva Tiryabyham Sutra can be applied to all the cases of multiplication. In this method, the partial products & their sum is obtained in parallel. The steps involved in 2x2 multiplication[14] using Urdhva

Tiryabyham Sutra are shown in fig.2. The same procedure can be extended for 3x3 multiplication[3] as shown in fig.3.

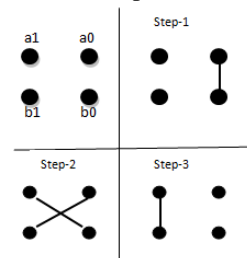


Fig.2. 2x2 Multiplication Using Urdhva Sutra

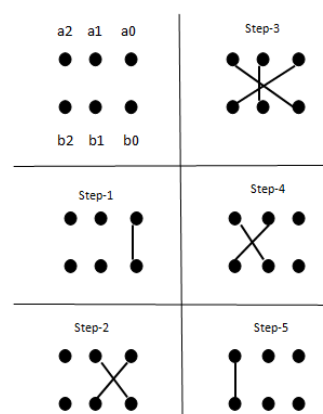


Fig.3. 3x3 Multiplication Using Urdhva Sutra

The 3x3 multiplier can be used for constructing higher order multipliers such as 6x6, 12x12 and 24x24 bit multiplication.

II. PREVIOUS WORKS

Swapnil Suresh Mohite, Sanket Sanjay Nimbalar, Madhav Makarand Bhathande, Rashmi Rahul Kulkarni presented the design of 32-bit FP multiplier using Urdhva Triyagbhyam sutra[1] which reduces the processing delay. Code was written in VHDL using Xilinx ISE series. Overall performance of designed multiplier depends upon the performance of mantissa multiplier unit. Mantissa multiplier was designed using Urdhva Triyagbhyam sutra. 3x3 multiplier was used as basic multiplier. 8-bit CLA is used for adding two 8-bit exponent. Output of the adder was biased to -127 to generate the exponent of output floating point number. The proposed multiplier circuit takes 71.239ns to perform multiplication of two 32-bit floating

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Sai Venkatramana Prasada G S, Assistant Professor, Dept. of E & C, Srinivas University, Mangaluru -574146 Research scholar, School of E&C, Reva University, Bangalore -560064, India. (E-mail: svprasad007@yahoo.co.in)

Dr.G Seshikala, Professor, School of E&C, Reva University, Bangalore -560064, India.

Dr.Niranjana S, Associate Professor-Senior Scale, MIT, MAHE, Manipal, Udupi -576104, India.

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point binary numbers. This delay is significantly less than Booth multiplier. Aniruddha Kanhe, Shishir Kumar Das, Ankit Kumar Singh described the design and implementation of IEEE 754, 32-bit FP multiplier [3] using Vedic mathematics. The

Urdhva Triyagbhyam sutra was used for mantissa multiplication. Multiplication was achieved by adding the biased 8-bit exponent, multiplying the normalized 24-bit mantissa and resultant was converted in excess 127 bit format. The exponent calculation unit was implemented using 8-bit RCA. Sign bit was calculated by XORing the MSB's of the inputs. The multiplier was designed in Verilog HDL and simulated using Modelsim simulator. This design was synthesized using Xilinx ISE12.1 tool targeted on the Xilinx Vertex5. The design utilizes lesser number of LUT's, thereby reducing the power consumption.

Soumya Havaldar, K S Gurumurthy [4] proposed the design of multiplier for floating point numbers using Vedic mathematics. This design also manages overflow, underflow and rounding. Design was coded in VHDL, simulated and synthesized using ISE14.6 tool targeting the Xilinx Vertex VI FPGA. This work concludes that; the proposed design occupies less space and high operating speed due to vertical and crosswise calculation using Urdhva Triyagbhyam sutra.

Pooja Hatwalne, Ameya Deshmukh, Tanmay Paliwal, Krupal Lambat proposed a design and implementation of single precision FP multiplier using VHDL [5]. 24-bit multiplier using Urdhva Triyagbhyam sutra of Vedic mathematics was designed for mantissa calculation. 8-bit CLA adder was used for exponent calculation. The design was synthesized and simulated in Xilinx ISE14.7 targeted on Spartan3 device. The proposed floating point multiplier showed optimized and better timing performance with total delay of 36.19ns.

III. SIMULATION RESULTS

32-bit floating point multiplier design is implemented in VHDL and simulated using Xilinx ISE10.1. The unsigned mantissa multiplication is achieved by using Urdhva Triyagbhyam Sutra of Vedic mathematics. Fig.4-6 shows the RTL schematics of 32-bit floating point multiplier, mantissa unit and exponent calculation unit respectively.

Fig.4: Schematic Of 32-Bit Floating Point Multiplier

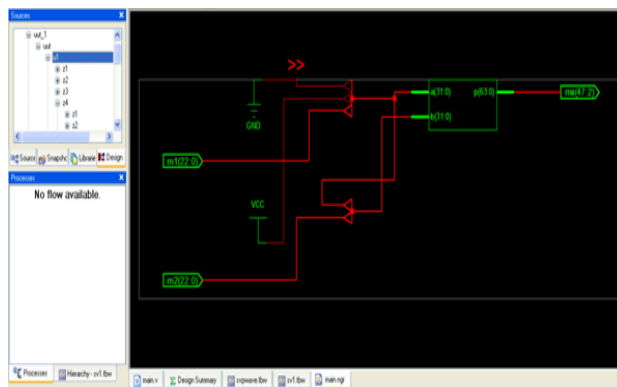


Fig.5: Schematic Of Mantissa Calculation

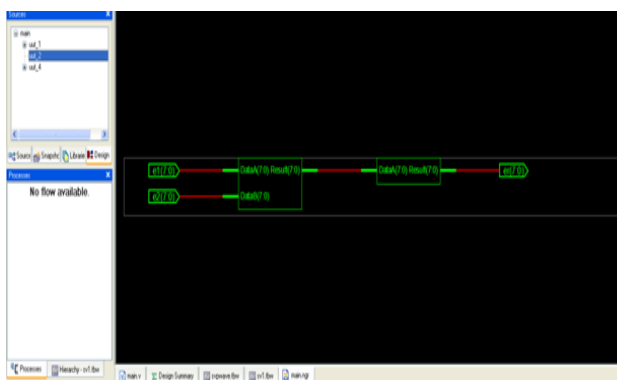


Fig.6: Schematic Of Exponent Calculation

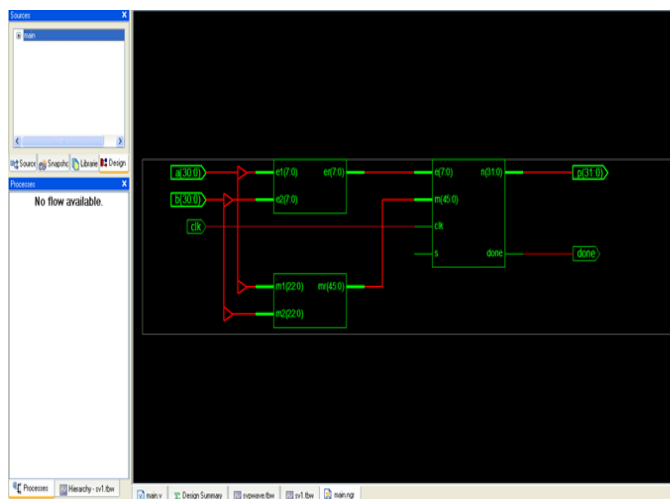
Table 1: Performance Analysis

Parameters	Proposed Urdhva 32X32
NO. SLICES	298
NO. 4 IP LUT	579
NO.OF BONDED IOBs	96
COMBINATIONAL DELAY	3.997ns

Table 1 shows the device utilization and combinational delay of the proposed design. Table 2 shows the comparison of the proposed design with the designs of the literatures. The proposed design exhibits lesser device utilization and delay.

Table 2: Comparison of Performance Parameters

Paper	Number of Slices	LUT's	Bonded IOB's	Time delay(ns)
[1]	911	1580	96	71.293
[3]	-	966	99	5.246
[4]	-	705	96	21.823
[6]	-	672	96	4.94
[9]	1389	1545	129	13.141
[10]	2041	3317	206	89.374
[11]	-	1032	99	5.246
[12]	999	1819	-	14.17
Proposed design	298	579	96	3.997



IV. CONCLUSION

The single precision FP multiplier using Urdhva Triyagbhyam Sutra is designed in VHDL, simulated using Xilinx ISE10.1 and parameters such as number of slices, 4 input LUT's and delay were analyzed and compared with the literatures. The proposed design utilizes lesser number of slices and LUT's thereby reduces the hardware requirement. High speed is also achieved by the use of Urdhva Triyagbhyam Sutra and CLA adder. This proposed work can be extended for the design of double precision(64-bit) FP multiplier using Vedic mathematics.

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