Performance Analysis of a 15-Level Cascaded Multilevel Inverter

K.C. Ramya, S. Sheeba Rani, K. Vinoth Kumar, S. Sivaranjani, S.R. Boselin Prabhu

Abstract—Multilevel Inverters (MI) are comprehensively used in both medium / high voltage applications because of its higher output and lower switching losses. The harmonics problem will automatically get reduced in case of MI by increasing the levels of an inverter. However, this results in increased cost and size the inverter. Hence in order to overcome this problem, this work proposed a novel 15 level MI topology with reduced switches. Space Vector Pulse Generation Circuit (SVPWM) is instigated to produce switching pulses for MI. Thus the efficacy of the proposed topology is validated using the MATLAB software. From the obtained outcomes, it is confirmed that this proposed topology results in better harmonic reduction with low switching losses.

Index Terms—MI, Cascaded H- Bridge Inverter (CHBI), SVPWM, THD

1. INTRODUCTION

In modern years, power quality issues plays a chief role in Industries. While implementing the conventional inverter in medium and high voltage applications, the power loss and rating constraint of semiconductor present in that inverter leads to some limitations. Hence in order to overcome this problem, MIs are introduced [3,4]. MIs are effective in both medium as well as high and medium voltage applications because of its high voltage output, lower THD and less dv/dt [7-9]. It also results in low Electromagnetic Compatibility (EMC) problems. Hence, the usage of MI for various applications has been increased.

Thus the conventional MI's are classified into,

- ✓ CHBI
- ✓ Neutral Point Clamped and
- ✓ Flying Capacitor Inverter.

Among those structures, CHBI offers more advantages such as lower EMI and THD than the other two topologies. Hence it is highly appropriate for high power applications.

However, whenever a levels of MIs increases, the usage of power modules implemented in the system gets increased. This leads to have complexity in driver isolations as the increased level necessitates an isolated power source. Thus in turn results in increased cost of driver circuit. In order to override this issue, this work proposed a unique single phase 15 level CHB MI with reduced switches. In this topology, SVPWM technique is tailored to generate gating pulses. The proposed topology is evaluated by simulation using software.

2. CONVENTIONAL METHOD

The configuration of traditional CHBI comprises series of H bridge unit. Every bridge part separately has one DC supply [1,2]. With the help of bridge circuit, three distinct output, +V/ -V/ zero is obtained. Every switching device conducts for 180°. This results in equal current stress over the entire witching devices.

Thus the number of levels resulted in an output is defined as,

$$s=2k+1 \quad (1)$$

Where,

s – No. of voltage (output) levels /phase

k – No. of DC supply / phase.

A number of single-phase full bridges present in M-level CHBI is given by,

$$n=(M-1)/2 \quad (2)$$

Where,

M- Total level of CHBI.

n- No.of H bridges /phase.

Thus, output voltage is the summation of each bridge output.

Where, $V_{ph}=V_{DC1}+V_{DC2}$ (3)

2.1 Operation of CHBI

Figure 1 describes the structure of a 1ϕ N-level CHBI. An isolated DC supply is associated with each bridge inverter. The distinct output voltage, $+V_{dc}$ / 0 and $-V_{dc}$ is obtained from the individual inverter level. Whenever the Switches S_1 / S_4 are in 'ON' condition, $+V_{dc}$ is attained. Similarly when the other two switches are in 'ON' condition,$-V_{dc}$ is obtained. When all the switches remains 'ON', then the voltage at the output becomes zero. Thus the voltage present at the output is the addition of the AC voltage obtained at all the levels[5].

The 1ϕ voltage waveform for a 5 level CHBI is shown in Figure 2.

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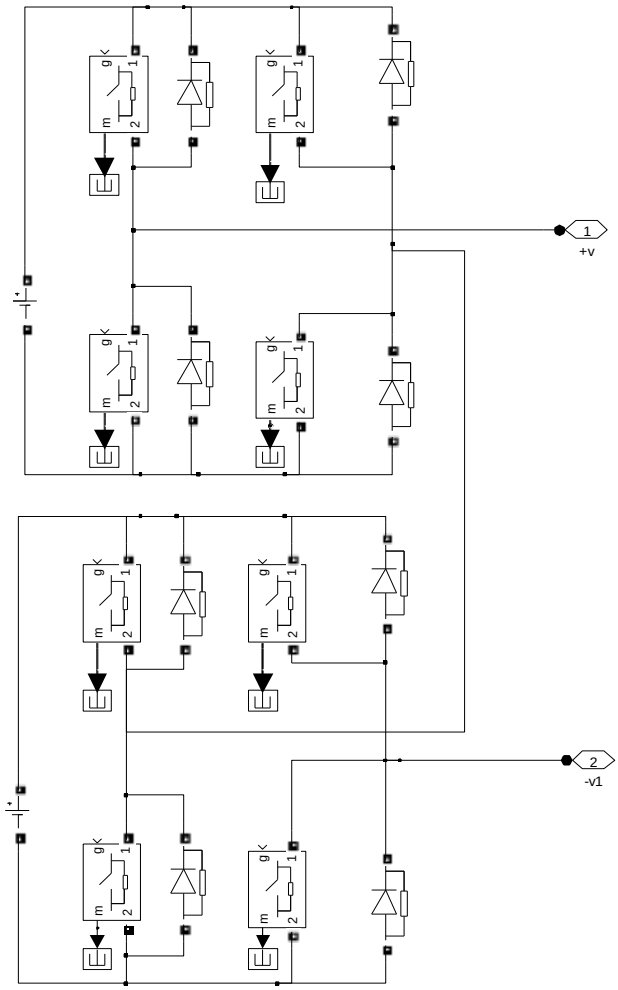

Figure 1: Structure of a single-phase N-level CHBI

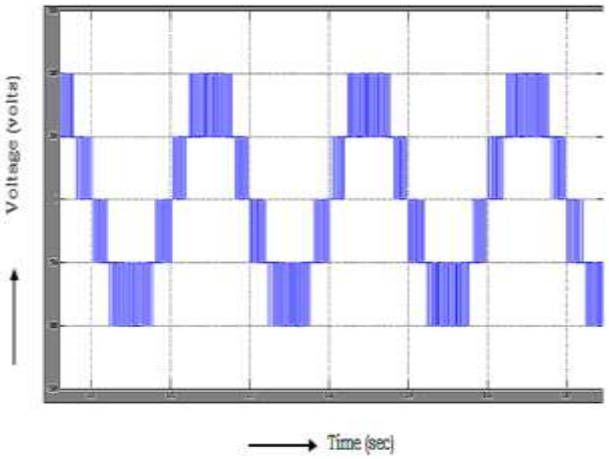

Figure 2: Output voltage of H bridge

3. PROPOSED MI TOPOLOGY

The projected MI topology is depicted in Figure 3. It comprises 7 switches and 3 diodes and 3 to generate 15 level output. Thus this proposed methodology is asymmetric and the implemented DC voltage sources are in the ratio 4:2:1. [6].

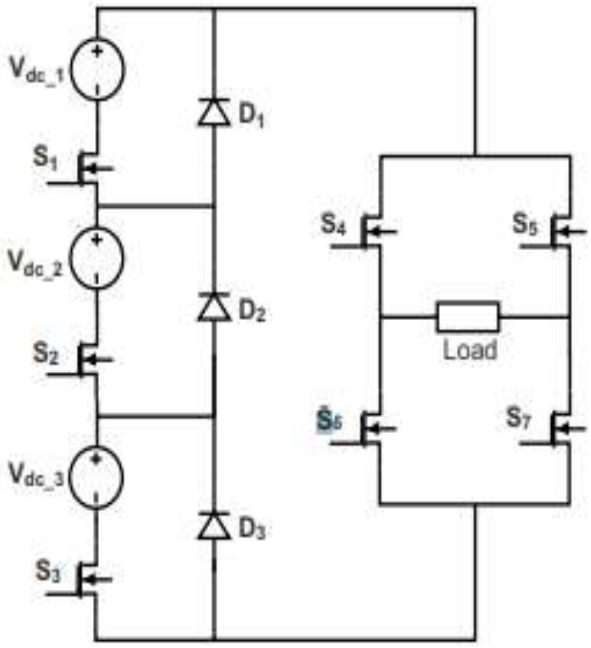

Figure 3: Proposed Topology

Thus the operation of this methodology is subdivided into 15 distinct modes which has dissimilar voltage levels. The operating modes and switching states of the proposed topology is shown in Figure 4. In these, state 1 to 7 are positive half and state from 9 to 15 corresponds to negative half of a output.

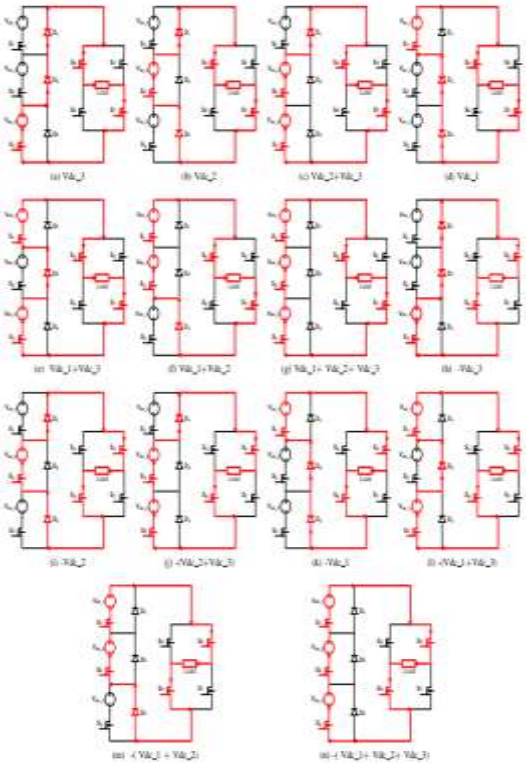

Figure 4 : Operating Modes of Proposed methodology

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3.1 Modulation Technique

The main aim of modulation technique is to produce triggering pulses for the switches which is plays a vital in generation of sinusoidal output waveform. Hence, proper modulation topology has to be adopted to control the output waveform. There are many different modulation topologies are available. Among those, the most popular one is SVPWM. Thus the Realization of SVPWM is carried out in the following steps

1. Determine, angle (α) ,V_d, V_{ref} and V_q
2. Determine of time duration for each sector
3. Calculate each transistor 's switching time (S_1 to S_6)

4. RESULTS AND DISCUSSION

Hence, to analyze the performance of this projected topology, it is replicated in MATLAB environment. THD is examined using Fast Fourier Transform (FFT) technique. Figure 5 depicts the output voltage. Figure 6 portrays THD spectrum of an output voltage and thus an obtained THD value is about 5.90%.

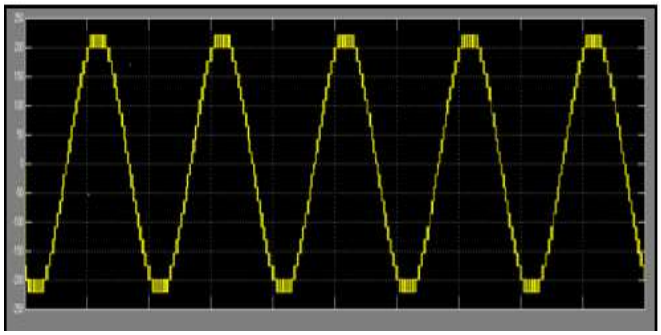

Figure 5 :Output voltage waveform

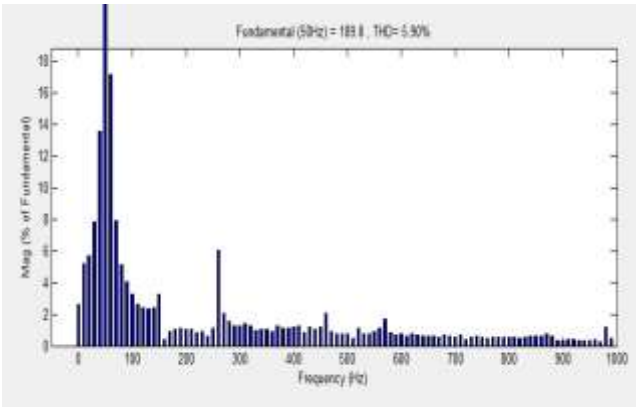

Figure 6 : FFT Analysis

Thus the performance of projected MI under different modulation topology and the obtained THD values are displayed in Table I.

Table I: Comparison of THD for different PWM topology

Topology	%THD
PDPWM	8.90
PODPWM	9.42
SVPWM	5.90

From the table, it is clearly perceived that the proposed SVPWM topology exhibits better harmonics reduction than other modulation techniques.

5. CONCLUSION

An asymmetric 15 level MI is proposed in this work. It comprises of 7 switches and 3 diodes to produced 15 level output. A novel SVPWM modulation technique is utilized to generate gating signals. From the results, it is evident that this proposed system reduces switching losses with less THD. Thus, the overall cost reduction and effective reduction of total harmonics distortion is achieved.

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