

A Low Power and High Reliability Magnetic Full Adder Circuit Design Based on Separated Pre-Charge Sensing Amplifier

K.Sudhakar, S.Arunprathap

Abstract: The Magnetic Tunnel Junction is entrenched in CMOS to built nonvolatile memory and logic circuits. Nevertheless this kind of circuit grieves from low reliability in sensing process and memory element. This leads to restriction of its real-world application for logic operations. This project work helps a novel design of magnetic full adder to avoid the above problem by using separated pre-charge sensing amplifier circuit. The proposed method results in operation at a lower supply voltage, less than one volt by separated discharging and evaluation phases of the sensing operation. Higher sensing reliability is achieved by reducing the effect of process variation. When compared to previous methods it preserves speed and low power consumption. This work all the circuits are designed by post layout simulation tool.

Index Terms: Magnetic Full adder, CMOS, MTJ and SPCSA.

I. INTRODUCTION

The conventional CMOS logic circuits consists the two main series problem are increasing leakage power and partial scalability, recently the various novel circuits are help the CMOS technology endure to second-rate. The three thin films –It consists of two ferromagnetic layers and one barrier

Self-possessed, vertical Nano pillar is called as Magnetic Tunnel Junction (MTJ). The ferromagnetic layer resistances depend on comparative spin bearings. In many application standards the storage film and reference film in opposite bearing, which is anti-parallel or parallel to storage layer.

Magnetic Tunnel Junction (MTJ) is consists as most favorable developing technologies to overwhelmed the CMOS logic circuit power leakage problem, which is appreciate to its non-instability, Infinite durability direct on/off, and CMOS process are easy to integrate. Also Magnetic Tunnel Junction can be easily employed in back end design process, above mentioned CMOS circuit has few number of extra masks. It permits hybrid CMOS circuit's to develop the both memory and applications which group the rewards of both technologies. More number of innovative circuits is currently proposed in hybrid Magnetic Tunnel Junction/CMOS circuits. It consists merits in both technologies. Reconfigurable logic circuit has two examples

1. Magnetic Look up Table
2. Magnetic Flip Flop.

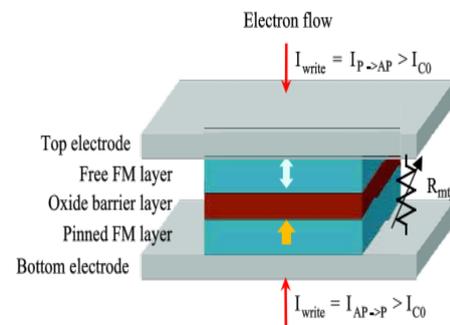


Figure 1.1 Vertical Structure of the Perpendicular Anisotropy Magnetic Tunnel Junction (MTJ)

The magnetic full adder circuit designed on login in Magnetic Tunnel Junction memory cell design near ultra-low power high mass density integrated circuits.

Magnetic full adder can also impress the jam of data communication among memory block and separated logic module. Magnetic full adder circuit diagram work based on sensing circuit of current mode. It is not suitable for 90 nm sub-micron technology for the following reasons

The first reason which is more sensitive to the Processing factors variation, which develops more significant for imminent miniaturization of manufacture process, another reason is linked with the capacitor (C₀), which performance the virtual current ground to the control the charge transported to outputs. The capacitor should be sufficient to put up the charge in load capacitance and outputs, which is complex to clear the guarantee correct function of DCM [2] logic circuits. The pre charging sensing amplifier is used to overcome the disadvantages of DCM circuits. Magnetic full adder circuit schematic is designed based on pre charge sensing amplifier circuit. It is not suitable to 28 nm sub micro meter technology for the following reason, first one is stack of transistor in pre charge sensing amplifier and large voltage headroom in CMOS logic tree, which creates problem in low supply voltage in sub micrometer technology. Another one is related to more mismatching in sensing logic circuits due to process-voltage-temperature difference.

To overcome this problem Separate Pre-charge Sensing Amplifier based magnetic full adder circuit is implemented to avoid the process-voltage-Temperature difference and increase more in sensing margin of the circuit.

Revised Manuscript Received on April 19, 2019.

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The post layout simulation tool is used to design a novel Magnetic full adder circuit design based on SPCSA (Separated Pre-Charge Sensing Amplifier), which demonstrate the more reliability and minimum power

II. THERMAL ASSISTED MAGNETIC TUNNEL JUNCTION

Three important approaches are used to switch the magnetic field junction:

1. Thermally Assisted Switching (TAS)
2. Field Induced Magnetization(FIMS)
3. Spin Control Transfer(SCT)

Field Induced Magnetization is first used in MRAM since 2006 for commercial purpose. Even this method suffer from fundamental problems like that power consumption, poor scalability and low selectivity due to more switching conditions (in 10mA).

Field Induced Magnetization and Spin Control Transfer method are reduce the power consumption and better scalability due that it consider as the second generation of MRAM[3]. Spin Control Transfer is act in only bi-directional low switching current. It working as a better scalability and fast memory access make it as favorable technology for MRAM.

To avoid the thermal reliability issues the more number of Spin Control Transfer-MRAM prototypes was developed, which leads to arbitrary state disturbance while difficult to store the more than ten years. For perpendicular anisotropy storage we can use a new trend of Spin Control Transfer-MRAM. It is used for overcome the thermal reliability problems.

However it offers minimum Tunnel Magneto Resistance ratio of 120%, which restrict its concern for logic applications. Tunnel Magneto Resistance is built on temperature dependent "Exchange Bias", which is key factor to the increasing the thermal stability of magnetic storage and random switching activity. To prevent the any kind of switching activity antiferromagnetic layer is restrained by reference layer with high blocking temperature. The free layer restrained with antiferromagnetic layer by minimum blocking temperature.

The Thermal Assisted Switching is accomplished for minimize the current which is passed through Magnetic Tunnel Junction and increase(heat) the blocking temperature of free layer, which is mostly reduce the switching activity current in 4 mA can the one state to other state of Magnetic Tunnel Junction. The improvement of the stability Thermally Assisted Switching continuous high write/read speed indefiniteresolution, high Tunnel Magneto Resistance, and easy three dimensional traditional Magnetic Tunnel Junction.

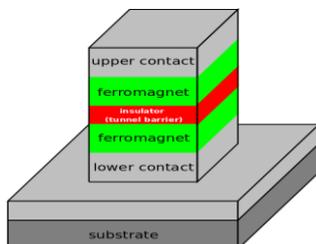


Figure 2.1: Nano pillar Thermally Assisted Switching MTJ

The fabrication technology is developed for practical applications, Therefore Thermally Assisted Switching method is used in magnetic full adder design.

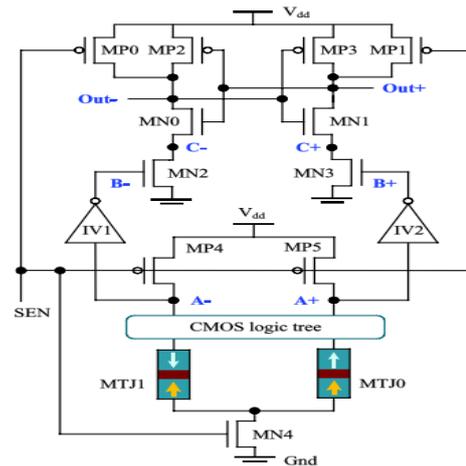


Figure.2.2: Separated Pre-charge Sense Amplifier

III. DESIGN OF MAGNETIC FULL ADDER CIRCUIT

The SPCSA (Separated Pre-Charge Sense Amplifier) produces the balancing output. It is used to design a complete logic family without supplementary inverters. All logic blocks can be easily implemented with the help of the combined MOS logic tree.

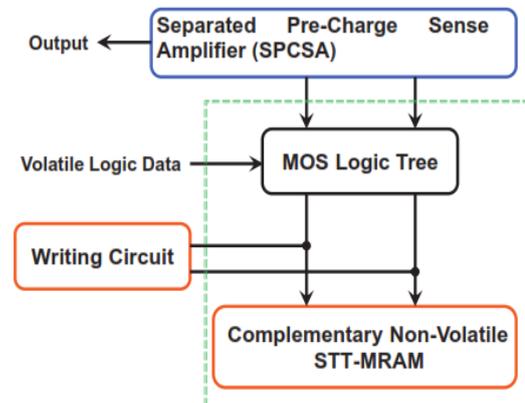


Figure 3.1: Magnetic full adder design with SPCSA

If we can design a magnetic full adder with separated pre charge sensing amplifier, for three inputs such as A, B and Carry, which produce the outputs sum and carry.

$$\text{Sum} = \text{passing } A \oplus B \oplus C = ABC_i + A\bar{B}\bar{C}_i + \bar{A}B\bar{C}_i + \bar{A}\bar{B}C_i$$

$$C_0 = AB + AC_i + BC_i$$

Then design contains the more number of transistors, the NMOS transistor from MN20 to MN24 are used produce the heat current over the magnetic tunnel junctions in writing operation process time. The circuit producing current (I_{switch}) is independent to magnetic tunnel junction heating/sensing circuit for to obtain the minimum power and area efficiency.



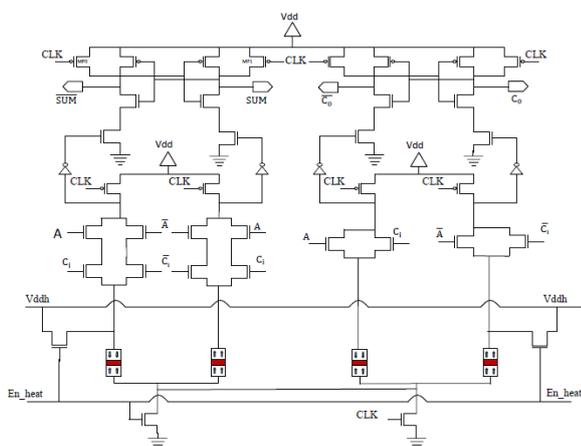


Figure 3.2: Magnetic full adder with separated pre charge sensing amplifier

IV. COMPARISON BETWEEN CMOS FULL ADDER AND PCSA AND SPCSAMFA DESIGN

Pre Charge Sensing Amplifier circuit mostly affected from submicron technology and low reliability. To obtain the high speed and low power in submicron technology we design a Separated Pre-Charge Sensing Amplifier with magnetic full adder.

The comparisons between the Separated Pre-Charge Sensing Amplifier with magnetic full adder, Pre-Charge Sensing Amplifier magnetic full adder design and CMOS full adder design in 180 nm technology node with following parameters

1. Reliability
2. Delay
3. Dynamic power
4. Static power
5. Area
6. Tunnel Magneto Resistance(TMR) Ratio

PARAMETER	CMOS FA	PCSA MFA	SPCSA MFA
Reliability		14.2	5.96
Delay	100ps	170 ps	180ps
Dynamic power	7.63uW	2.951uW	3.25μw
Static Power	71.12 nW	0	0
Area (Device count)	46MOS	(30MOS +4MTJ)	(38MOS+ 4MTJ)
TMR Ratio		200%	200%

The DCM full adder circuit is not considering for this analysis due submicron technology. To characterize the both design in balance purpose the two full adder latches are used to synchronize CMOS full adder output with clock signal, as Separated Pre-Charge Sensing Amplifier and Pre-Charge Sensing Amplifier magnetic full adder are basically synchronized. The design processes are used only the minimum width transistors are used apart from magnetic full adder circuit.

The design are developed in 180 nm technology at 500MHz and $V_{dd}=1.8$ volt, compare with CMOS full adder our Separated Pre-Charge Sensing Amplifier magnetic full adder design obtain 2X dynamic less energy.

V. SIMULATION RESULTS OF SEPARATED PRE-CHARGE SENSING AMPLIFIER

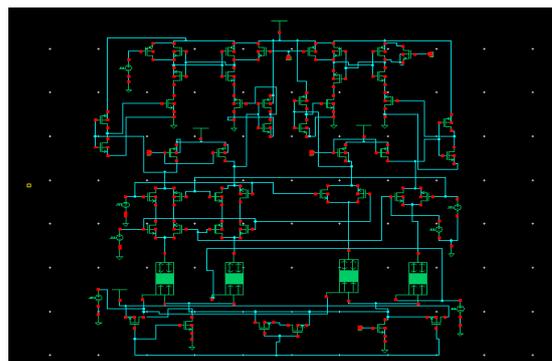


Figure 5.1: Design of Separated pre-charge sensing Amplifier

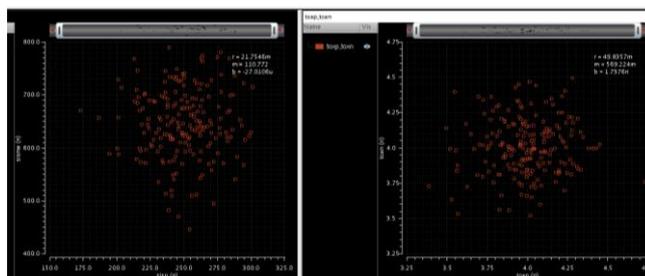


Figure 5.2: Design of Separated pre-charge sensing Amplifier Full Adder Transistor Variation

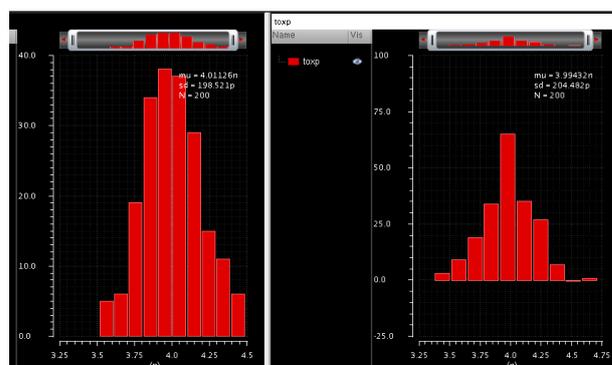


Figure 5.3: Figure 5.1 Design of Separated pre-charge sensing Amplifier Full Adder reliability output

VI. CONCLUSION

The high speed and high power is obtained by MFA circuit design depends on SPCA(Separated Pre-charge Sensing Amplifier).The comparison with CMOS full adder endorses the die area and Power efficiency and Pre-charge Sensing Amplifier endorse reliability of the circuit. Separated Pre-Charge sensing Amplifier magnetic full adder circuit used to build complex logic circuit in simple manner. The separated pre-charge sensing amplifier circuit able to operate in less than voltage, so it can be used in submicron technology to increase the reliability and minimize the sensing error.

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