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Design & Optimization of CNTFET based Low Power Schmitt Trigger using MTCMOS Technique

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Abstract: ***Power consumption to be reduced is a critical burden for any circuits reduced in portable electronic gadgets to improve battery for long life has put mandatory friction to construct low power circuit. MTCMOS technique gives two sleep mode transistors in current circuits are engage to reduce power consumption. In this proposed work is to construct powerless Schmitt trigger using MTCMOS technique in 32nm both on CMOS and CNTFET Schmitt trigger. The proposed Schmitt trigger circuit to be improved in terms of leakage, hysteresis loss and propagation delay for CMOS and CNTFET Schmitt trigger has been done by MTCMOS technique in 1V supply. The proposed design is simulated using SPICE tool in 32nm technology node. After simulation it is established that results give a notable reduction in leakage power or hysteresis loss for current design. Leakage power offers by MTCMOS approach in CNTFET based technology are 2pW and hysteresis loss 17mV at 1V power supply.***

Index Terms: CMOS, CNTFET, MTCMOS, Schmitt Trigger.

I. INTRODUCTION

The most useful and excellent method used in both the analog as well as digital application for the elimination of noise is Schmitt Trigger since its discovery. There are various area's which have been covered using this technique being communication systems, instrumentation systems and measurement, buffering and signal processing. Now-a-days lot of research going on these diverse circuits; some of them require instrumentation and the measurement as a part of the complete circuit. Basically a single chip is a requirement of implementing these systems with primary functioning circuitry [2].

Earlier Schmitt trigger used an op amp along with two resistors for the implementations but, unfortunately these are now not adaptable for the current CMOS chip design era because of various existing issues being large dissipation of power and area constraints [15]. So, to overcome these drawbacks and issues numerous new technologies and configurations have been developed which are in compatibility with CMOS technology [1].

Comprising of the three NMOS or one PMOS transistors are simplest structure was established and made. A diagram of conventional Schmitt trigger comprising of four transistors is shown in the figure 1 below [6]. Because of the well defined property of hysteresis, Schmitt trigger is famous amongst these diverse applications because two threshold levels are present. The signal of the output is drag low when the threshold input move high to low, in the conventional Schmitt trigger circuit [7].

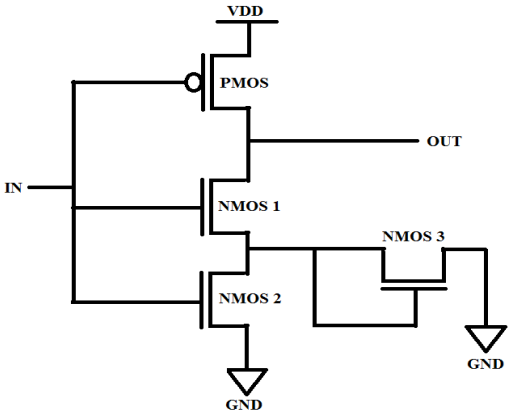

Figure 1: Conventional 4T Schmitt Trigger

There is an outcome of a high voltage then the input voltage is negotiating and the threshold values reaches below low to high. These threshold voltages values are dependent over the dimensions and the process parameters of the transistor [3]. For the enhancement and improvement of the characteristics and features there are several ideas and various techniques which have been improved in Schmitt Trigger being high speed, hysteresis which is tunable, functioning of temperature co-efficient [8].

Currently, the main challenge amongst us is initiation of low voltage designed battery powered nanoscale VLSI systems. Power dissipation is required by portable electronic devices to improve the life time of battery. Over the overall reduction of power dissipation exhibits a great impact of the scaling of the supply voltage [5]. There is a critical effect exhibited on the effects of short channels when the feature size of CMOS technology nanometre scales were scaled down, as the device dimensions cannot be scaled similar to supply voltage. There are some drawbacks being the density of power is high along with the reliability issues or leakage currents are high. The aforementioned limitations function as hindrance in scaling of CMOS technology for high demanded density and energy efficient applications [12]. To control these limitations there are some techniques being MOS/SOI which is used, but the technology still needs some alternative materials to control these nano-scale challenges [16]. Therefore, amongst several nano-devices CNTFET is related to MOSFET in electrical and structural devices. The architectures of CMOS have been used in CNTFET, but these new alternative technologies should be considered as the robust designing of the circuit is becoming crucial time of nano-scale [11].

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II. LITERATURE REVIEW

[1]. Joseph et.al (2015) stated the model of Schmitt trigger is comprised of low voltage MOS transistor. The techniques used for implementation was named as dynamic threshold MOS (DTMOS) and multiple threshold MOS (MMTMOS), variable threshold MOS (VMOS) and floating gate MOS (FTMOS). The circuits were designed in 180nm CMOS technology using TSMC for the conventional and the proposed circuits are stimulating at 0.5v. They investigated and compared to the performance of Schmitt trigger being hysteresis curve width, delay introduced, and dissipation of power for the inputs as well as supply voltages. After attaining their results various applications for every Schmitt triggers were suggested [13].

[2]. Parakundil et.al (2014) stated that the most difficult and the crucial task for the circuits is the reduction or the minimization of the power consumptions. As the order of portable devices is enhancing, so it is essential that these portable devices are designed with circuits consuming low power along with lesser dissipation of energy. The flip flops which are designed were both explicit and implicit. The circuits were diminishing of power consumption and the techniques to be applied in that circuit are MTCMOS and self tractable voltage level. The circuits which they designed were of 45 nm technology and the frequency taken was 1 GHz [12].

[3]. Dobriyal et.al (2012) stated that there is an important part played by the consumption of power in the integrated circuits and amongst the roadmaps of semi-conductors it is placed in the top of three challenges in international technology. They reported that the internal transitions are most of the powers were devoured by the timer allocation network and flip flop in the integrated circuits. They have described various techniques for the implementation of flip flops along with the clocking system in low power as they were also analyzed. On comparing various techniques they discovered and reported that the least power was consumed by CPSFF than CDMFF, CDFF and DEFF. They have reported and used a new technique CPSFF incorporating MTCMOS technique and thus which minimizes the power dissipation from 20% to 70% by the initial CPSFF. They also illustrated that for the creating a new clocking system into a new flip-flop two techniques can be incorporated easily being the double edge triggering and low vibrates clocking [9].

The advantages of CNTFET devices are that they are small in size, their transport is ballistic and their compatibility with the high k materials is good. The device exhibiting the aforementioned features and characteristics depicts excellent potential for being used in ultra high density as well as performance along with the low power designs [4]. The band shape of CNTFET which is one dimensional it reduces the backscattering, they also indicate ballistic transport characteristic features with extremely high speed operations [10]. As the holes and electrons their mobility is similar therefore the p type and n type transistors having same geometries exhibit similar current drive. Because of the aforementioned reasons the size and optimizations of the circuits is simpler [14].

III. CIRCUIT DESCRIPTION

A. CNTFET based Low Power Schmitt Trigger

Schmitt trigger is working as a comparator to differentiate the input signal with some patent to choose threshold values. In this conventional circuit, the input signal goes to high-rise than the patent to choose high threshold value, the output of that circuit is going to high. Comparably, input goes lower than patent to select lower threshold value or output is going to low. But the main aim to be regarded in this design is that the input is applied between two select threshold values, the output conserves its value because Schmitt trigger can perform dual action in the circuit. The design of VLSI system has pretty a restrict aspect due to leakage power consumption when CMOS technology is diminishing. The application of plotter technologies in power consumption circuits, leakage power reduced up to a substantial area. In this circuit to disconnect the powers condemn then the circuit is not handling in standby mode, leakage power enhance to neglible. But, below notable scaling circumstances planner device formation undergoes to a restriction of short channel effects (SEC). This construct the planner to moves towards three dimensional structures like CNTFET transistors based technology. Figure 2 recognize the diagram of CNTFET low power ST circuit.

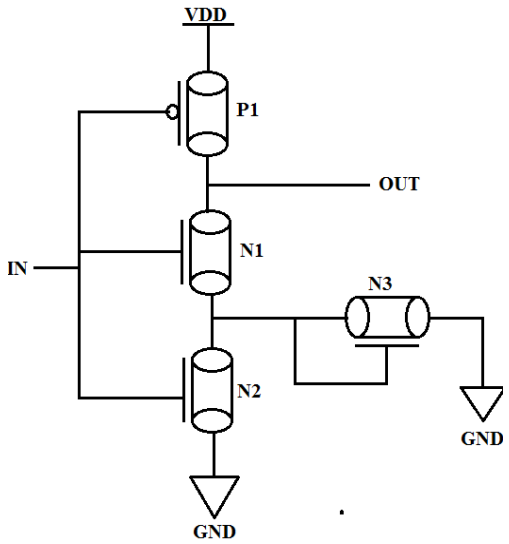

Figure 2: CNTFET Low Power Schmitt Trigger Circuit

B. CNTFET Construct Low Power Schmitt Trigger Using MTCMOS Technique

The leakage power or current is required to be more diminished so different design has been implemented known as MTCMOS. As shown in figure 3 high Vt sleep transistor which are entrance of power supply and ground to the low Vt (Sleep Bar) results in diminish of the leakage power along with the embracing power dissipation in that circuit.

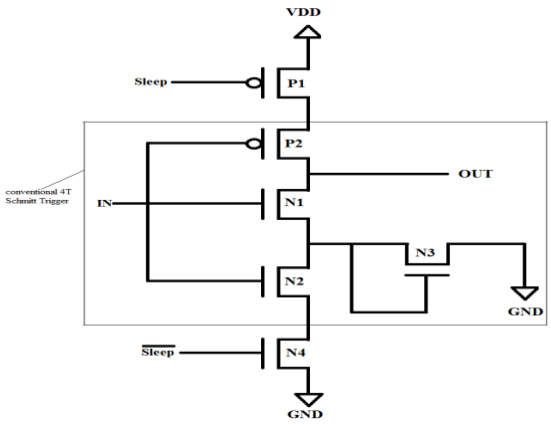

Figure 3: CMOS 4T ST using MTCMOS

This is constructing by integrated two sleep transistors in the CNTFET Schmitt trigger circuit. Yet, when the input sine wave is applied to that circuit then sleep signal becomes low than transistors with Sleep and Sleep bar input is high threshold voltages are used to turn ON inactive mode condition and connect to power supply (VDD) and ground to the low threshold voltage. Leakage current is cut OFF to the low V_t circuit in standby mode condition. The leakage of sub threshold in standby mode is diminished by high threshold transistors through undo the low threshold transistors from straight connection to (VDD) and (VSS). While the circuit gives high threshold V_t is turned ON causing low threshold V_t to be implemented in active mode condition. This type of implementation is shows extremely changed parameters as adorn in simulation results. Figure 3 represents CMOS based 4T Schmitt Trigger using MTCMOS technique as shown. Transistor P1 is a sleep transistor and transistor N4 is sleep bar transistor. These two transistors provide by MTCMOS technique and rest of the part is conventional 4T Schmitt trigger circuit. Transistor P1 is attached to the virtual VDD of conventional 4T Schmitt trigger and transistor N4 is connected to virtual GND. When low input signal is applied in proposed circuit sleep transistor P1 is OFF condition and sleep bar transistor N4 is ON means working condition. Alternately, high input signal is claim in circuit P1 is ON and transistor N4 is OFF (standby) condition.

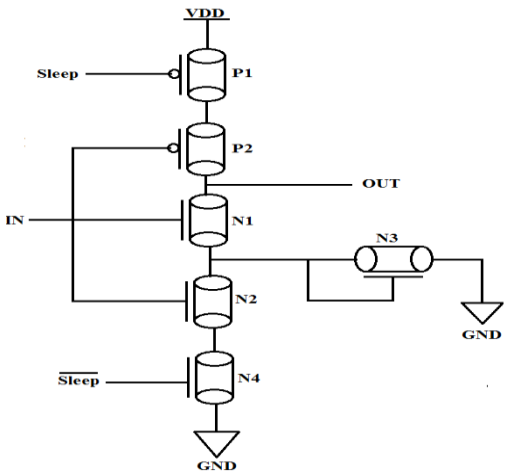

Figure 4: CNTFET 4T Schmitt Trigger Using MTCMOS

Figure 4 represents CNTFET based 4T Schmitt trigger using MTCMOS technique. We have to replace CMOS transistors by CNTFET transistors because it can work in nanometeric condition and reduced sizes of the circuit and reduced power consumption as compare to CMOS circuit.

IV. SIMULATION AND RESULTS

The proposed 4T Schmitt trigger circuits were simulated using SPICE tools in 32nm technology and their transient analysis or hysteresis curve waveform is acquired at 1v power supply. Figure 5 represents the simulation waveform of CMOS based Schmitt trigger employ MTCMOS technique.

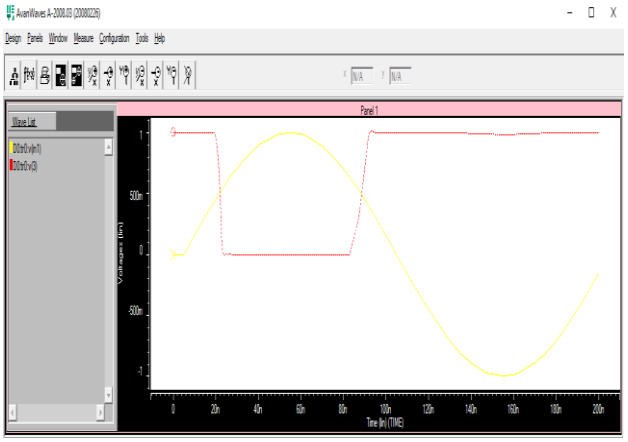

Figure 5: Simulated Waveform of CMOS Schmitt Trigger Operate MTCMOS Technique

In case of figure 6 illustrate hysteresis curve waveform of CMOS Schmitt Trigger using MTCMOS Technique. When we operate MTCMOS Technique in CMOS build Schmitt Trigger to obtain hysteresis loss is 21mV.

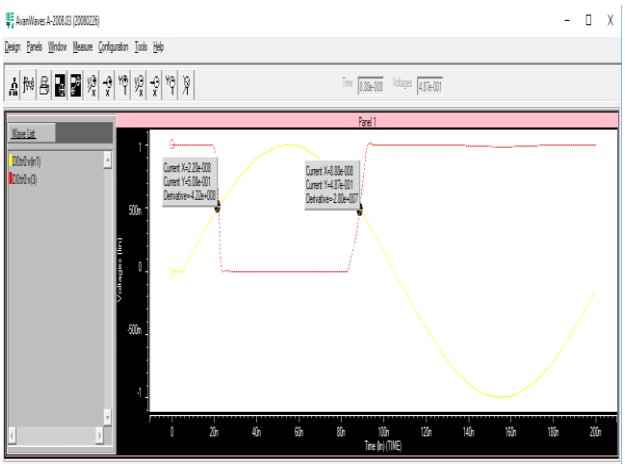

Figure 6: Hysteresis Curve Waveform of CMOS Schmitt Trigger Operate MTCMOS Technique

Similarly, figure 7 represents simulated waveform of CNTFET based Schmitt Trigger use of MTCMOS Technique. In case of figure 7 clearly seen to better waveform result in comparisons of CMOS waveform.

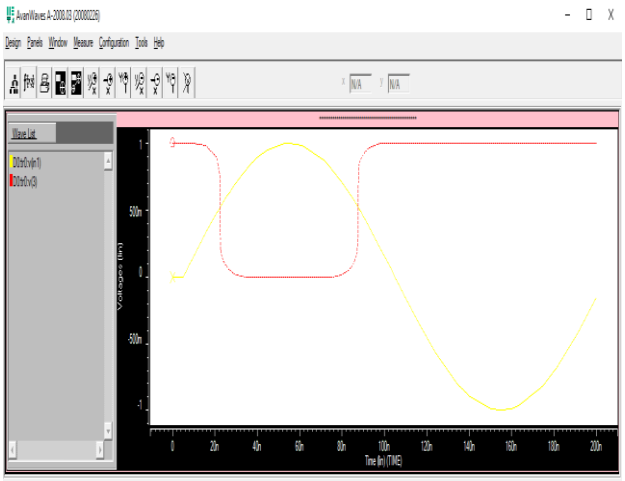

Figure 7: Simulated Waveform of CNTFET Schmitt Trigger Operate MTCMOS Technique

Finally, figure 8 illustrate the waveform of hysteresis curve of CNTFET based Schmitt Trigger using MTCMOS Technique. Operate MTCMOS Technique in CNTFET form Schmitt Trigger to get minimum hysteresis loss is 17mV.

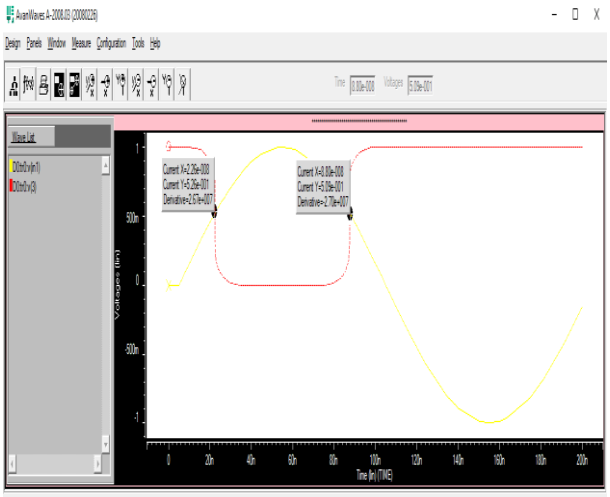

Figure 8: Hysteresis Curve Waveform of CNTFET Schmitt Trigger Operate MTCMOS Technique

Table 1 Represent a Relative Analysis of Both CMOS and CNTFET Schmitt Trigger Using MTCMOS Technique.

Performance Parameters	CMOS based ST	CNTFET based ST	CMOS based ST using MTCMOS	CNTFET based ST using MTCMOS
Technology	32nm	32nm	32nm	32nm
Supply Voltage	1V	1V	1V	1V
Leakage Power	149.82pW	107pW	10.36pW	2pW
Leakage Current	149.82pA	107pA	10.36pA	2pA
Hysteresis loss	360mV	130mV	21mV	17mV
Delay	65.93nS	62.31nS	66.34nS	65.21nS

V. CONCLUSION

Proposed work to be analyzed MTCMOS technique to diminish leakage power, leakage current and hysteresis loss in CNTFET based Schmitt trigger circuit over CMOS based circuit. This power reduction technique provides diminish standby leakage, without any remarkable results on the structure performance. As a result of superior gadget quality of CNTFET based Schmitt trigger in low voltage operation. These power reduction technique is becomes a most favorable for lower VDD operation in CNTFET technology. A relative analysis of CMOS as well as CNTFET to diminish leakage power, leakage current and hysteresis loss in proposed circuit perform in standby mode. MTCMOS technique to be applied in proposed circuit to get quick operation speed to apply low power supply voltage.

Proposed circuits are design and simulated using SPICE tool in 32nm technology at 1V. Power consumption in CNTFET based Schmitt trigger using MTCMOS technique is 2pW and hysteresis loss is 17mV. Propagation delay in Schmitt trigger based CNTFET technology using MTCMOS technique is little bit more than conventional circuit is 65.21nS but the vital concept of this proposed work to diminish power consumption and better efficiency of that circuit. So that CNTFET Schmitt triggers using MTCMOS technique get better results in comparison of other conventional circuits.

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