Design and Analysis of (2x1) and (4x1) Multiplexer Circuit in Quantum dot Cellular Automata Approach

Aishwarya Tambe, Snehal Bhakre, Sankit Kassa

Abstract: ***The scaling of the widely used CMOS technology is reaching its boundaries now. We are in need of new emerging nanotechnologies. Quantum dot Cellular Automata is one such of the top emerging technologies. This technology assures low power and high speed for assembly of logic circuits at nano-scale. One of such important logic circuit is Multiplexer. In this paper, the design of quantum dot cellular automata based (2x1) and (4x1) Multiplexer is presented. The proposed design saves upto 63.15% number of QCA cells and 66% of area compared to previous design approaches. The designs are simulated using the QCADesigner 2.0.3 software.***

Index Terms: Multiplexer, QCA cell, simulation, technology

I. INTRODUCTION

The scaling of CMOS transistors has driven the tremendous growth of the semiconductor industry for the last four decades [2]. However, this scaling limits are reaching to its end now which leads in discovering new ways and technologies to overcome this scaling problem. Quantum dot Cellular Automata is a technology which can overcome this barrier of scaling. Basically, QCA is array or wire of cells which store information using electrons.

QCA cell is the fundamental unit of QCA technology. It is created with four quantum dots positioned at the vertices of a square [8]. This cell contains two electrons which take position diagonally because of columbic repulsion. In this paper the design and simulation of a proposed (2x1) and (4x1) multiplexer using QCA is presented.

II. DESCRIPTION

A. QCA Cell

This technology is based upon cells [1]. Each cell has two electrons and four wells in which this electrons are stored as shown in figure 1. In between these wells tunnels are present for movement of these electrons from one well to another. However, due to coloumbic repulsion these electrons acquire two states only. These state are logic 0 and logic 1.

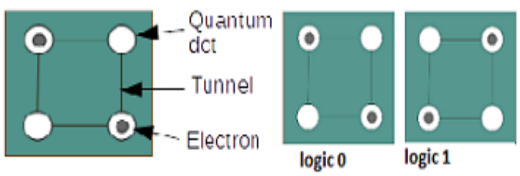

Figure 1: QCA cell and its logic

B. Basic Gates

1) MAJORITY GATE:

The majority gate is the most crucial gate of QCA. It consists three input and one output as shown in figure 2. As the name says, in this gate output is dependent on the majority of similar logic state of the inputs. Furthermore, we can construct logic gates AND and OR using majority gate and with fixed polarization. When this polarization is fixed as 0 majority gate acts as AND gate and when it is fixed to 1 it acts as OR gate. The equation for majority gate is given as follows:

'Y=AB+BC+AC' (1)

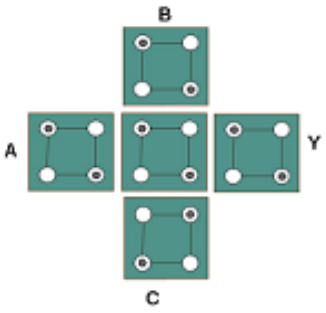

Figure 2: Majority gate

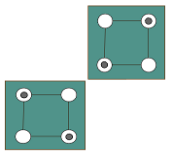

Figure 3: Inverter

2) INVERTER:

The inverter gate is basically not gate which is designed using QCA cell by adjusting two cells inverse to each other (as shown in fig 2). Due to such placing, the inverted output of input is obtained thus, an inverter.

C. CLOCKING:

Clocking provides path to quantum dots for transfer of electrons between the dots. Each QCA cell goes through four stages in one clock cycle. This stages are named as switch, hold, release and relax states.

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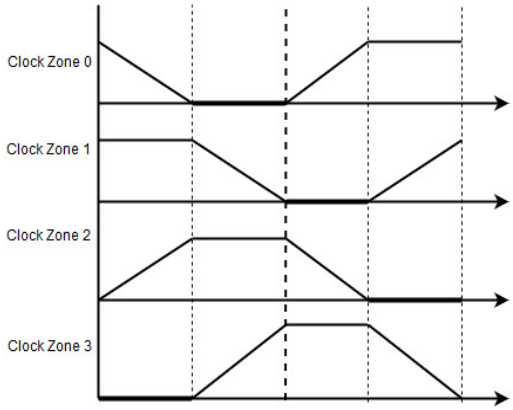

Figure 4: Clock zones in QCA

III. IMPLEMENTED DESIGN OF MULTIPLEXER USING QCA

A. MULTIPLEXER:

Multiplexer is a circuit with digital combinations. Among multiple data inputs, one or more are select inputs. Only one combination of inputs is selected as output. Signals are passed from one of the inputs to output.

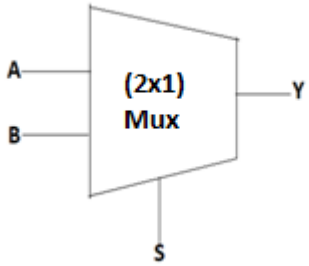

Figure 5: Multiplexer

B. IMPLEMENTED (2X1) MULTIPLEXER

The (2x1) Multiplexer consists two inputs , one selection line and one output line as shown in figure 5.

The equation for (2x1) Multiplexer is:

$$Y = AS' + BS \quad (2)$$

The truth table for (2x1) Multiplexer is as follows:

Table .1: Truth Table for (2x1) multiplexer

S	A	B	Y
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

The schematic for proposed design of (2x1) multiplexer is shown in figure 6 whereas the layout for proposed design of (2x1) multiplexer is shown in figure 7. The logic diagram is shown in figure 8.

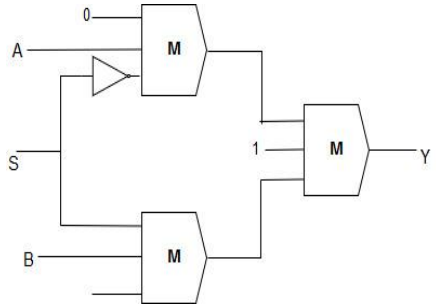

Figure 6: Schematic of (2x1) Multiplexer

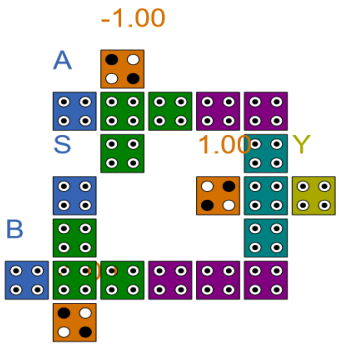

Figure 7: Proposed (2x1) Multiplexer Layout

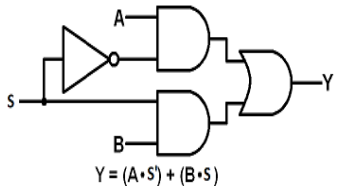

Figure 8: Logic Diagram of (2x1) Multiplexer

The output for the layout of (2x1) Multiplexer using QCA simulation software is presented in figure 9.

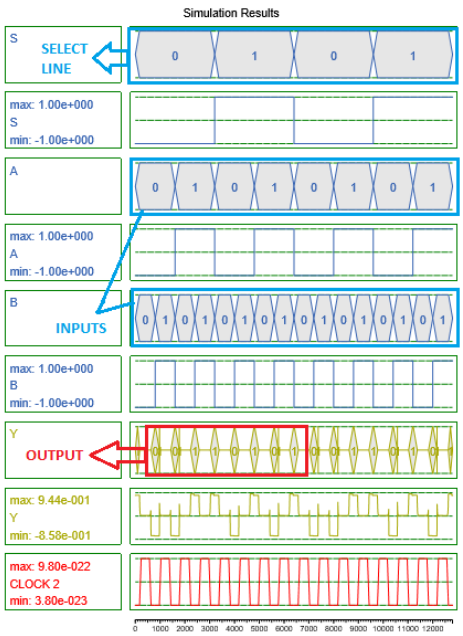

Figure 9

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IV. (4X1) MULTIPLEXER

The (4x1) Multiplexer consists of four inputs, two selection line, one output line.

The equation for (4x1) Multiplexer is:

$$Y= A.S0'S1' + B.S0'S1+ C.S0'S1+ D.SOS1 \quad (3)$$

The truth table for (4x1) Multiplexer is as follows:

Table 2: Truth Table for (4x1) Multiplexer

SELECT LINES		INPUTS				OUTPUT
S0	S1	A	B	C	D	Y
0	0	A	0	0	0	A
0	1	0	B	0	0	B
1	0	0	0	C	0	C
1	1	0	0	0	D	D

The schematic and layout in QCA for proposed (4x1) Multiplexer is as shown in figure 10 and 11 respectively.

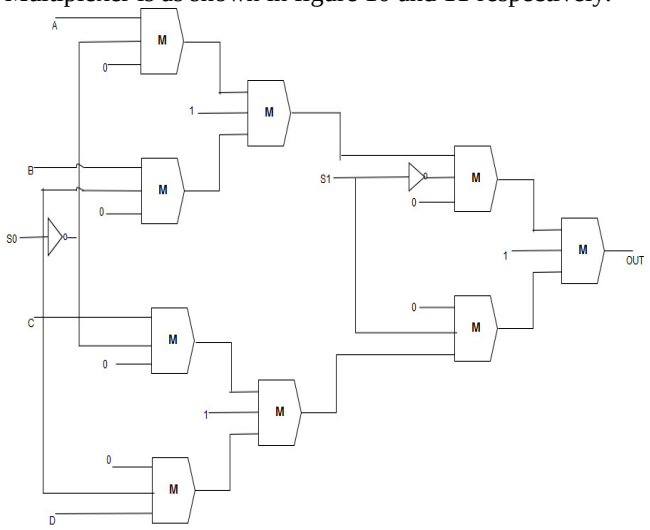

Figure 10: Schematic of (4x1) Multiplexer

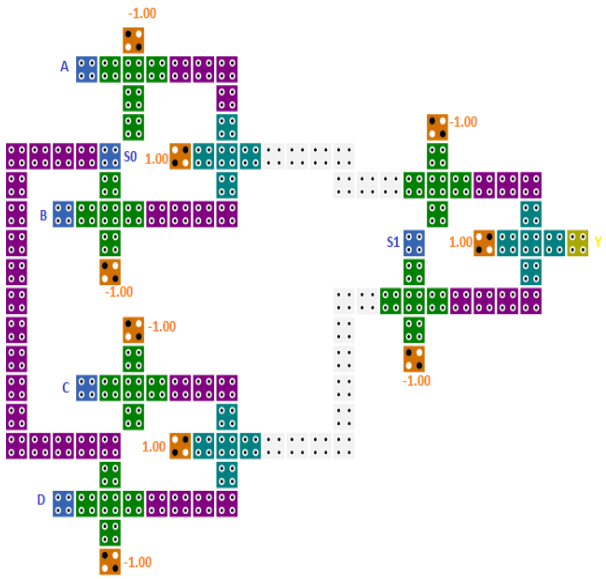

Figure 11: Layout for (4x1) Multiplexer

The output for the layout of (4x1) Multiplexer using QCA simulation software is as shown in figure 12.

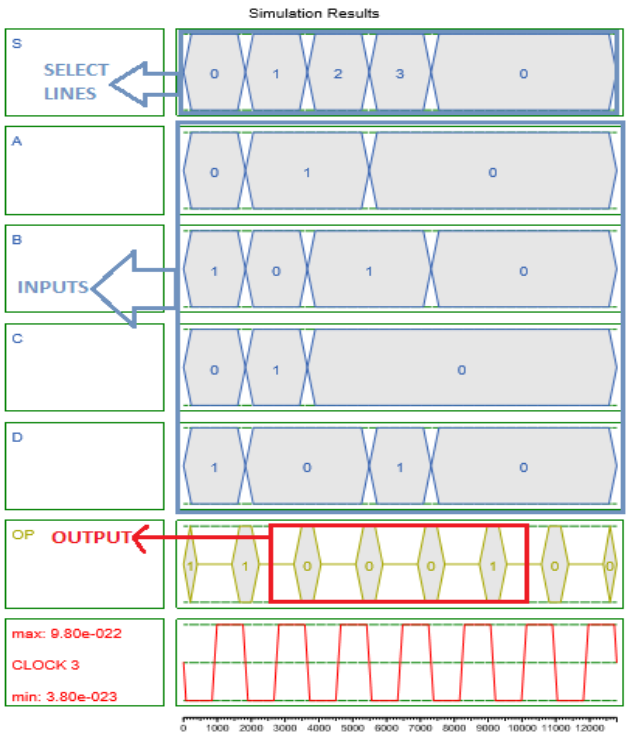

Figure 12: Output of (4×1) Mux

V. COMPARISON WITH PREVIOUS DESIGNS

The various designs which have been designed previously have been taken into consideration. The proposed (2x1) and (4x1) Multiplexer is compared with previous designs. Figure 13 shows few such different designs. Table 3 shows comparison of these designs with proposed design.

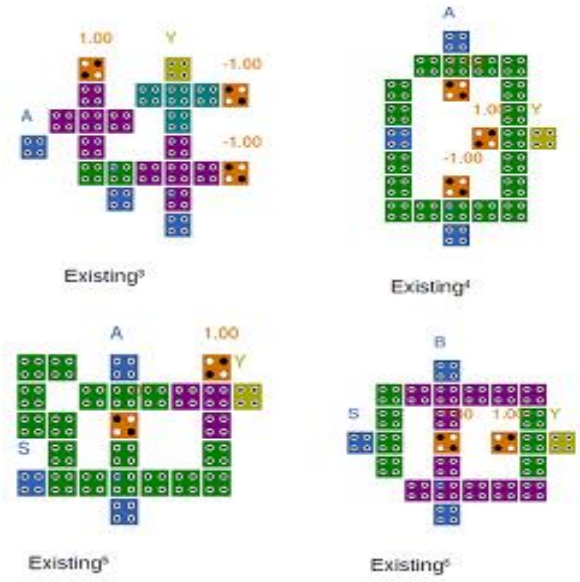

Figure 13: Some existing designs

Table no. 3: Comparison of (2x1) and (4x1) with previous designs

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VI. RESULTS AND DISCUSSION

Proposed QCA (2x1) Multiplexer	Number of majority gate used	No. of QCA cell	Total Area(nm^2)	Cell Area (nm^2)	Area usage %	Clocking zone
Proposed	3 majority gate	21	24164	6804	28.15	3
Existing 3	3 majority gate	23	18144	7452	41.07	3
percentage reduction w.r.t 3		8.69	33.17	8.69	-12.9	0
Existing 4	3 majority gate	25	21600	10000	46.29	3
percentage reduction w.r.t 4		16	11.87	31.96	-18.1	0
Existing 5	3 majority gate	26	15552	8424	54.16	2
percentage reduction w.r.t 5		19.23	55.37	19.23	-26	33.33
Existing 6	3 majority gate	27	23328	8748	37.5	3
percentage reduction w.r.t 6		22.22	3.58	22.22	-9.37	0
Proposed QCA (4x1)						
Proposed	9 majority gate	118	202104	38232	18.91	4
existing 3	9 majority gate	130	101952	41874	41.07	4
percentage reduction w.r.t3		9.24	98.23	8.7	-22.2	0
existing 4	9 majority gate	141	121372	56191	46.29	4
percentage reduction w.r.t 4		16.32	66.51	31.97	-27.4	0
existing 5	9 majority gate	146	87388	47335	54.16	4
percentage reduction w.r.t 5		19.18	131.27	19.23	-35.3	0
existing 6	9 majority gate	152	131082	49156	37.5	4
percentage reduction w.r.t 6		22.37	54.18	22.23	-18.6	0

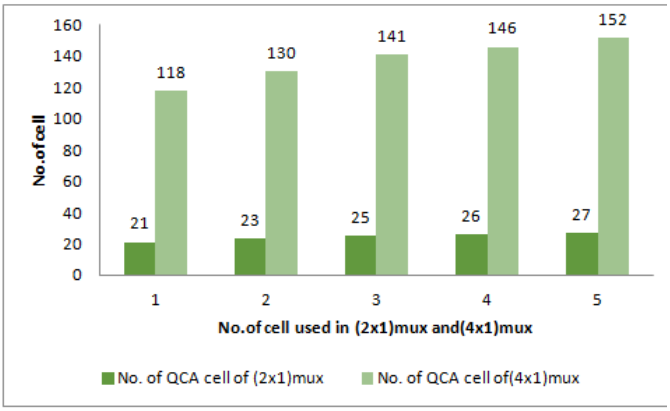

Figure 14 : No. of cells utilised by (2x1) and (4x1) multiplexer

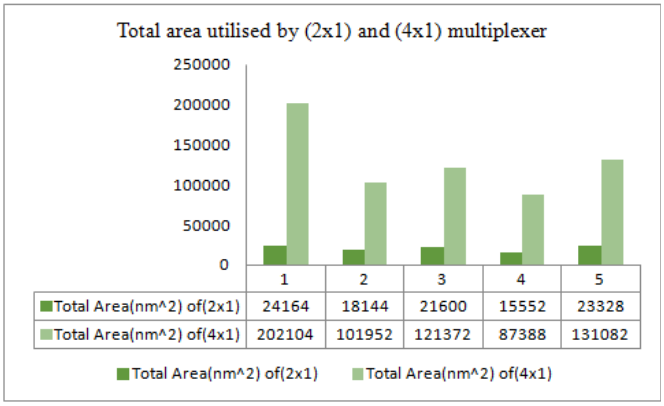

Figure 15: Total area utilised by (2x1) and (4x1) multiplexer

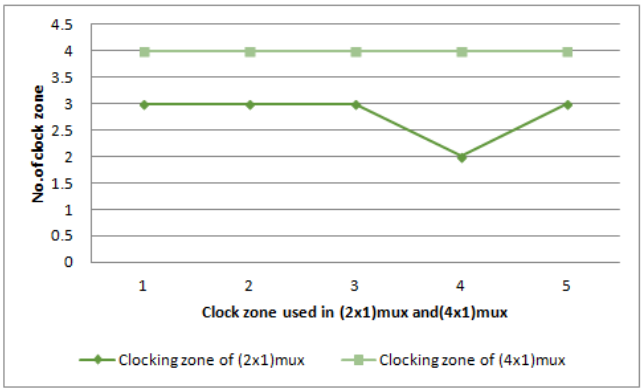

Figure 16: Clock zones used by (2x1) and (4x1) multiplexer

The schematic and layout in QCA for proposed (2x1) Multiplexer is presented in figure 6 and 7 respectively. Figure .9 gives the simulation result of proposed design of (2x1) Multiplexer. Similarly, the schematic and layout in QCA for proposed (4x1) Multiplexer is given in figure 10 and 11 respectively. Figure 12 presents the simulation result of proposed design of (4x1) Multiplexer. These results are confirmed with the original truth table. From table 1, it can be observed that when S=0, then output is A and when S=1 then output is B. From table 2, it is observed that when S0= 0 and S1=0 the output is A. When S0=0 and S1=1, then the output is B. When S0=1 and S1=0 then output is C. When S0=1 and S1=1 then output is D. Table 3 describes the detailed comparison of proposed Multiplexer with previous designs. Figure 14 depicts the number of QCA cell required by proposed design compared to other designs. Figure 15 describes the graph of total area utilized. Figure 16 represents the number of clock zones used in each design. Table 3 clearly states that proposed (2x1) Multiplexer requires 3 majority gates, 1 inverter, 3 clock zones and total number of cells used are 21. Detailed comparative study with previous designs is explored in table 3. The proposed (4x1) multiplexer is designed using the proposed (2x1) multiplexer. According to the comparison, it can be observed that the proposed Multiplexer has 63.15% reduced cell count than that of existing designs. The implementation and simulation of proposed design is completed using QCA designer.

VII. CONCLUSION

Multiplexers are required in many coherent and functional circuits. This paper represents an innovative design of a Multiplexer in QCA. The proposed designs are efficient in terms of overall area and cell count. The proposed design saves up to 63.15 % number of QCA cells and 66 % of area compared to previous design approaches. This circuit can also portray a crucial role in the area of digital nano communication for signals encoding in near future.

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