Investigation of Junction-less Double Gate MOSFET With High-k Gate-oxide and Metal Gate Layers

Ambika, Gaurav Dhiman

Abstract: ***With the development of Moore's law, the size of the transistors is decreasing so fast which led to various effects like leakage current and short channel effects(DIBL, low threshold voltage etc). With the scaling, the performance of device degrades, so to improve the performance of the device multi-gate architectures can be used. It improves the control of gate over channel increases and it also provides ideal sub-threshold swing and better ION/IOFF ratio. Generally, SiO2 is used as oxide material in metal oxide semiconductor field effect transistors (MOSFET) but it leads to high leakage current and direct tunneling of electrons. So in this paper to overcome all these problems SiO2 is replaced by high-k dielectric materials (HfO2, Al2O3, ZrO2). High-k materials provide high density and low energy consumption. In this paper, the study of n-type JL-DG MOSFET with high-k dielectric oxide materials and all results were compared with SiO2 material layer.***

Keyword: DIBL, JL-DG MOSFET, SCEs, etc

I. INTRODUCTION

Conventional CMOS transistor has been a very important component in very large-scale integration technology for the past four decades, but in semiconductors due to short-channel-effects (SCEs) like a drain- induced-barrier-lowering (DIBL), threshold voltage roll-off and sub-threshold swing and gate tunneling these transistors are approaching their fundamental physical limits. As an alternative multiple-gate- MOSFETs have been proposed to conventional CMOS mainly because of their robust electrostatic control. Junctionless MOSFET (JLMOSFET) do not have any pn junction in the source-drain channel path can be scaled to very low channel length because of the lower SCEs and easy fabrication steps. It has homogeneous and uniform doping throughout the source- channel-drain, unlike a junction-based (JB) inversion mode (IM) transistor. But when a device is scaled down to sub-nano-scale the fabrication becomes difficult for junction based device. So new device junction less MOSFETs are designed to avoid these problems. Scaling of gate-oxide layers led to the reduction in the thickness to around 1 nm which results in large leakage currents

A JL-DG MOSFET demands high channel doping concentration in the channel region to achieve an acceptable threshold voltage. Despite its high doping concentration, JL MOSFET has comparable drain current as JB device. Therefore JL MOSFET can be a possible candidate for substitution to conventional multi-gate MOSFET in ultra short channel length regime.

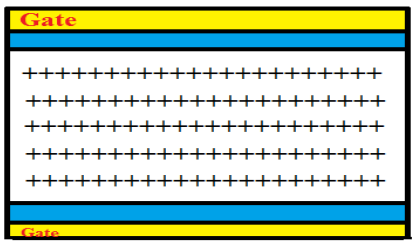
Scaling of gate-oxide layers led to the reduction in the thickness to around 1 nm which results in large leakage currents. So silicon dioxide (SiO_2) is replaced by high dielectric constant material like hafnium oxide (HfO_2) and zirconium dioxide (ZrO_2) is important.

This paper compares the design of junctionless double gate MOSFET (JL-DG MOSFET) silicon dioxide and high-k material as gate-oxide layers at 22 nm technology. In this work, the performance of JL-DGMOSFET due to high-k gate dielectrics on JLMOSFET performance are studied for improvement of on current to OFF current ratio (I_{ON}/I_{OFF}), DIBL, sub-threshold swing, and transconductance. The effect of variation of the carrier concentration of the metal gate on the parameters of devices is also studied. It is observed that JL-DG MOSFET with high-k oxide layer has better I_{ON}/I_{OFF} ratio, better DIBL, and sub-threshold swing (SS) parameter[2][3][6].

II. OPERATION OF JL-DG MOSFET

A. Depletion mode

In depletion mode as shown in fig.1 when the threshold voltage(V_{th}) is larger than the voltage between gate to source (V_{gs}) than at that time the channel is fully depleted and the device is turned off. Under this condition no channel appearance between source and drain.



(a) Vgs < Vt

Fig. 1 OFF condition of JL-DG MOSFET

B. Bulk current mode

In bulk current mode as shown in fig. 2 that when threshold voltage is lesser than the voltage between gate to source (V_{gs}) but is less than flat band voltage (V_{fb}) than the channel is partly depleted and in the core of the channel a small bulk current starts to flow from drain to source[2].

Revised Manuscript Received on April 12, 2019.

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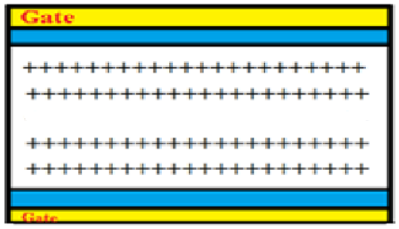
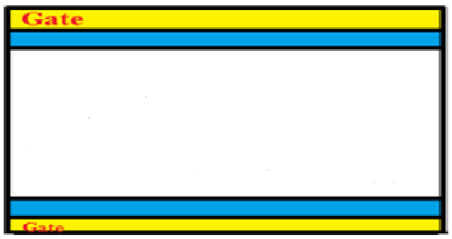


(b) Vgs > Vt

Fig 2. Bulk mode of JLMOSFET

C. Flat-band mode

In flat band condition as shown in Fig. when the voltage between gate to source (V_{gs}) is equal to flat band voltage than the device operates in flat-band mode. The channel region of the device is now completely unbiased. Under this bias condition, the JLT is fully turned on. The dominant conduction mechanism is a bulk current.



(c) Vgs = Vfb

Fig 3 Flat band mode of JLMOSFET

D. Accumulation mode

As shown in Fig. 4 when the gate to source voltage (V_{gs}) become greater than flat band voltage at this condition, under the silicon boundary charge carriers are collected. This is not right for favorable device operation, since the charges which accumulate under the surface it cause surface and scattering at the oxide interface, as the result of this the mobility of the carriers reduces and therefore the output current of the device[2].

(d) Vgs > Vt

Fig 4. Accumulation mode of JLMOSFET

III. RESULT AND DISCUSSION

As shown in fig.5 JL-DG MOSFET is simulated by using ATLAS simulator and here as gate-oxide materials, high-k materials are used[7]. The propose JL-DG MOSFET device with high-k materials as gate-oxide has the channel length (L) of 22 nm, the channel thickness (t_{si}) of 10 nm, gate-oxide thickness (t_{ox}) of 2 nm. And the gate work function is taken as 5.0eV.[5]

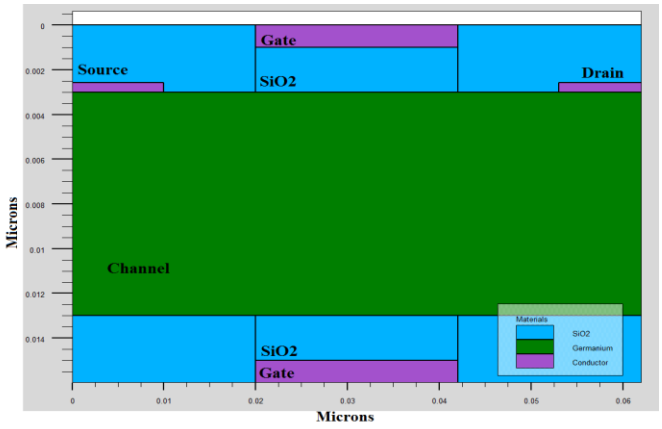


Fig. 5 Tony-plot of JL-DG MOSFET

A. I_{OFF}

OFF current in a device is that current when a gate voltage is equal to zero(V_G=0) and at that time any current flow in the device in called I_{OFF} current of the device. This current is also called leakage current in the device. This current effects the performance of the model.

The variation of I_{OFF} is shown in figure 6 with carrier concentration and it is observed that high-k dielectric materials results smaller I_{OFF} as compare to SiO_2 for all range of carrier concentration. This is due to strong electrostatic behavior of JL-DG MOSFET. And among all the high-k materials HfO_2 shows the smallest $I_{OFF.}$

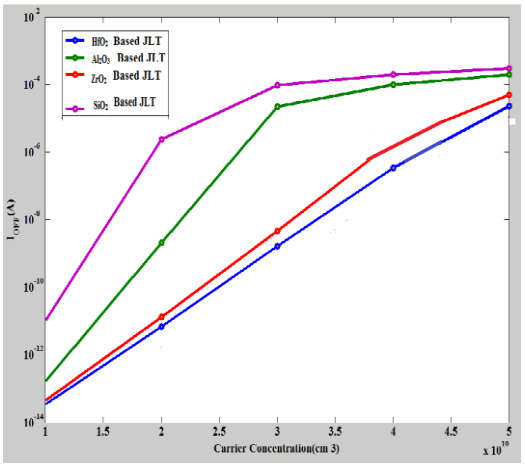


Fig.6 Variation of I_{OFF} with the carrier concentration

B. I_{ON}

When the applied voltage is more than the Threshold Voltage the device starts working in ON condition, in this condition current following through the device is called ON current.

Figure 7 shows the variation of I_{ON} with carrier concentration and it is observed that high-k materials show higher I_{ON} as compare to SiO_2 .And among all the high-k materials HfO_2 shows the highest $I_{ON.}$

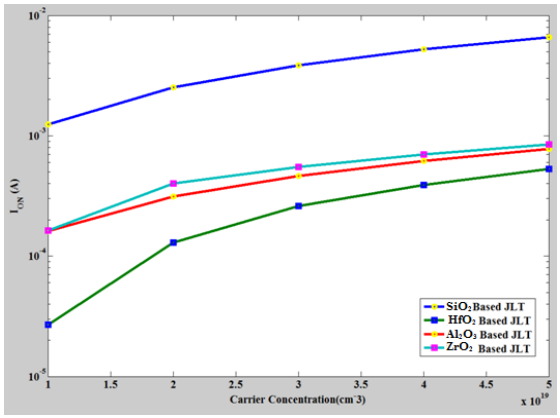


Fig.7 Variation of I_{ON} with the carrier concentration

C. I_{ON} / I_{OFF}

I_{ON}/I_{OFF} is directly proportional to the gate control on the circuit, so if gate control increases I_{ON}/I_{OFF} also increases. I_{ON}/I_{OFF} leads to the high performance of the device and for low leakage power in the CMOS circuit.

Figure 8 shows the variation of I_{ON} / I_{OFF} with carrier concentration and it is observed that SiO_2 has smaller I_{ON} / I_{OFF} ratio as compare to high-k materials.HfO_2 gives better I_{ON} / I_{OFF} ratio among all the high-k materials. This is due to strong depelation of a channel with higher barrier potential in HfO_2 devices.

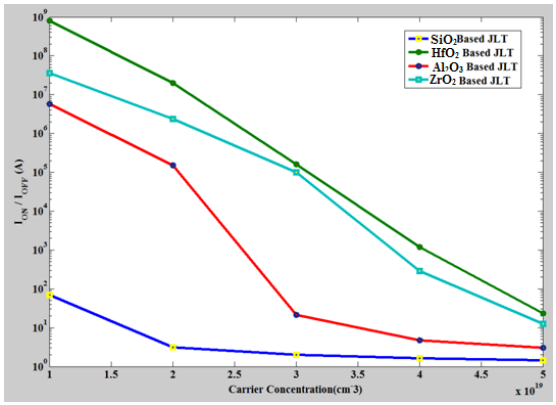


Fig.8 Variation of I_{ON} / I_{OFF} with the carrier concentration

D. Threshold voltage(V_{th})

The threshold voltage of a MOSFET is usually defined as the gate voltage (V_g) where an inversion layer forms at the crossing point between the insulating layer (oxide) and the substrate (body) of the transistor. The reason for the creation of the inversion layer is to permit the flow of electrons through the gate-source junction. The minimum voltage needed to ON the transistor is called V_{th}.

Figure 9 shows the comparison of threshold voltage (V_{th}) between SiO_2 and other high-k gate-oxide materials. The variation of V_{th} with carrier concentration for SiO_2 and high-k materials gate-oxide materials shows high-k materials have high V_{th} as compare to SiO_2, and among all the high-k materials HfO_2 shows highest V_{th}.

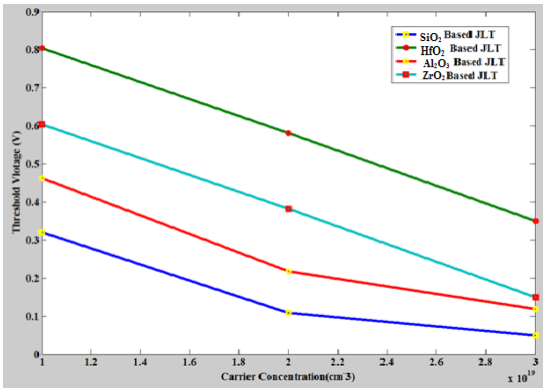


Fig.9 Variation of threshold voltage with the carrier concentration

The variation of drain voltage with drain current at gate-oxide thickness for different materials is shown in figure 10. It is shown that HfO_2 has better performance among all the other materials. This makes the design more flexible with different gate-oxide thickness.

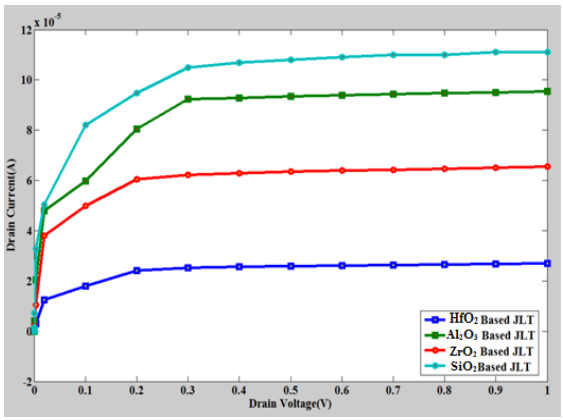


Fig. 10 Variation of drain voltage with a drain current

E. Drain-Induced Barrier Lowering (DIBL)

DIBL is the most important SCEs which generate because of decreasing the size of the device. The gate voltage is the only voltage which controls the device. This effect is better understood when to go from source to drain the electron has to overcome the potential barrier profile. Under ordinary conditions (V_{ds}=0 and V_{gs}=0), there is a potential barrier that stops the electrons flowing from source to drain. The gate voltage has the utility of lowering this barrier down to the point where electrons are able to flow. Ideally, this would be the only voltage that would affect the barrier. But when the channel length becomes small, drain starts to behave like a second gate. Drain current (I_D) is controlled by both gate voltage and drain voltage. When the channel length is long in a device, then an increase in V_{DS} decreases band only in the drain terminal side. But, when channel-length decrease, this leads to an increase in V_{DS} and decrease the source to channel barrier. Due to the effect of DIBL threshold voltage decreases. Low V_{th} increases the OFF current of the device. There are many ways to control DIBL-

a) By decreasing the oxide thickness, the increase in the gate can be controlled, which increase the tunneling current through gate-oxide.

b) By increasing the doping of the substrate, which keeps the drain and source apart by decreasing the widths of the depletion region.

c) Instead of Si, by using low dielectric material the drain coupling to a source is reduced.

In table 1 DIBL of SiO_2 is compared with all high-k materials and it is observed that high-k materials have very less DIBL as compare to SiO_2. And among all high-k materials, HfO_2 has the smallest DIBL.

Table 1 Performance comparison of DIBL with the carrier concentration

S.No.	Material	Carrier Concentration(cm^{-3})	DIBL
1	HfO_2	1e19	0.0049
		2e19	0.0131
2	Al_2O_3	1e19	0.0300
		2e19	0.0372
3	ZrO_2	1e19	0.0152
		2e19	0.0179
4	SiO_2	1e19	0.0769
		2e19	0.2069

IV. CONCLUSIONS

In this paper, the performance of the junctionless double gate tunnel has been studied. And this is observed that replacement of SiO_2 with high-k dielectric materials as the oxide layer in JL-DG MOSFET is very important for semiconductor devices. When SiO_2 oxide layer is compared with high-k oxide layer materials it is shown that it reduces the short channel effects (DIBL) in the device, low DIBL enhance the performance of a device under high drain bias. It also reduces I_{OFF} current and increases the threshold voltage. The I_{ON} / I_{OFF} ratio for high-k materials is far better than SiO_2. At different carrier concentration, it was found that high-k materials have better control over channel due to better electrostatics. And among all high-k materials, HfO_2 shows that better results as compared to others..

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Ambika was born in Chirawa,, India in 1995. She received the B.Tech degree in Electrical and Electronics engineering from Mody University of Science and Technology (MUST) Lakshmangarh, Rajasthan, India, in 2016 and perusing M.Tech degree in VLSI design from Mody University of Science and Technology (MUST) Lakshmangarh, Rajasthan. Her research interest includes semiconductor device modeling, Microcontrollers.

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