A Novel Low Power MUX based Dynamic Barrel Shifter using Footed Diode Domino Logic

Bharathesh Patel N, Manju Devi

Abstract— The choice of the Complementary Metal Oxide Semiconductor logic to be used for implementation depend on the given specified optimization and the performance constraints that the finished chip is required to meet. Dynamic logic provides better performance for higher fan in and complex logic circuits and also with the increasing level of integration, high speed and low power dissipation have become the mandatory requirements for any logic design along with the performance.

Many design logics are available within Dynamic Logic stream. One of the popular logic is the Domino logic (DL) for low power dissipation and high- speed. This paper presents a comparative study and analysis of Barrel Shifter using Pseudo nMOS multiplexer and Footed Diode Domino (FDD) multiplexer.

Keywords— Domino CMOS circuits, Dynamic Logic, Pre-charge, Evaluation, Barrel Shifter, Pseudo nMOS, charge sharing, Power consumption.

1. INTRODUCTION

A Barrel shifter is a logic circuits extensively used in embedded digital signal processors as well as in general purpose processors to manipulate the data as rotating and shifting information is required in a few fields including bit-indexing, arithmetic tasks and variable-length coding. Several patents and copyrighted research articles efficient designed and implementation for barrel shifters [1-2].

A shifter is designed to shift and rotate the data by specified number of bits logically or arithmetically either left or right. With the increasing level of integration there is always a need to reduce the delay of operation and reduction in the power consumption. This paper presents 2 different designs of Barrel shifter using multiplexer and dynamic multiplexer and compares both in terms of power and delay [3-6]

Pseudo nMOS rationales are the most widely recognized type of CMOS ratioed rationale which Provides high speed for large fan in circuits but suffers from static power consumption [7]

Dynamic logic is widely used in high performance microprocessors and is attractive for high speed circuits as compared to static logic. Dynamic circuits use fifty percent of transistor check concerning integral static circuits. Domino reason networks are high power effective & co-operatively quicker [8]. Domino method of reasoning is on a very basic level a dynamic basis network sought after by a static inverter & capacitor as a stack. Dynamic rationale circuit yield is put away in the capacitor, it is associated next beyond the static inverter. The task of domino rationale circuit controlled by clock flag. Footed Diode Domino rationale is one of the domino rationale which defeats the issue of debasement of execution because of proliferation of pre-charge beat.

A. Shift & Rotate Tasks

In this report, the input operand as denoted X and W defined as shift/rotate operation and Y denoted as shifted/rotated output result. X is defined as an m-bit esteem, m term is a number intensity of 2. Consequently, W is a logarithm of 2(m) bit number speaking to values from 0 to m-1.The bi-directional barrel shifters introduced here can perform six unique tasks: shift right arithmetic (SRA), shift right logical (SRL), rotate left(RL),shift left logical(SLL), shift left arithmetic(SLA), & rotate right(RR).

Table 1 gives a case of these tasks. In this input vector X is signified as x7x6x5x4x3x2x1x0 and the S/R sum W is a 3 bit vector indicated as b2b1b0 and the yield vector is meant as y7y6y5y4y3y2y1y0 and Table 2 demonstrates the task control bits.

Table I Shift And Pivot Models

Operation	y7y6y5y4y3y2y1y0
3-bit SRL	$000a_7a_6a_5a_4a_3$
3-bit SRA	a7a7a7a7a6a5a4a3
3-bit RR	a2a1a0a7a6a5a4a3
3-bit SLL	$a_4a_3a_2a_1a_0000$
3-bit SLA	$a_7a_3a_2a_1a_0000$
3-bit RL	a4a3a2a1a0a7a6a5

Table II. Operation Control Bits

'Rotate'	'Left'	'Arithmetic'	Task
H	H	X'	RL
L	H	L	SLL
H	L	X'	RR
L	H	H	SLA
L	L	H	SRA
L	L	L	SRL

- SRL task of a W-bit is RS & value 1's the higher W bits of the outcome to 0's.
- SRA task of a W-bit RS & value 1's the higher B-bits of the outcome to xm-1, which relates to the signal piece of X.
- RRA activity of a W-bit RS & value 1's the higher W-bits of the outcome to the lower W-bits of X.
- SLL activity of a W-bit LS & value 1's the lower W bits of the outcome to 0's.

Revised Version Manuscript Received on April 12, 2019.

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Blue Eyes Intelligence Engineering
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- SLA activity of a W-bit LS & value 1's the lower W bits of the outcome to 0's and the signal piece of the outcome is 1's to xm-1.
- RR activity of a W-bit LS & value 1's the lower W bits of the outcome to higher W bits of X.

B. Pseudo nMOS logic

Pseudo nMOS rationales are the most widely recognized type of CMOS ratioed rationale. The draw down system is same as the static entryway however the draw up system has been supplanted with a solitary pMOS transistor which is grounded so it is dependably ON. The basic circuit of Pseudo nMOS Logic is shown in "Fig.2a". [7-12]

The pull-up transistor width is selected to be about 1/4th the strength. The output of n-block can pull down by chosen to conduct a multiple of the n-block's leakage and narrow enough. High speed and lesser transistor count are advantages of pseudo-nMOS logic.

The static power consumption slightly increases with improvement in overall speed. Further, an appropriate control signal connected to gate of all the pull up transistor it can be turned off i.e. with no extra cost power down mode supported by pseudo-nMOS.

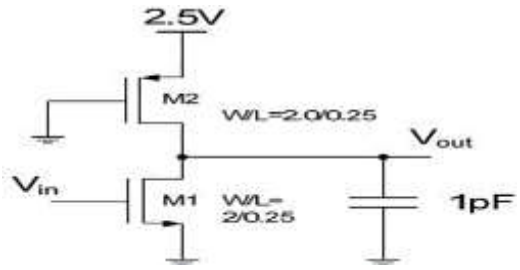


Fig.2a. Pseudo nMOS Logic circuit.

C. Multiplexer based on Pseudo nMOSLogic.

A 2:1 multiplexer can be designed using Pseudo NMOS Logic based on the EX_OR logic. "Fig. 2.1a" shows the gate level & Fig.2.1b represent the schematic of the same. As the circuit produces a complemented output, an inverter Is added at the output side.

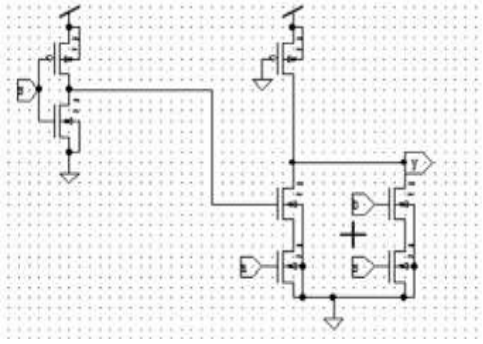


Fig.2.1a. 2:1 multiplexer Circuit.

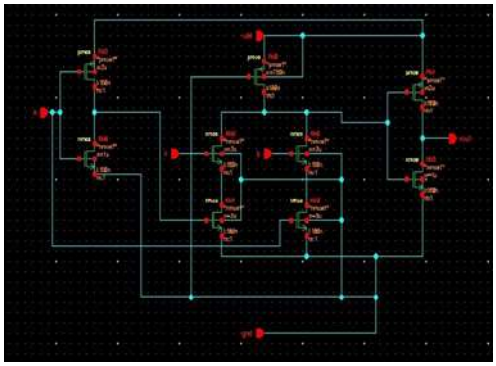


Fig. 2.1b. 2:1 Multiplexer Schematic

D. Dynamic logic

Major objective is to reduce delay and area, due to improves density and performance of digital implementations; static logic circuits have fewer advantages compared to dynamic logic circuit [7-13]. Dynamic circuit uses a clocked pull up transistor rather than a pMOS that is always ON. "Fig.3a" CMOS based dynamic logic circuit. Depend on temporary storage of capacitor will affect the operation of all dynamic logic gates

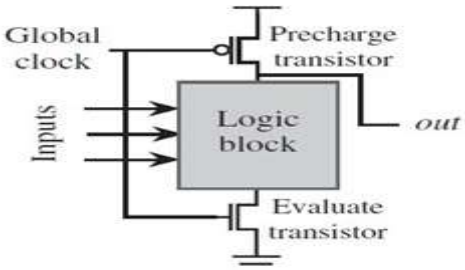


Fig.3a. Dynamic Logic circuit

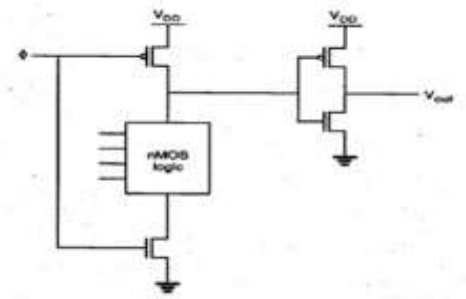
2. DOMINO LOGIC

Domino circuits are executed in high fan-in circuits with rapid task [14]. In any case, domino circuits are risky to noise. Because of exchanging limit voltage the noise affectability of domino circuit's is equivalent to Vth of nMOS in the recreated system. The innovation scaling and considerable increment in profound submicron noise seriously effects the handiness of domino circuits. By innovation scale decline the power utilization by scale down the supply voltage.

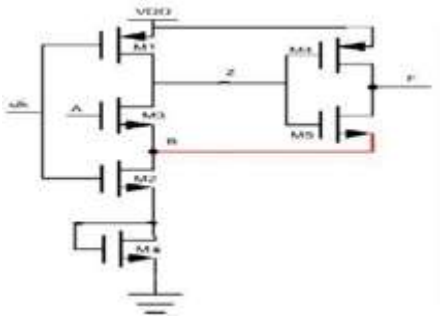
So as to enhance exhibitions a higher drive charge equivalently scaled the transistor edge potential level. Because of high spillage charge, cross-talk, commotion, input clamor & current sharing builds the profound sub-micron clamor level. The sub edge spillage current generously expands edge voltage scaling results. Increments of spillage of the assessment transistors exponentially because of scale down, while expanded crosstalk the commotion at the contribution of the advancement transistors may increments.

Domino circuit execution corrupted due to pre-charge beat from dynamic hub to the yield hub. The Pseudo Dynamic Buffer (PDB) based plan for domino rationale repays this

issue for domino rationale up to some degree [17] yet there is dependably an extension for development. In our proposed Footed Diode Domino circuits we put an NMOS transistors which is filling in as a diode in the middle of Ground & M-2 clocks of transistors [18-20]. Fig.3.1a shows the circuit of Domino rationale and Fig.3.1b shows the Footed diode Domino (FDD) Logic.



"Fig.3.1a" Domino Rationale circuit



"Fig.3.1b" FDD Logic circuit

A. Multiplexer based on FDD Logic

"Fig.3.2a" Represent the schematic of a 2:1 multiplexer using Footed Diode Domino logic. The logic is designed considering the aspects of ratios to adjust resistance of the pull up and pull down network.

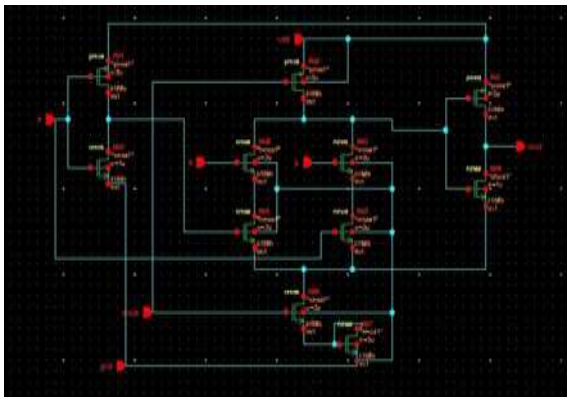


Fig.3.2a.2:1 multiplexer using Footed Diode Domino Logic

B. Barrel Shifter using 2:1 Multiplexer (8 bit)

A right shifter or rotator can be designed with the help of multiplexers as shown in "Fig.4a". Circuit uses cascading of 2:1 multiplexers to get the logic required [3-6]. Circuit performs both right logical, right arithmetic shift operation along with right rotation. "Fig.4b" shows the schematic of the same designed using cadence software.

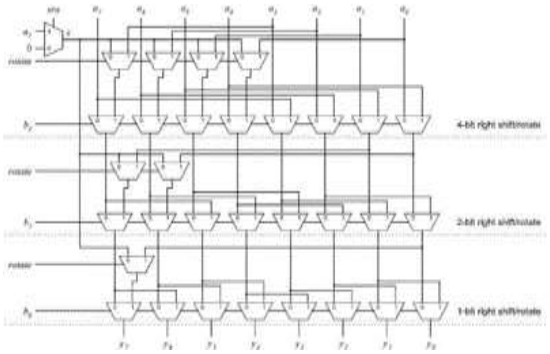


Fig. 4a MUX based right shifter or rotator circuit.

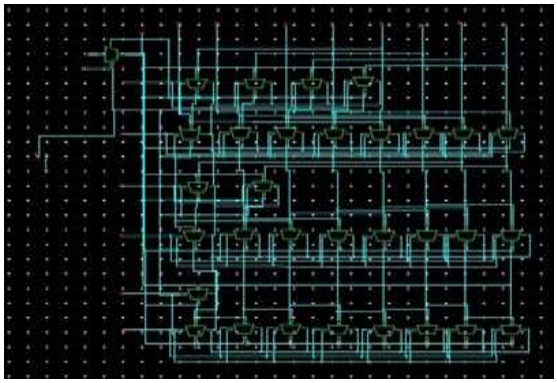


Fig.4b MUX based right shifter or rotator schematic

The complement logic is used to design an 8 bit multiplexer based left shifter or rotator. Both the circuits are combined to design bidirectional 8 bit logical or arithmetic shifter and rotator."Fig.4c" shows the complete bidirectional arithmetic/logical shifter and rotator

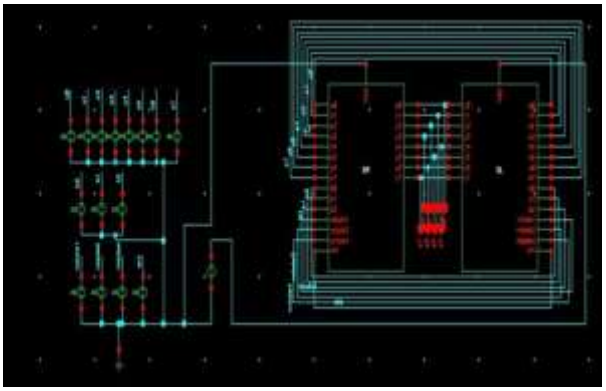


Fig.4c 8 bit barrel shifter Schematic

3. RESULTS AND ANALYSIS

The circuits are designed on cadence tool using 180nm technology files. Table 3 compares the results of both logics for 2:1 multiplexer regarding improvement of deferral, structure power and power postpone item (PPI). "Fig.5a","Fig. 5b" shows the analysis for the same.

Table III Performance Analysis of MULTIPLEXER

Architecture Design	Delay in 'us'	Power in watts 'W'	Power Delay Product in 'J'
Pseudo nMOS Logic	20.00	162.6E-6	3.232E-9
Footed Diode Domino	64.10	40.17E-9	2.575E-12

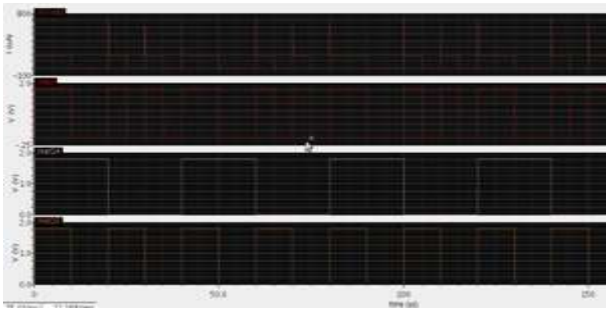


Fig.5a. Analysis of using pseudo nMOS Logic Multiplexer

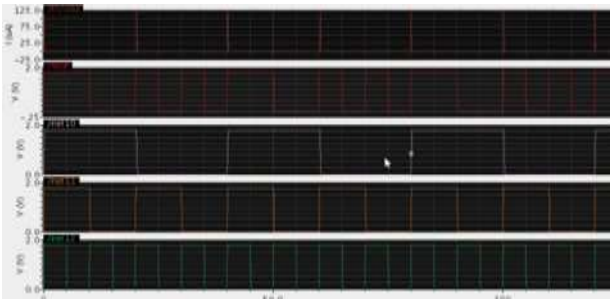


Fig.5b. Analysis using FDD Multiplexer

Barrel shifter is designed using the above discussed logics. Table 4 shows the comparison between the two logics in terms of delay, power and PDP. "Fig.5c-5f" shows the analysis for different operations. "Fig.5g-5h" shows the power waveforms of both thelogics.

Table vi Performance Analysis of BARREL SHIFTER

Architecture Design	Delay in 'ps'	Power in watts 'W'	Power Delay Product in 'J'
Pseudo nMOS Logic	90.04	17.52E-3	1.577E-12
Footed Diode Domino	200	1.398E-3	0.278E-12

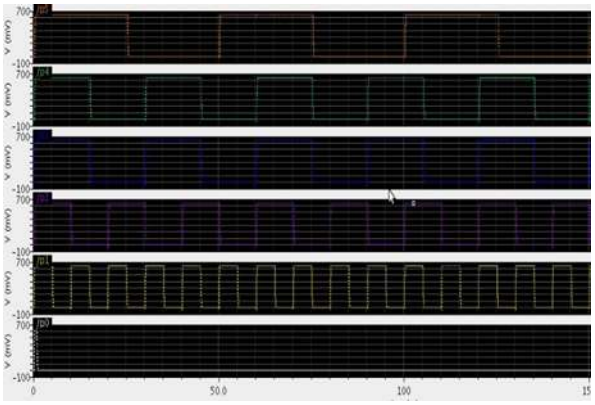


Fig.5c. Left shift logical one bit

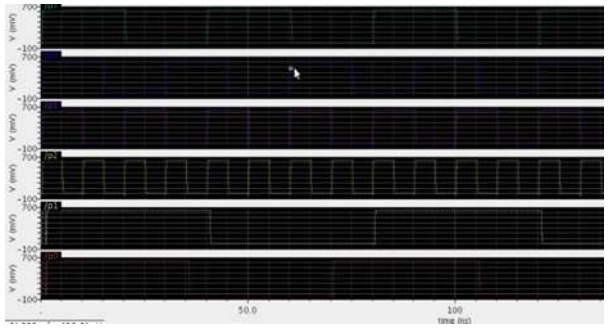


Fig.5d. Left rotate two bit.

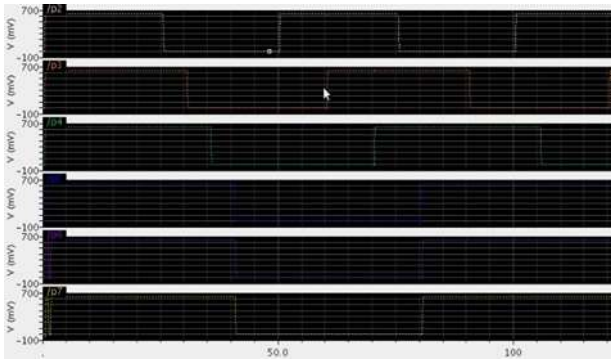


Fig.5e. Arithmetic right shift two bit

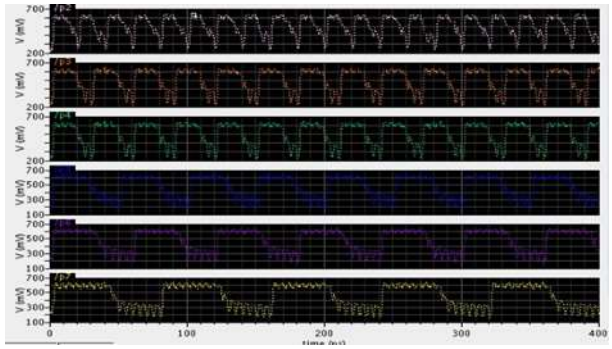


Fig. 5f. Arithmetic right shift two bit (FDD Logic)

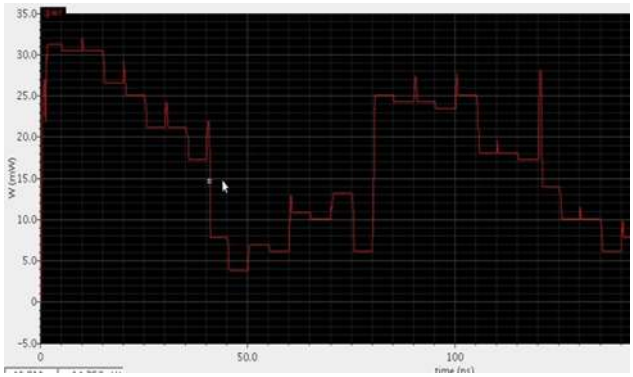


Fig.5g. Power waveform of pseudo nMOS Barrel shifter

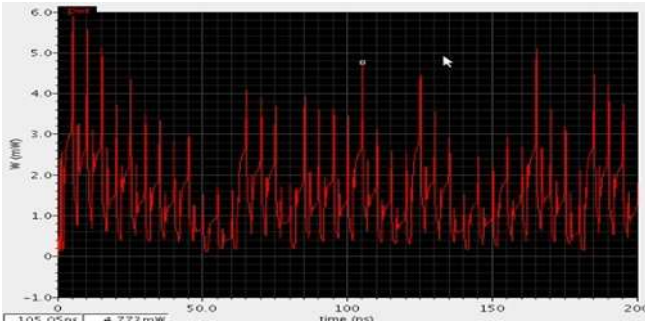


Fig.5h. Power waveform of FDD Barrel shifter

4. CONCLUSIONS AND FUTURE WORK

An 8 bit bidirectional barrel shifter using Footed diode Logic and pseudo nMOS logic was designed using 180 nm CMOS technology. The power consumption of FDD logic is compared with pseudo logic. The power utilization is altogether lessened with negligible overhead as far as postponement and zone. The simulation results indicate that optimization of the Arithmetic Logic Unit (ALU) is possible by designing the circuits using FDD logic. This work shall be further carried out on 16, 32 bit shifters with lower technology files for further improvisation of the characteristics.

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