Advanced Rail Clamping PWM Techniques based Three Level VSI fed DTC Induction Motor Drive for THD and Common Mode Voltage Reduction

C. Harinatha Reddy, K. SriGowri, T. Brahmananda Reddy, A.Pradeep Kumar Yadav

Abstract*— A space vector approach to advanced rail clamping pulse width modulation methods (ARCPWM) is developed to integrate direct torque control (DTC) scheme for the speed control of a three level inverter fed induction motor. In this method the behavior of different ARCPWM methods is analyzed with respect to zero state variation. It is observed that ARCPWM-3 shows reduction in both current harmonics as well as the common mode voltage (CMV) during near rated speed operation of the drive. To validate the proposed method a generalized ARCPWM (GARCPWM) program is developed to generate various ARCPWM methods using a constant variable 'k' that facilitates the instant of variation of zero state. Simulations results for various ARCPWM controlled three level inverter fed DTC induction motor drive are presented for comparing the performance in terms of total harmonic distortion of motor currents (I_{THD}) and CMV.

***Index Terms*—ARCPWM, CMV, DTC, GARCPWM, I_{THD}**

I. INTRODUCTION

For the past few decades many industrial applications are driven by semi-automatic and fully automatic controlled machines, and especially induction motor (IM) control has been receiving superior attention because of the advancements in power electronics field. Development of Field oriented control (FOC) of IM has enabled an AC motor to attain good dynamic responses as good as with DC motor and is based on control of stator current. Many researchers worked on the problems associated with this control and Classical Direct Torque Control (CDTC) has emerged as an alternative to the well-known field oriented control strategy for induction motor control and further better performance is achieved through Space vector Modulation techniques which is generally termed as conventional SVPWM based DTC(CSVPWMDTC).

In general voltage source inverter (VSI) used for DTC IM is the two-level VSI, that has number of inherent limitations and is traditional one. This VSI results in high distortion in the harmonics of output voltages and currents and also includes large values of *dV/dt* in the output voltages, which in turn results in deterioration of the machine performance and considerable electromagnetic interference during operation. Multilevel inverters (MLI) are viable for resolving the above mentioned limitations as given in [1].

Research on two level VSI fed DTC IM drive is still continued by many researchers towards development of switching control strategies for the decrease in torque ripple in DTC, but for better performance of the drive presently concentration is on DTC systems employing multilevel topologies. Various topologies have been introduced and the most commonly used is the three-level neutral point clamped (NPC) VSI [2] that results in the increase of the number of voltage vectors and also good extent of increase in the number of possibilities in the vector selection process which in turn leads to considerable reduction of the torque and flux ripples. Also it has advantages like increment in number of levels in the output voltage, less harmonic distortion, and lower switching frequencies when compared to two level VSI.

Another important parameter in DTC IM drives that causes damage to the IM is the Common Mode Voltage (CMV) and is a source of electromagnetic interference that results in damage of machine windings insulation and bearings. To overcome this problem numerous pulse width modulation schemes have been proposed for VSI fed Induction motor drives and however research on three level VSI fed DTC IM drive is considered in this paper. Many researchers are paying attention towards high performance PWM algorithms fed VSI fed DTC induction motor drive for better performance of the drive and some of them presented their research as given in [3-4] and are restricted to two level VSI fed only. However for three level VSI fed DTC induction motor drives there are many control strategies as discussed in [4].

For further improvement in performance of the drive mentioned above a reference voltage vector calculator is employed for three level VSI fed DTC IM drive and is applied to various Space vector based PWM schemes to avoid the use of hysteresis comparators and look up tables. Various Advanced rail clamping sequence based PWM (ARCPWM) schemes are employed to synthesize stator voltage of an induction motor for the synchronized control of torque and stator flux and are presented in this paper.

Fig.1 is a diode clamped neutral point three level inverter in which instantaneous voltage vectors possess redundancy

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characteristics that results in flexibility of inverter switching mode selection. Due to this advantage in switching selection control is done comfortably and hence performance can be improved for three level VSI fed DTC IM drive. For validating the results a simulation programme has been developed.

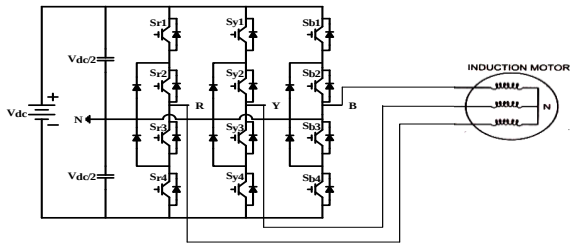

Fig. 1 Three level inverter Topology (Neutral Point Clamped) fed IM.

II. SPACE VECTOR APPROACH

For a pulse width modulation technique in which space vector approach is employed, the reference voltage vector, V_{ref} (sample reference vector) is generated by maintaining the principle volt-second balance. Different possible voltage vectors and their corresponding switching states are represented on a three level $\alpha-\beta$ axis space plane, shown in fig. 2. In a conventional two level inverter for the instantaneous position and magnitude of V_{ref} the nearest switching states are V_0, V_1, V_2 and V_0 as represented in Fig. 3. When three level space plane is considered additional switching states are possible and the voltage ripple can further be reduced by utilizing these additional switching states. The nearest switching states with three level inverter are V_7, V_1, V_{13} and V_7. The switching states with three level inversions are V_7, V_8, V_9, V10, V_{11}, and V_{12} and additional when compared to two level inverter. The switching states and inverter switch positions of r-phase are depicted in Table I.

Table I Switching states and their corresponding Pole voltages

Switching state	ON state devices	Pole voltage
2	S_{r1} and S_{r2}	$+V_{dc}/2$
1	S_{r2} and S_{r3}	0
0	S_{r3} and S_{r4}	$-V_{dc}/2$

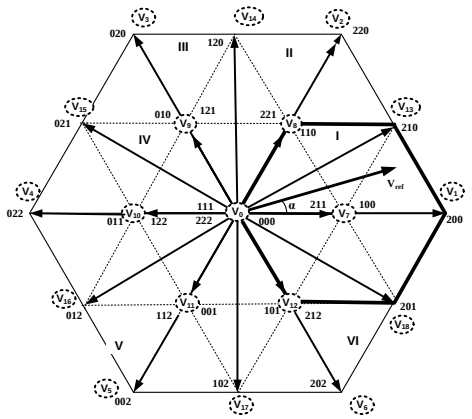

Fig.2. Three phase three level inverter switching states and their corresponding voltage vectors. I, II, III, IV, V, VI are the sectors.

For synthesizing the V_{ref} the number of steps in a three level inverter is the same as with the two level inverter and is employed in the proposed algorithm. In order to achieve this the initial point of V_{ref} is shifted to the centre of the sub hexagon in which V_{ref} is located as shown in Fig.3. The shifted reference vector V'_{ref} has V_1 as initial point and is making an angle β with reference to α axis. The time duration for voltage vectors in order to get V'_{ref} i.e state 1 (200), state 2 (210), and voltage vector state (100, 211) are obtained as T1, T2, and Tz, respectively and are given by (1)-(3). It is an added advantage in the design of PWM techniques to have T_Z division between the two zero states.

$$T_1 = M * \frac{Sin(60^0 - \beta)}{Sin60^0} * T_S \quad (1)$$

$$T_2 = M * \frac{Sin(\beta)}{Sin(60^0)} * T_S \quad (2)$$

$$T_Z = T_S - T_1 - T_2 \quad (3)$$

Here 'M' is the modulation index, given by

$$M_i = \frac{\pi V_{\text{ref}}}{2V_{dc}} . \quad (4)$$

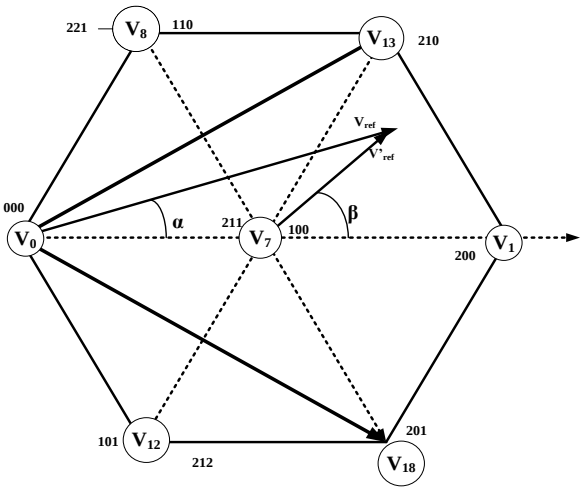

Fig. 3 Reference vector and shifted reference vector in Sector-I of sub hexagon-I

The time durations for 0127, 012 and 721 sequences are shown in Fig.5. Equal division of T_Z results in lesser ripple current in lower modulation region and is used in conventional space vector modulation to generate a given sample in sector I. Only one zero state can also be used to generate the sample as shown in fig. 4 i.e for the sequences like 0121 and 7212 and this results in better performance i.e reduced current ripple when used in little higher modulation region. Also sequences like 2721 or 1012 can be used to generate the sample by considering the time division in to two equal intervals for one of the active vectors only. The switching states placement and time division with 0127, 0121 and 7212 are shown in fig. 5.

III. CSVPWM ALGORITHM BASED THREE LEVEL INVERTER FED DTC DRIVE:

The reference voltage vector is constructed by using the errors between the reference and actual d, q axes stator fluxes and this is for controlling the torque and flux cycle-by-cycle. The block diagram of the proposed SVPWM based three level NPC fed DTC drive is as shown in Fig. 4.

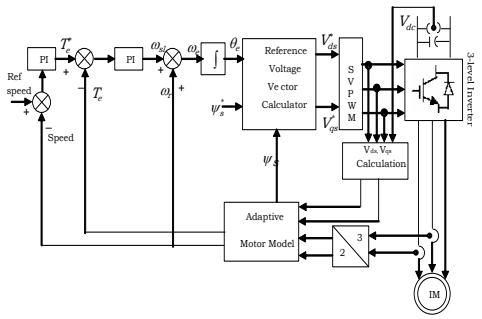

Fig. 4 Block diagram of proposed CSVPWM based NPC fed DTC-IM drive

IV. EXTENSION OF SPACE VECTOR APPROACH TO ARCPWM:

The performance parameters considered for the validation of the fact are THD in stator currents, line voltages, torque, flux ripple and CMV. In the Generalized Rail clamping PWM (GRCPWM) algorithm[5] the criteria of selection of zero states is only considered. However the degree of freedom of selection of active state along with zero state can be utilized in other way. That is active state division along with use of one zero state at any sampling time interval as shown in Fig. 5 can also be considered for generation of various advanced rail clamping PWM methods (ARCPWM) utilizing the same concept explained in GRCPWM. Since the algorithm is based on advanced rail clamping sequences it is referred as GARCPWM. This is similar to the GRCPWM algorithm in addition to zero state selection one of the active states division (either active state 1 or active state 2 in first sector) is considered for the generation of various ARCPWM methods. Also the present work considers equal division of active state time only. The placement of switching states for optimum performance is in such a way that only one state transition must be there during state change. With the proposed three level inverter fed ARCPWM based DTC significant reduction in line current THD, torque and flux ripple, common mode voltages are observed. The different ARCPWM techniques considered are ARCPWM1, ARCPWM2, ARCPWM3, ARCPWM4, ARCPWM5 and ARCPWM6.

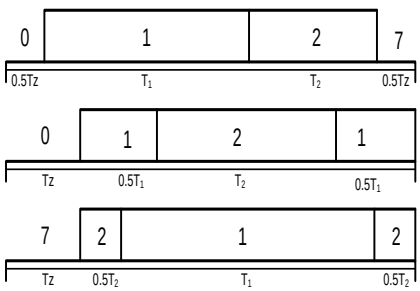

Fig. 5 CSVPWM and ARCPWM sequences

The reduction in line current THD is based on the position of clamping of the switching pulses. With ARCPWM1 clamping takes place to positive dc rail in second half and first half of sectors 1, 2 each for 30^0 and in sectors 6 and 1 respectively. With ARCPWM2 pulses of r-phase clamps to negative dc rail from second half of sector 3 to first half of sector 5 leading to a continuous 120^0 clamping. ARCPWM3 clamps for 120^0 with 60^0 clamping to positive rail in sector 1 and 60^0 clamping to negative rail in sector 4. ARCPWM4 clamps to positive dc rail in second half and first half of sectors 1, 2 each for 30^0 and to negative dc rail in second half and first half of sectors 4, 5 respectively leading to continuous 60^0 clamping to positive rail and negative rail in each half of the fundamental cycle. ARCPWM5 generates split clamping pulses each clamping for 30^0 duration in first half of sector 2, second half of sector 3, first half sector 5 and second half of sector 6 in each fundamental cycle. With ARCPWM6 clamping takes place to positive dc rail in second half and first half of sectors 6, 1 each for 30^0 and in sectors 3 and 4 respectively. This is achieved by executing the corresponding sequences as explained below.

ARCPWM1 executes 7212 in all sectors and ARCPWM2 executes 0121 in all sectors

ARCPWM3 executes 7212 in odd sectors and 0121 in even sectors and exactly opposite i.e. 0121 in odd sectors and 7212 in even sectors will synthesize pulses for ARCPWM5

ARCPWM4 requires shifting of sequence 7212 to 0121 exactly in the middle of odd sectors and 0121 to 7212 in even sectors. Similarly if sequences are reversed the algorithm generates ARCPWM6.

Fig. 6.shows the schematic diagrams of the instances of generation of various ARCPWM methods where Z1-Z6 are sectors

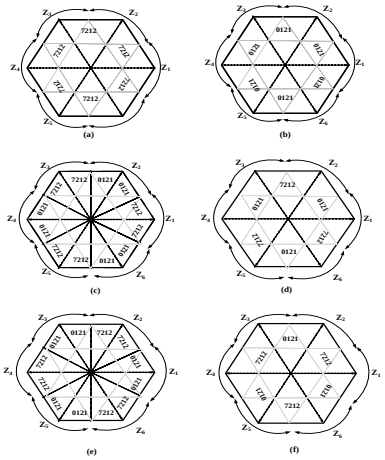

Fig. 6. Schematic diagrams showing the instances of generation of various ARCPWM methods (a) ARCPWM1 (b) ARCPWM2 (c) ARCPWM3 d) ARCPWM4 e) ARCPWM5 (f) ARCPWM6 where Z1-Z6 are sectors

V. COMMON MODE VOLTAGE

The common mode voltage (CMV) is the voltage between the centre of star connected

point and the ground in a star connected 3-phase induction motor. For any star connected 3-phase induction motor the CMV(V_{com}) is given as

$$V_{com} = V_{so} = \frac{V_{ao} + V_{bo} + V_{co}}{3} \quad (5)$$

where V_{ao}, V_{bo}, V_{co} are inverter pole voltages. For a balanced 3-phase supply this CMV is zero. But it changes instantaneously whenever the drive is fed from an inverter. The CMV depends on the switching states of the inverter and also its DC link voltage. Therefore the CMV changes whenever the switching state is changed. The different switching states along with the associated CMVs are given in table 2.2. There will be no change in CMV if only even vectors or only odd vectors are used. When a change from an even voltage vector to an odd voltage vector occurs, CMV of Vdc/3 is generated. If the change from an odd vector voltage vector to the zero voltage vector occurs a CMV of 2Vdc/3 is generated which is the worst case.

VI. PROPOSED THREE LEVEL INVERTER FED GARCPWM BASED DTC

The present section investigates the effect of variation of zero state and distribution of active states on the DTC induction drive. A generalized algorithm to extract all the advanced PWM methods is programmed in MATLAB to synthesize required three level switching pulses. The pulses are synthesized based on the selected PWM method, torque and speed controller outputs. The speed controller generates reference torque based on the error between reference speed and actual speed and error in torque generates reference slip speed. Addition of reference slip speed with actual rotor speed generates reference frequency.

With inputs as reference flux magnitude and its rotating speed, RFVC block will generate reference voltage vector to synthesize three level output phase voltages to match the reference speed through GARCPWM algorithm. GARCPWM is an m-file program developed in MATLAB for easy implementation in any controller. Adaptive motor model takes motor voltages and currents as inputs and estimates actual speed and torque. The overall block diagram for executing the GARCPWM based three level inverter fed induction motor drive is shown in Fig. 7.

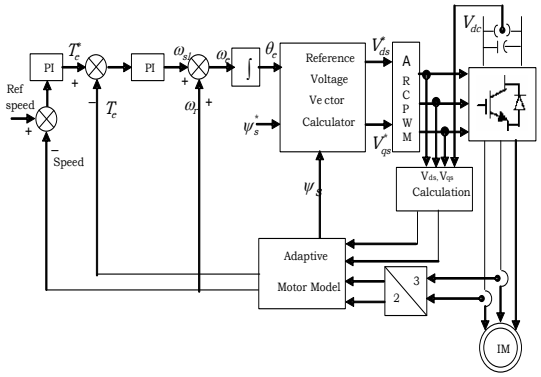

Fig. 7. Block diagram of GARCPWM based DTC Induction motor drive

VII. RESULTS AND DISCUSSION

To verify the proposed ARCPWM schemes, numerical simulation has been carried out in MATLAB/Simulink environment. The average switching frequency of the inverter is taken as 3KHz. Simulation results for different ARCPWM based three level VSI fed DTC induction machine are given in Fig.8 to Fig.17. It can be observed that among ARCPWM algorithms for three level VSI fed DTC drive, the performance is significantly improved with the proposed ARCPWM3 method in terms of torque and flux ripple. Apart from these the common mode voltage is also shown in Fig 18 for all ARCPWM methods which depicts the better values ARCPWM3 method employed. The line current THD is shown in Fig 7 and also the locus of flux ripple shown in Fig. 8. Table. 1 shows the comparison of various ARCPWM methods with CSVPWMDTC method. Among the various ARCPWM methods ARCPWM3 gives less THD in line current along with common mode voltage. The overall behavior in terms of starting transients, steady state. no-load behavior, transients during step change in load and transients during reversal of speed is presented from Fig. 9 to fig. 17. for all the ARCPWM methods that drive the DTC induction motor. The harmonic spectral performance is measured for steady state no-load condition since the performance of any PWM method is judged by this and it agrees with ARCPWM3. The simulation parameters are given in Annexure and results are given below.

SIMULATION PARAMETERS

Induction Motor Parameters: 3-ϕ, 400V, 4 kW, 4-pole, 1470 RPM, 50 Hz,T=30 N-m

Stator Resistance, R_s	**1.57 Ω**
Rotor Resistance, R_r	1.21 Ω
Magnetizing Inductance, L_m	0.165 H
Stator inductance, L_s	0.17 H
Rotor inductance, L_r	0.17 H
Moment of Inertia, J	0.089 Kg - m^2
Viscous friction coefficient, B	0 N-m.sec/rad

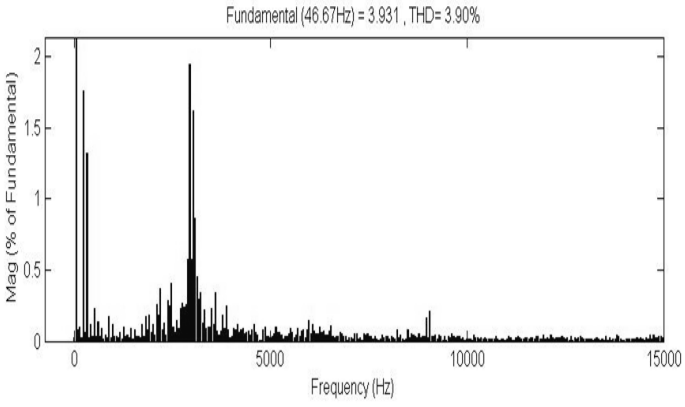

Fig. 8 ARCPWM3-three-level VSI fed DTC: Harmonic Spectra of Line current

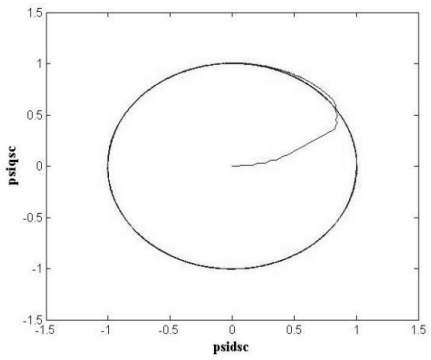

Fig. 9 ARCPWM3-three-level VSI fed DTC: Stator flux locus.

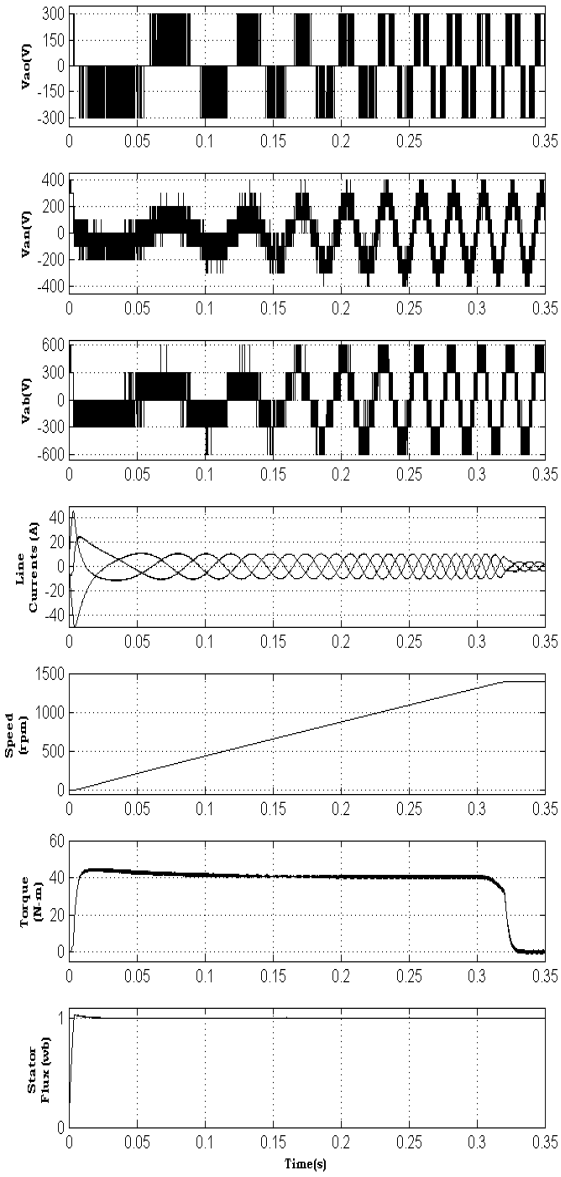

Fig. 10 ARCPWM3 based three level VSI fed DTC: Pole, phase and line voltages, Line currents, speed, torque and stator flux plots during transients.

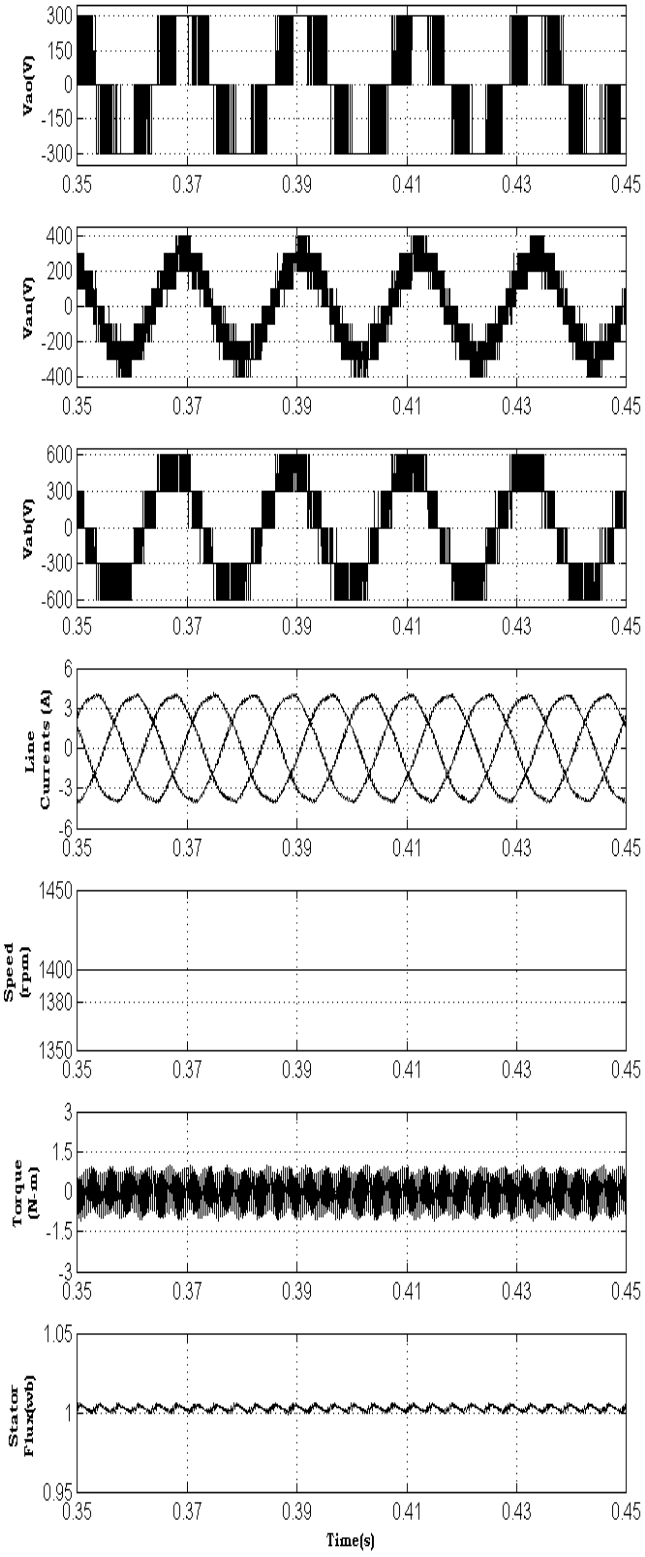

Fig. 11. ARCPWM3 based three level VSI fed DTC: Pole, phase and line voltages, Line currents, speed, torque and stator flux plots during steady state.

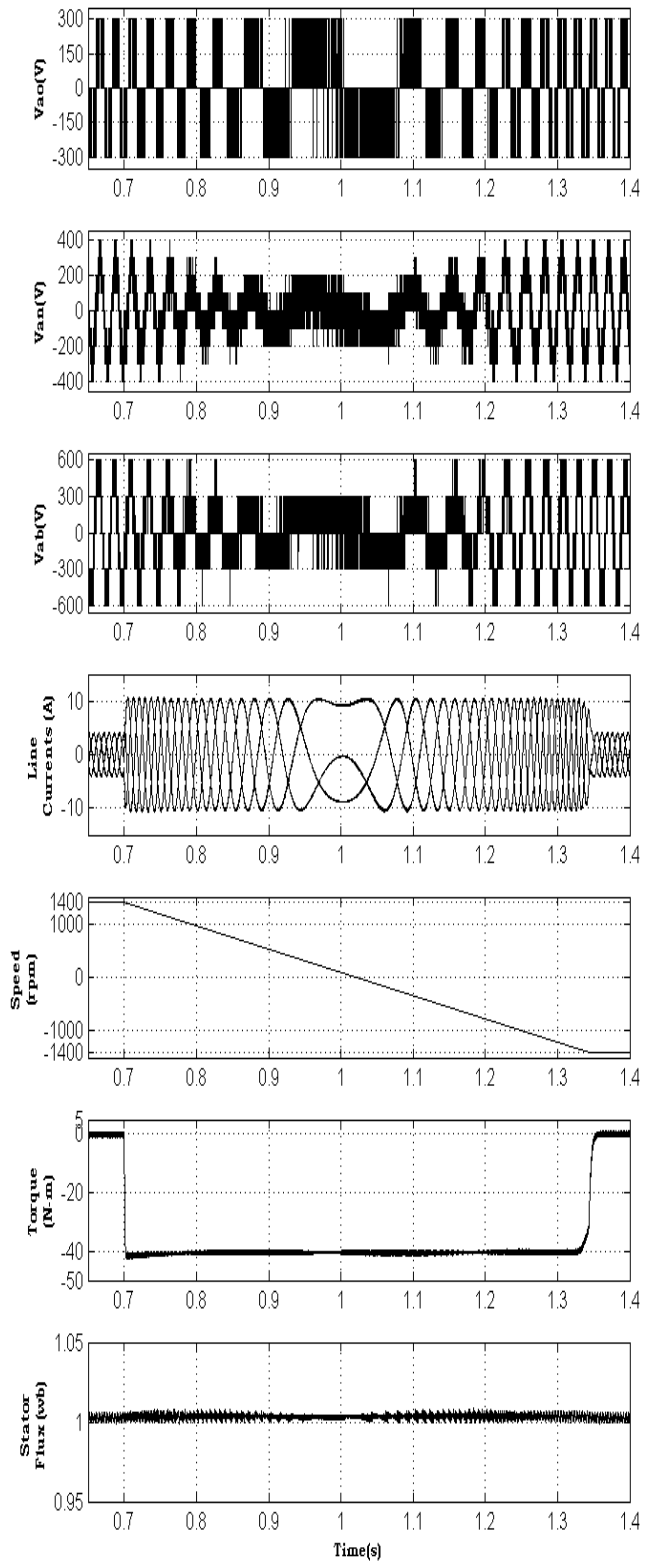

Fig. 12. ARCPWM3 based three level VSI fed DTC: Transients in pole, phase and line voltages, Line currents, speed, torque and flux during change in load: a 30 N-m load is applied at 0.5 s and removed at 0.6 s

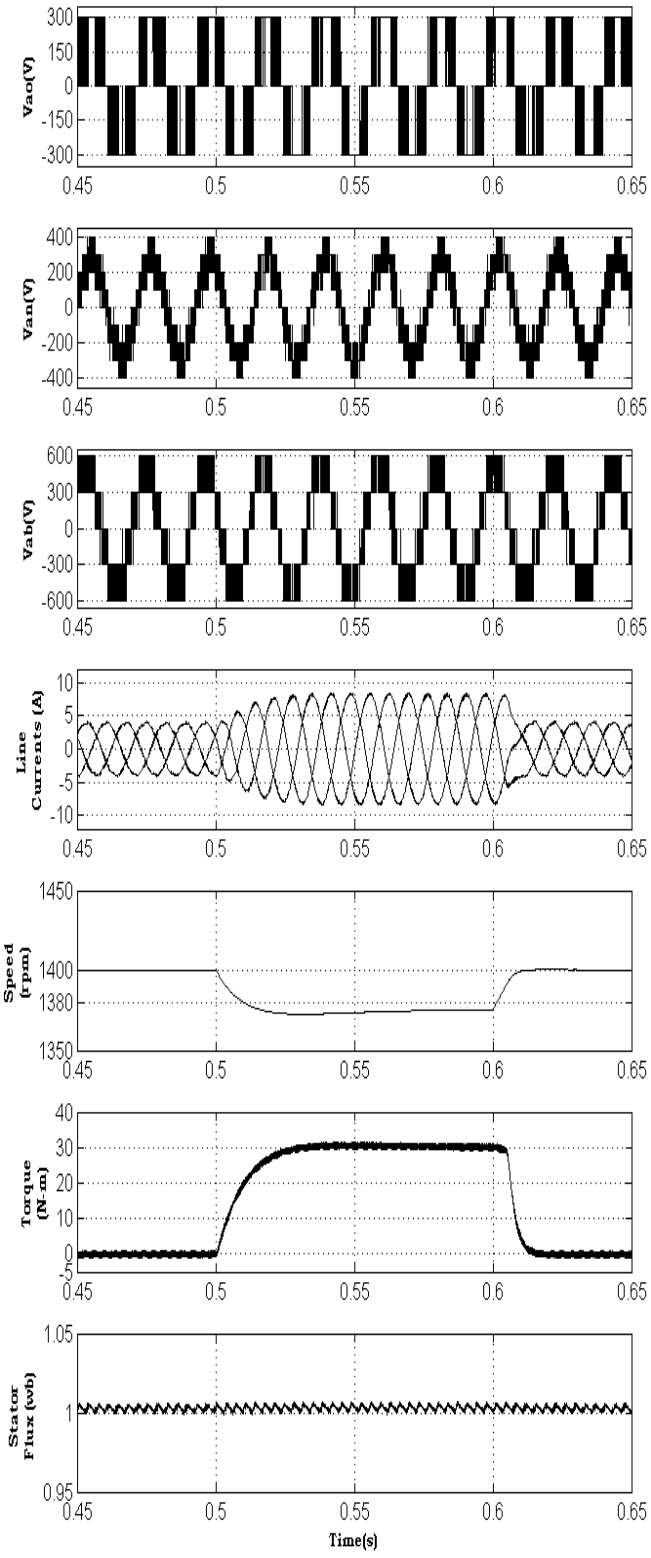

Fig. 13. ARCPWM3 based three level VSI fed DTC: Transients in pole, phase and line voltages, line currents, speed, torque and stator flux during speed reversal: speed is changed from +1400 rpm to -1400 rpm at 0.7 s and from -1400 to +1400 at 1.3 s

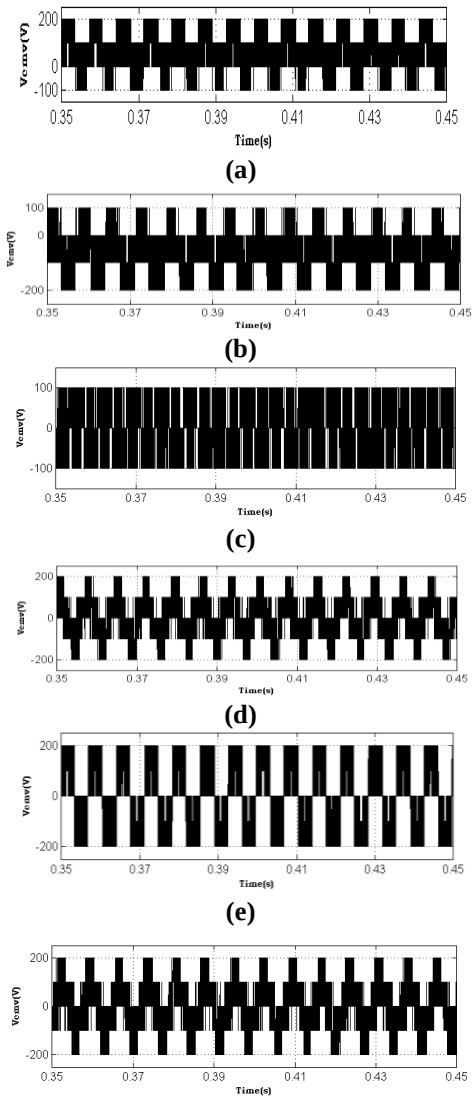

Fig 14. Common mode voltage waveforms during steady state for (a) ARCPWM1, (b) ARCPWM2, (c) ARCPWM3, (d) ARCPWM4, (e) ARCPWM5, (f) ARCPWM6 based three level VSI fed DTC IM drive.

Table 1 Comparison of THDs in line currents and common mode voltage with various RCPWM, ARCPWMs integrated with two & three level inverter fed DTC Induction motor drive with respect to CDTC and CSVPWM DTC

VIII.RESULTS

S.No	Method	Three level VSI fed DTC IM % THD of line current	CMV for three level VSI fed DTC IM drive (Peak to Peak Magnitude) in Volts
2	CSVPWM DTC	4.75	400
3	ARCPWM1	4.27	300
4	ARCPWM2	4.29	300
5	**ARCPWM3**	**3.90**	**200**
6	ARCPWM4	5.34	400
7	ARCPWM5	5.37	400
8	ARCPWM6	5.38	400

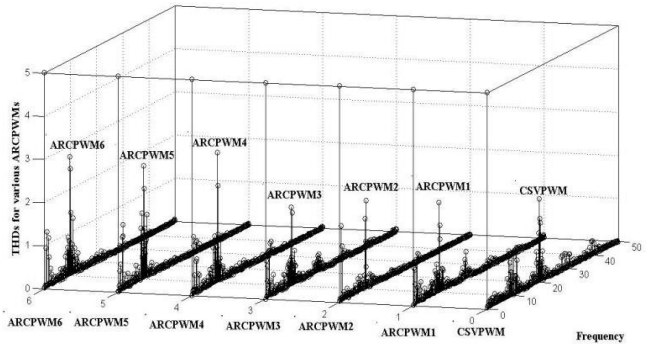

Fig.15. Comparison of THDs for various ARCPWMs with CSVPWMDTC

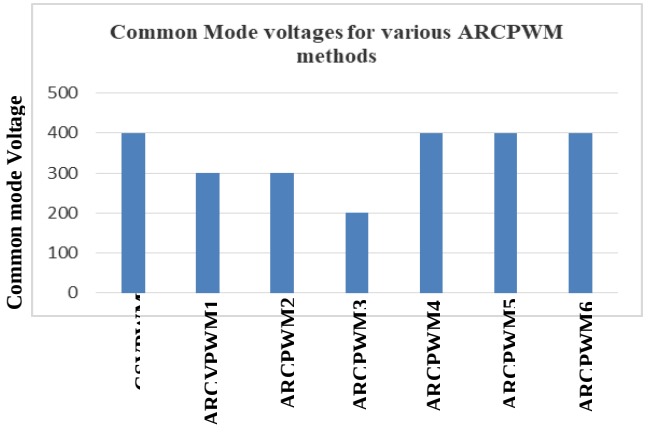

Fig. 16.Comparison of common mode voltages for various ARCPWM methods.

IX. CONCLUSIONS:

From the results obtained in the previous sections for the proposed three level VSI fed ARCPWM DTC drive, it is clear that the % THD of the line current in CSVPWM method are high compared to ARCPWM methods. CSVPWM has highest THD of 4.75% for three level VSI fed DTC where as ARCPWM methods have low THD's because of the better performance. There is a considerable reduction in flux and torque ripple also. It has been proved that by proper selection of zero state vectors and other vectors and their time width, the amplitude of developed torque also can be controlled. Therefore, control of flux and torque is done separately. Also there is considerable reduction in the common mode voltage by 33.33% for ARCPWM3 method in comparison with CSVPWM method. At the outset the overall performance of the drive operating at high modulation is noticeable with three level inverter controlled by ARCPWM3 method integrated with DTC speed control technique.

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