

# Research on Two Stage and Folded Cascode Bulk Driven OTA in 0.18um CMOS Process

N.Sharath Babu, G.Sreenivasa Raju, Amrita Sajja

**Abstract**— This paper presents a comparative analysis of two stage and folded cascode bulk driven operational trans conductance amplifier (OTA) topologies for biomedical applications. A two stage bulk driven OTA and Folded cascode OTA operated with a 1V power supply. Bulk-driven PMOS-transistors as an input differential opamp provides high input common-mode range (CMR). To achieve low power consumption all transistors must be operated in sub threshold region. The test results are carried out in standard gpdk180nm CMOS technologies.

**Keywords**— OTA, Bulk Driven, CMR, CMOS, Folded Cascode.

## I. INTRODUCTION

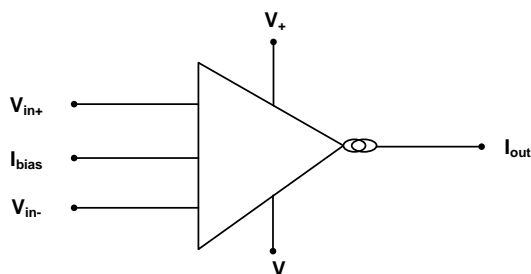


Figure.1 Symbol of OTA

The operational trans conductance amplifier (OTA) is a voltage (V) to current (I) converter device, is an amplifier which converts differential input voltage to output current. OTA has additional input terminal compared to a conventional operational amplifier.

Low power operating conditions considered tough when it comes under portable applications. Especially when it is operated at below 1V applications for such cases leakage currents and voltage drops will play major role[1-6]. These problems can be overcome if we accommodate weak inversion regions of advanced VLSI technologies. Portable applications reduced power consumption made lower supply voltages increasingly common, for a single battery cell migrating down to 0.8V. In biomedical applications amplifier and analog filters[2] plays an essential role because neural signals are very weak in amplitude so amplification is essential before transmitting [7-9].As

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mentioned in the references common mode range input circuits is limited by few approaches like charge pump and the floating gates. Bulk driven concept is very sensitive in cmos design[11-13]. Additionally, with the proper scaling of the supply current and by opting weak inversion techniques can increase the product battery life time[8]. By connecting a p-channel or n-channel differential pair in parallel a conventional rail to rail operational amplifier is designed. But it will work properly in saturation levels only because of the larger value of the threshold voltage to that of total supply voltage. The transconductance of the amplifier can be increased if can able to increase trans conductance of input differential pair which can also alter common mode voltage[12].

## II. TWO STAGE BULK DRIVEN OPERATIONAL AMPLIFIER

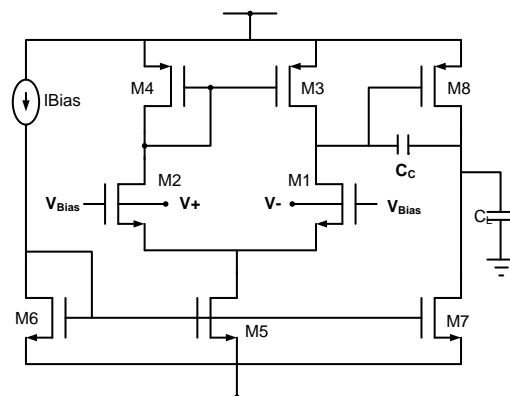


Figure.2 Schematic of FD Bulk driven OTA

The gain of the amplifier is the ratio between output current and differential voltage. The conventional OTA is an amplifier that converts differential input voltage to output current. It is called a trans conductance amplifier. Fig.2 shows the fully differential operational trans conductance amplifier with Low voltage bulk driven topology. M1, M2 are differential bulk driven pair with the conjunction of the M3, M4 form a differential input stage. M5 form a biasing transistor, M6 form a current mirror transistor and M7, M8 form a gain stage. However, the only difference is that input is applied from the bulk terminal and channel is kept in strong inversion region by connecting the gates of transistor M1 and M2 to desired power supply.

The bulk driven operational amplifier’s transconductance is given by

$$g_{mb} = g_m \frac{\gamma}{2\sqrt{2\phi_f - V_{SB}}} \quad (1)$$

Where  $\gamma$  is the Body Effect Coefficient and  $V_{SB}$  is a source of bulk voltage.

**Table.1 Operating points for transistors in the OTA shown in Figure.2**

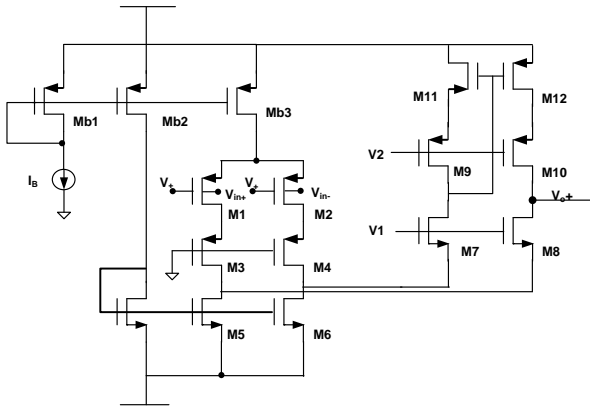
Devices	W/L (in um)	I <sub>D</sub> (uA)	Region
M1:M2	5/1.75	9.943	Saturation
M3:M4	6/980	9.943	Saturation
M5:M6	1.62/1.29	20	Saturation
M7	46/1.23	67.68	Saturation
M8	5/1.06	67.56	Saturation

The differential input pair will not conduct unless the supplied gate voltage is greater than threshold voltage. So  $V_{Bias}$  is the voltage which turns the transistor into saturation.

The differential gain of OTA is shown in Fig.5 and common mode gain of OTA is given in Fig.6 with 63.98dB differential gain and -30.16 dB common mode gain

The Fig.7 shows output waveforms of the OTA phase and unit gain bandwidth of the proposed OTA which shows a phase of 61.9° and 9.05MHz unity gain frequency. The average power of OTA is 77.26uW.

**III. PROPOSED BULK-DRIVEN OTA WITH A CURRENT SCALING TECHNIQUE**



**Figure: 3 Bulk Driven OTA proposed schematic**

The above schematic shown in Fig.3 bulk driven OTA also similar to the previous model but it is a folded cascode structure. The input signal is given to the bulk terminal of the transistor and channel is formed between the source and the drain by biasing the gate terminal. The equivalent trans conductance ( $G_M$ ) of the amplifier is the sum of individual transistor trans conductance.  $G_M$  depends on the bulk trans conductance of the input pair for a bulk driven input stage[1]. Bulk trans conductance ( $g_{mb}$ ) of an input device is less than its gate trans conductance ( $g_m$ ) because its gate-driven counterpart, a bulk-driven opamp has less gain and larger bandwidth. Bulk trans conductance  $g_{mb}$  can be expressed in equation 1.

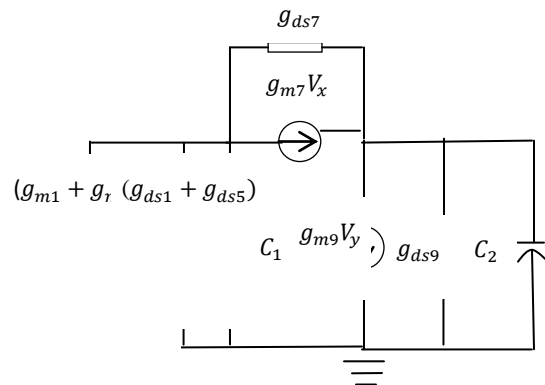
The weak physiological signal of the input stage as shown in Fig.3 is connected to the bulks of input pair M1 and M2

and the gates are connected to ground which makes the M1 and M2 transistor operate in the weak inversion region. The drain to source current  $I_{DS}$  in equation 2 in weak inversion region depends on reverse saturation current  $I_S$ , is ambient temperature is given by T, the inclination of the curve in weak inversion is represented by n, the Boltzmann constant is K, charge of the electron or hole is represented by q.

$$I_{DS} = I_S \left(\frac{W}{L}\right) \exp\left(q \frac{V_{GS} - V_{th}}{nKT}\right) [1 - \exp\left(-q \frac{V_{DS}}{KT}\right)] \quad (2)$$

The current scaling technique is implemented by the transistors M5 – M8. Transistors Mb1, Mb2, Mb3 converts voltage to current, to deliver the differential currents to the output stage by forming a current mirror. Transistors M1-M12 operated in weak inversion region with appropriate W/L ratio

**III-I Small Signal Analysis**



**Figure 4: Small signal analysis of proposed folded OTA**

The equivalent circuit of a folded cascode CMOS OTA to determine the voltage gain with respect to input voltage is as follows. OTA shown in Fig.4 has the input signal  $V_i$  is given at bulk terminals of the input differential pair of transistor. That is, for the bulk of M1 and M2. To inflate gain with body effect, M3 and M4 transistors bulk pins are applied to the power supply  $V_{DD}$ , whereas those terminals of M5 and M6 to the power supply  $-V_{SS}$ . The capacitance C1, C2 represents the total node capacitance at the drains of M3, M5 and M9 respectively. Whereas  $g_{ds1}, g_{ds5}$  are the trans conductance of M1 and M5 respectively.  $g_{ds7}, g_{ds9}$  are the trans conductance of M7 and M9 respectively.

The overall DC small-signal differential gain is

$$G_M = g_{mb1} \left(\frac{G_{S7}}{G_{S7} + G_{d5}}\right) \left(\frac{G_{S3} r_{o1}}{1 + G_{S3} r_{o1}}\right) \quad (3)$$

$$A_{dm} = G_M \left(\frac{g_{m7} + g_{m9}}{g_{ds5} + g_{ds7} + g_{ds9}}\right) \quad (4)$$

The current which flows in the folded branch transistors is a little amount of the current in the input differential pair transistors.

**III-II Current Scaling**

Current scaling is done by increasing the output impedances and thereby ensuring current scaling. M1 and M2 have a small portion of currents from M5, M6 and the



differential currents between M3, M4 due to source degenerated current mirrors formed by transistors M5 and M6 and R2, R3 resistors. Current scaling ratio of 7:1 is done between Mb1 and Mb2 to save the bias power in circuit as shown in Fig 3. The currents in M5 and M6 are set to  $8I_B/7$  adjust  $I_B/7$  currents in the folded branch transistors, which is 1/3rd of the differential input pair current. By using resistors R2,R3 these current ratios are achieved and the ratio of R1 and R2 or R3 is 1:50.

**Table 2: Operational trans conductance amplifiers Operating points**

Devices	W(um)/L(nm)	$I_D$ (nA)	Operating Region
M1:M2	20/180	393	Sub threshold
M3:M4	50/180	393	Sub threshold
M5:M6	10.02/200	505	Sub threshold
M7:M8	1/180	112	Sub threshold
M9:M10	1/180	112	Sub threshold
M11:M12	1/180	112	Sub threshold

**Table 3: Design Summary of OTA:**

	Current Division Ratio's
Mb1:Mb2	7:1( $2I_B/14$ )
M1:M2, M3:M4	$7I_B/14$
M5:M6	$9I_B/14$
M7:M8, M9:M10, M11:M12	$I_B/7$

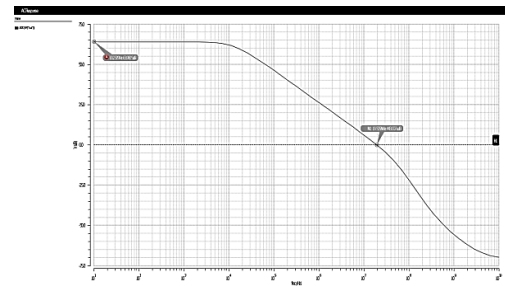
**Table 4: Key Parameters Of The Bulk Driven OTA**

Parameter	Body Input OTA
Supply Voltage	0.5V
Power Dissipation	620nW
Input Current	100nA
DC Gain	58.4dB
3dB Bandwidth	282.16KHz
Unity Gain Bandwidth	18MHz
CMRR	87.9
PSRR	94.3
Load capacitance	1pF

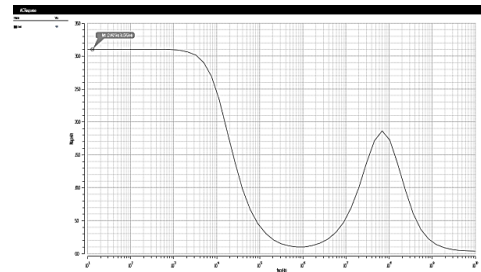
**Table 5: Performance Comparison**

Parameter	Body Input OTA	Two Stage
Supply Voltage	0.5V	1V
Power Dissipation	620nW	77.26uW
DC Gain	58.4dB	63.98dB
Unity Gain Bandwidth	18MHz	9.05MHz
CMRR	87.9	94.14

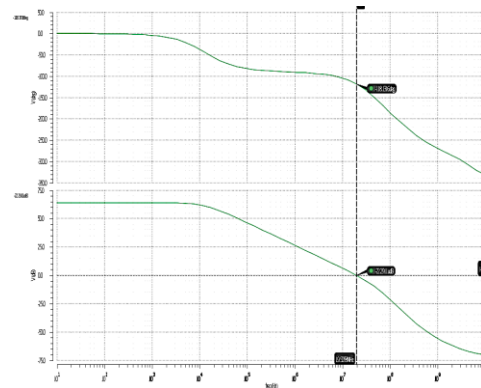
**IV. TEST SIMULATION RESULTS**



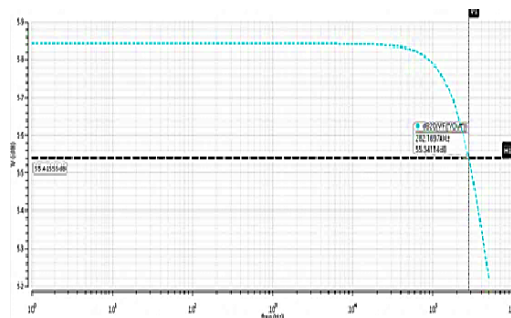
**Figure: 5 OTA Differential Gain plot**



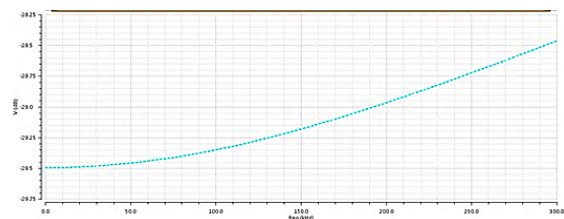
**Figure: 6 OTA Common mode gain plot**



**Figure: 7 phase and UGB plot**



**Figure 8: Differential Gain 58.4dB and BW=282.16 KHz**



**Figure 9: Common mode Gain -29.5dB**



## V. CONCLUSION

A comparative analysis of fully differential bulk driven to stage OTA and folded cascode OTA is presented. Power consumption of folded cascode OTA is less compared to two stage OTA because of transistor operating regions are in sub threshold with very small current in terms of nano amperes. But Gain is reduced in folded cascode OTA because of its reduced transconductance.

## REFERENCES:

1. N. Tang, W. Hong, J. Kim, Y. Yang and D. Heo, "A Sub-1-V Bulk-Driven Opamp With an Effective Transconductance-Stabilizing Technique," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 62, no. 11, pp. 1018-1022, Nov. 2015.
2. S. Chatterjee, Y. Tsividis and P. Kinget, "0.5-V analog circuit techniques and their application in OTA and filter design," in *IEEE Journal of Solid-State Circuits*, vol. 40, no. 12, pp. 2373-2387, Dec. 2005.
3. J. M. Carrillo, G. Torelli, R. Perez-Aloe Valverde and J. F. Duque-Carrillo, "1-V Rail-to-Rail CMOS OpAmp With Improved Bulk-Driven Input Stage," in *IEEE Journal of Solid-State Circuits*, vol. 42, no. 3, pp. 508-517, March 2007.
4. E. Kargaran, M. Sawan, K. Mafinezhad and H. Nabovati, "Design of 0.4V, 386nW OTA using DTMOS technique for biomedical applications," *2012 IEEE 55th International Midwest Symposium on Circuits and Systems (MWSCAS)*, Boise, ID, 2012, pp. 270-273.
5. T. Lehmann and M. Cassia, "1-V power supply CMOS cascode amplifier," in *IEEE Journal of Solid-State Circuits*, vol. 36, no. 7, pp. 1082-1086, Jul 2001.
6. Troy Stockstad, Hirokazu Yoshizawa, "A 0.9V, 0.5pA Rail-to-Rail CMOS Operational Amplifier" *IEEE 2001 custom integrated circuits conference*, IEEE, pp 467-470. 2001
7. K. Lasanen, E. Raisanen-Ruotsalainen, and J. Kostamovaara, "A 1-V 5 $\mu$ W CMOS-opamp with bulk-driven input transistors," in *43rd IEEE Midwest Symp. Circuits and Systems*, 2000, pp. 1038-1041.
8. E. Vittoz and J. Fellrath, "CMOS analog integrated circuits based on weak inversion operations," in *IEEE Journal of Solid-State Circuits*, vol. 12, no. 3, pp. 224-231, Jun 1977.
9. J. Pan and W. J. Tompkins, "A Real-Time QRS Detection Algorithm", *IEEE Transactions On Biomedical Engineering*, vol. -32, no. 3, pp. 230-236, March 1985
10. Valtino X. Afonso, "ECG QRS Detection" in *Biomedical Digital Signal Processing*
11. Arash Ahmadpour and Pooya Torkzadeh "An Enhanced Bulk-Driven Folded-Cascode Amplifier in 0.18  $\mu$ m CMOS Technology" *Circuits and Systems*, vol. 3, no. 2, pp. 187-191, March 2012.
12. G. Raikos and S. Vlassis, "Low-voltage bulk-driven input stage with improved transconductance," *Int. J. Circuit Theory Appl.*, vol. 39, no. 3, pp. 327-339, Mar. 2011.
13. M. De Matteis, A. Donno, S. Marinaci, S. D'Amico and A. Baschiroto, "A 0.9V 3rd-order single-OPAMP analog filter in 28nm CMOS-bulk," *2017 7th IEEE International Workshop on Advances in Sensors and Interfaces (IWASI)*, Vieste, 2017, pp. 155-158.