1.5mW,14.68V/µS-Low Power and High Speed Comparator Design for ADC Applications

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Abstract— Advanced medical equipments embedded with the sensors, analog to digital converters (ADC) and other equipment. Gain amplifier and the comparator are key blocks in ADCs improvement. Comparator is the key element in achieving a low offset and high slew ratein the ADCs, in addition power and speed optimizationdesigns are preferred. To achieve high speed and low power a modified architecture of a comparator is introduced. A 5V two stage comparator is designed to meet the specifications as, offset value <8.4mV, power dissipation <1.5mW and slew rate>14.68V/µS. Cadence Virtuoso tools and SCL 0.18 µm technology parameters are used for design. Designed comparator shows improved slew rate and power consumption in comparison with the existing comparators.

Keywords— Comparator, High speed, ADC, low offset, high slew rate

I. INTRODUCTION

Comparator is a decision making circuitand is widely used in data converters,thesymbol is shown in fig.1.In ADC, the input signal is sampled with comparators to determine the Logical 0 or 1 equivalent to sampled analog signal [1]. It compares the input analog signal with reference voltage and gives a logical 0 or 1based on the comparison. If positive input voltage is greater than negative input voltage($+V_P > -V_N$) logic 1 is resulted in output, when positive input voltage is less than negative input voltage($+V_P < -V_N$) logic 0 is resulted in output[2]. Pre-amplifier, decision making stage and an output buffer stage forms comparator as shown in the Fig.2 [3].Pre-amp amplifies the input signal to improve the comparator sensitivity and isolates the input of the comparator from switching noise coming from the positive feedback stage i.e. kick back noise effect,latchbased comparators reduces this noise effect.Second stage determines which input signal is larger, and is optional for single bit comparators. The final stage is used as amplifier gives logical values as output. Their role of Comparator in ADCs (SuccessiveApproximation Register (SAR), flash, pipeline) has special importance, because there is a need of accurate translation of even small analog signals into digital form. Therefore, resolution, noise, offset, power consumptionandSpeed dictates the overall ADC performance [4–6].In simplest way, comparator can be considered as 1-bit A/D. Offset, resolution, Unity gain band width, speed, sensitivity, resolution, noise, metastability, overdrive recovery and power dissipation are the design parameters of the comparator.Technology scaling reduces the output conductance output voltage swing, thereby reduces the DC gain [7].Comparators divided into open-loop and regenerative type, open-loop comparators are basically Op-Amps without compensation, the regenerative comparator uses positive feedback similar to the sense amplifiers or flip-flops, to accomplish the comparison of the magnitude between the two signals.Third type comparator emerges as a combination of the open-loop and regenerative type and are extremely fast.When the comparator is designed in ultra deepsubmicrometer (UDSM) CMOS technologies, they are suffers with supply voltages.

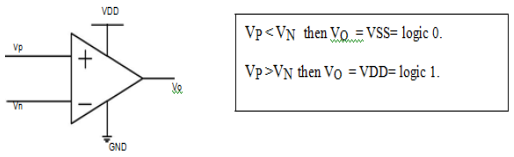

Fig.1: Comparator operation

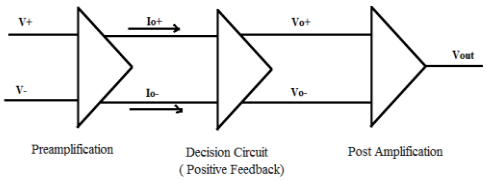

Fig. 2: Block diagram of Comparator

To attain high speed, transistors are designed with large size to compensate scaling of supply voltage requiring more power and area. ICMR is important in comparator for high speed ADC but limited by low supply voltages. The techniques, such as supply boosting methods [8-9], body-driven transistors techniques [10-12] and dual-oxide processes helps in controlling higher supply voltages meeting challenges of low voltage designs. To address input-range and switching problems, effectively boosting and bootstrapping are used but they are not reliable [11]. These allow body driven MOSFET operating as a depletion device by removing the threshold voltage requirement. But special fabrication process makes the body driven transistor suffer from smaller transconductance. Avoid stacking

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transistors is preferred for low-voltage operations. In [13]–[15], to increase speed an extra circuitry is added to conventional Coparator. The comparator [13] dissipates 18 µW power at a supply of 0.5 V having clock frequency of 600 MHz. Fast operation over a wide common-mode range is achieved in double-tail dynamic comparator [16] by separate input and cross-coupled designs. The comparator design issues are, as it is usually gain stage and attained by either cascading. The cancellation of the offsets, PSRR, Overdrive recovery and power consumption are the challenges.

II. EXISTING DESIGNS

Comparator has to be designed with high accuracy providing high slew rate and gain, since the decision of 0 logic and 1 logic should be passed quickly for data converters [17, 18].Dynamic latch comparator shown in the Fig.3 has a setback of limited to only two stages and to reduce delay an extra stage is introduced with more area and a higher power consumption [19, 20, 21, 22]. Conventional comparator is shown in the fig.4 [23].

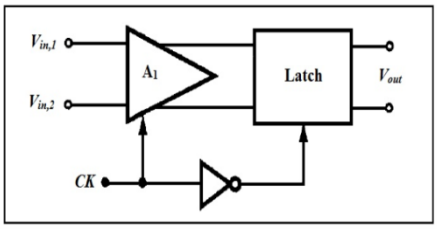

Fig.3: Block Representation of a latched comparator

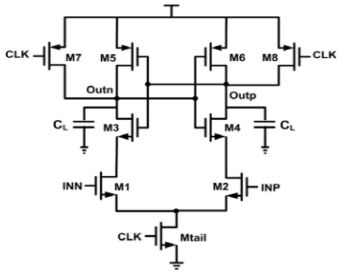

Figure 4. Conventional comparator [23]

Transistors M3 and M4 are in positive feedback in the design, decision process begins as the voltage level of one output drops so small to turn on transistors M5 and M6[24]. For small supply voltages, the V_{GS} of M3 and M4 are small and equal to those of M5 and M6 which leads to low transconductance of transistors resulting in raise in the delay time. The transistor Mtail is off, as CLK is 0 in reset phase,M7 and M8 are reset transistors which pull output nodes to V_{DD} to have valid logical level which defines start condition at the reset. Transistors M7 and M8 are off while Mtail is on during CLK is Vdd in comparison phase. Pre-charged output voltages (Outp, Outn) starts to discharge from Vdd depending on input voltages. Case 1: if Positive input voltage is graeter than negative input voltage, positive output discharges fast than negative output, which falls to V_{DD}–$|V_{THP}|$ before negative output, the corresponding pMOS transistor (M5) will turn on initiating the latch regeneration caused by back-to-back inverters (M3, M5and M4, M6). Thus, negative output pulls to V_{DD} and positive output discharges to ground. Clocked regenerative comparators have found wide applications in many high-speed ADCs since they can make fast decisions due to the strong positive feedback in the regenerative latch. Many ample analyses have been presented, from different aspects, such as noise [24], offset [25], [26], and [27], random decision errors [28], and kick-back noise [29].

III. PROPOSED COMPARATORDESIGN

Comparator design starts with initial specifications of Offset, Gain, slew rate and power consumption. Slew rate is rate of change of output with respect to input.Propagation delay can be improved by large input voltage. Propagation delay can be deduced by

$$t_p = \Delta T = \frac{\Delta_V}{SR} = \frac{V_{OH} - V_{OL}}{2SR}$$

Where,

ΔT = propagation delay; ΔV = Change in output voltage of the comparator

SR = Slew rate; VOH = Comparator Upper limit

VOL = Comparator Lower limit

Dynamic power dissipation of Comparator

$$P = fCV_{DD}^2$$

Where,

f: output frequency

V_{DD}: supply voltage

C: output capacitance.

The comparator proposed is shown in fig.5. M1 and M2transistors sizes and load capacitance will be optimized by considering transconductance and the input resistance. By keeping the channel length constant the conversion speed can be improved but it leads to channel length modulation which rises unwanted offset voltage [30]. The gain is enhanced by sizing widths of M3 and M4 transistors. Output currents are given below

$$i_{o+} = \frac{g_m}{2}(v_+ - v_-) + \frac{I_{ss}}{2} = I_{SS} - i_{0-} \quad (1)$$

$$g_m = g_{m1} = g_{m2} \quad (2)$$

Currents i_{o+} and $i_{o-}$are transferred to decision circuit which in turn leads to the switching of transistors M7-M10 to make the decision. Transistors M1 and M2 have same g_m but when input varies it generates two different currents.

Transistors M7- M11 forms the decision circuit which can be capable of discriminating millivolt level of signal shown this circuit in fig.5, and noise on a signal is eliminated by design with hysteresis [31]. Gain is enhanced by Positive feedback in cross-gate connection of M8 and M9.

When, $i_{0+} >> i_{0-}$ which leads to Vgs>Vth of M7and M9, hence these transistors will be turned ON pushing M10 andM8 transistors into OFF since its Vgs<Vth. Assume that $\beta_{M7} = \beta_{M10} = \beta_A$ and $\beta_{M8} = \beta_{M9} = \beta_B$. Under these conditions, $v_{0-} \approx 0V$ and v_{0+} is given by

$$v_{0+} = \sqrt{\frac{2i_{o+}}{\beta_A}} + V_{THN} \quad (3)$$

When i_{0-} starts to increase and i_{0+} starts to decrease (i.e, $i_{0-} >> i_{0+}$) the switching takes place when V_{DS} (M8) =V_{TH} (M9), Current through M7 is drawn away by M8 which decreases theV_{DS} of M7 and pushes M9 off. If v_{o+} or v_{o-} = $2V_{THN}$, then M8 and M9 operates in triode region. When the M9 voltage reaches V_{THN} it enters the saturation region, the current of M9 is

$$i_{o-} = \frac{\beta_B}{2}(v_{O+} - V_{THN})^2 = \frac{\beta_B}{\beta_A} i_{o+} \quad (4)$$

When M9 turns off and M8 gets on switching takes place. If $\beta_A = \beta_B$ and currents $i_{o+} = i_{o-}$ then switching takes place. Hysteresis is shown when βs is Unequal.

$$i_{o+} = \frac{\beta_B}{\beta_A} i_{o-} \quad (5)$$

Switching point voltages are derived from Eq.(1 to 5)

$$V_{SPH} = v_+ - v_- = \frac{I_{SS}}{g_m} \frac{\frac{\beta_B}{\beta_A} - 1}{\frac{\beta_B}{\beta_A} - 1} \; for \beta_b \geq \beta_A \quad (6)$$

And VSPL = - VSPH (7)

VSPL= Voltage at switching point Low; VSPH= Voltage at switching point High

Both Preamplifier and Decision stages are connected and shown in fig.5 with transistors M1-M11. Sweep the voltage from 0 to 5 volts by fixing voltage reference as 2.5 volts. That the positive output voltage is at logic 0 before 2.5 volt and at logic 1 after swept from 2.5 volt and also the negative output voltage is at high logic level that is logic 1 before it swept from the reference voltage. It is at logic 0 after crossing 2.5 volt. And as seen in waveform switching takes place at 2.5 volt.

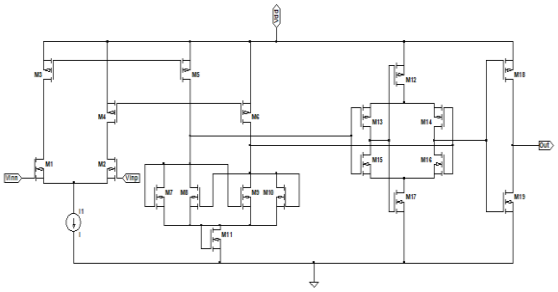

Fig.5: CMOS Comparator with Pre-amp, Decision and buffer circuit

The final output buffer stage accepts a differential input signal and convert the result of the decision circuit into a logic signal (i.e., 0 or 5V)without slew-rate limitations. Transistors M12-M19 represents output buffer circuit in the fig.5. Transistor M11 is added in series with the decision circuit to avoid problem in connecting the decision circuit to the output buffer directly by increase the average voltage. To increase the output of decision circuit by V_{THN} adjust W_{11}/L_{11}. The comparator schematic is shown in fig.5. Set the input voltage as reference parameter and sweep it from 0-5V. If the voltage is less than the chosen reference parameter the output is 0 logic and if it is greater than the selected reference then the output is 1 logic.MOS Comparator designed in cadence 180nm technology for 5V supply.

This design is implemented to achieve high gain and speed at low power dissipation. This is the three stages comparator based on pre-amplification. Performance is increased by using this circuit. DC sweep, ac analysis and transient analysis is done in Cadence Virtuoso tool [32]. The proposed design provides low power consumption since the decision circuit requires the current generated from the transistors M1 and M2 which is low and can be sent to decision circuit for comparison. This differential pair is sized in such a way that it provides minimum offset.

IV. RESULTS AND ANALYSIS

i) Transient analysis: comparator transient analysis is done by providing 40mV and 250MHz frequency to VP input, VN is fixed at voltage of 900mV. At input voltages pulse is given to both Vinp and Vinn with the width of 100ns. The amplitude of the pulse is varied as Vinp is given from 0 to 5 volts and Vinn is given from 5 to 0 volts. And the output is as shown above in fig.6. This shows that if positive voltage (V+) is larger than negative voltage (V-), result is 1 then if positive voltage (V+) is smaller than negative voltage (V-), result is 0. The time period of both the pulses is given as 200ns. The corner analysis is also done for transient response to find the slew rate variation according to 45 corners and it showed in the range of 10- 15 V/us as shown in fig.7.

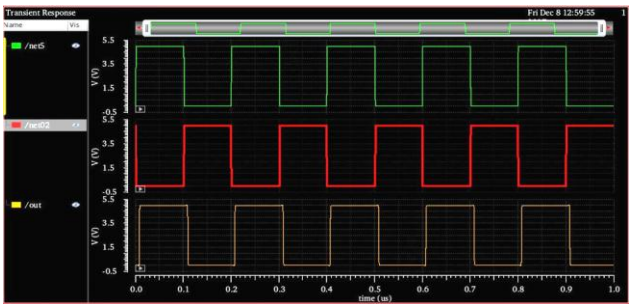

Fig.6 Waveform of transient response

ii)DC analysis: with the DC analysis, biasing conditions (node voltages, loop and branch currents and operating point) of the circuit can be finding. From this it can be observed that what would happen if simply turned the circuit on and applied no signal to it. During DC analysis of this comparator, same input parameters are applied as for double clock preamplifier based comparator. Offset voltage obtained is approximately 18 mV. The corner analysis is done in cadence by using ADE GXL. The analysis is dc analysis with sweep from 2.49 to 2.50 volts with the step of 0.005 volts. The outputs plotted are selected from the design and shown in fig.8.

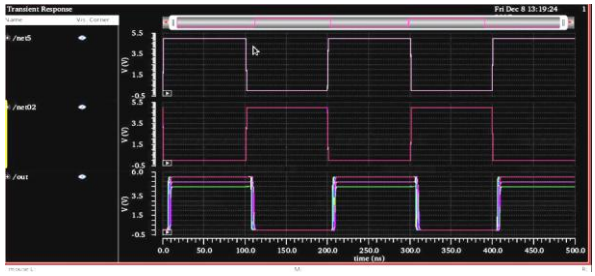

Fig. 7: Transient analysis for 45 corners

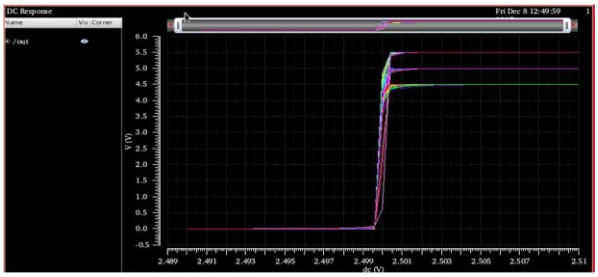

Fig. 8 DC analysis for 45 corners

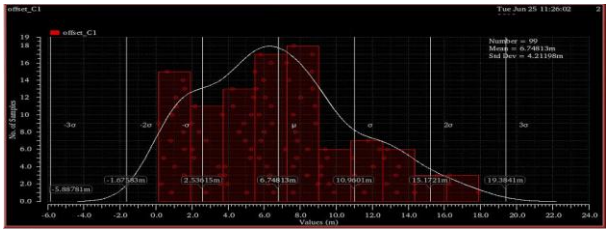

Fig. 9 Monte Carlo analysis for off set

This graph depicts that there are 45 graphs of DC analysis at three different temperatures as -40°, 27° and 125° with the variation in the supply voltages as 10% of 5 volts that is 4.5, 5 and 5.5 volts the variation of minimum and maximum voltage offset is obtained as 5mV to 9mV.

iii) AC analysis: After finding the bias conditions, AC analysis uses to find the frequency response of the analog circuit. The AC analysis figure out what happens to the circuit when applying a well behaving AC signal as the input.

Since the main parameter of comparator considered for ADC and DAC is speed and accuracy, we have done DC and transient analysis for obtaining the offset and slew rate. Monte Carlo Analysis: After DC analysis we need to find the offset due to mismatch and process variations for which we have simulated Monte Carlo analysis by taking 100 samples and the graph is shown in fig. 9. The mean value of 6.748mV and standard deviation of 4.21mV , offset is obtained. From table 1 the designed comparator shows a minimum offset and lower powerconsumption and used to implement the ADC.

Table 1: Performance comparison table of different comparators

S.No.	Parameter	Specs. Value	This work	[33]	[34]	[35]	[36]	[37]
1	Technology ,µm	0.18	0.18	0.35	0.35	0.18	0.18	0.18
2	Supply Voltage, V	5	5	3.3	3.3	1.5	3.3	1.8
3	Input Offset Voltage, mV	5	8.4	16	50	8.27	21.9	7.99
4	ICMR Range,V	1-4	0-5	0-2.5	0-3	0-1.2	0-1.65	0-1.8
5	Slew Rate, V/µS	10	14.68	11.35	14.72	17.87	33	
6	Load Capacitance, pF	2	2	5	5	1.72	1.11	1.49
7	Bias Current,µA	20	25	-	-			
8	Power consumption, mW	2.5	1.5	21.38	25.66	11.5	18.2	10.2

V. CONCLUSIONS

CMOS Comparator is designed in cadence virtuoso using SCL's 0.18µmtechnology at 5V supply.The simulation results showed that the designed comparator consumes a power of 1.5mW providing an offset of 8.4mV and slew rate of 14.68V/µS, for a high speed and accurate comparison comparator used in Analog to Digital converter.

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