

Low Power and Area Efficient Full Adder using GDI and 2T XNOR

Radhika P, Aswathi Gopan

Abstract— This paper portrays plan of low electricity and vicinity gifted based complete viper utilizing GDI approach. Full snake utilizes 2T XNOR entryway utilizing skip transistor cause. In full viper, low power utilization and least unfold deferral are done via skip transistor rationale and door dissemination enter technique. GDI applied for low energy computerized combinational circuits gives lower in power, deferral and sector of the circuits by means of preserve up the low multifaceted nature of the motive layout. GDI based AND or potentially is utilized. Skip transistor approach lower the amount of transistors. The proposed snake reduced parameters, as an example, manipulate usage, postponement or power-defer object. Undertaking results display that, within the proposed snake eleven. Seventy eight% decreased in power usage and 16.05% in spread defer while contrasted and present viper. The proposed snake is orchestrated utilising CADENCE 5.1.0 EDA device and reenacted using ghost virtuoso.

Keywords— Full adder; Gate Diffusion Input(GDI)Technique; Pass Transistor Logic(PTL); 2T XNOR; CADENCE tool

I. INTRODUCTION

The essential element of various automated circuits is snake and it likewise assumes the significant activity in diverse multiplier to determine the entire of fractional objects. Growth of paired numbers assumes massive activity in variety-crunching unit. Decrease in entire electricity usage through making plans elite adders. The proposed framework is displayed with advanced in parameters like energy, postponement and transistor tally [1].

The GDI machine offer utilization of complex capacities using just less range of transistors. This method is beneficial for structure of speedy, using less number of transistors (while contrasted with CMOS)while improving reason degree swing and static strength and permitting honest top-down plan by using using much less number transistor mobile library.

Vicinity II subtleties the door dispersion enter. Section III clarifies the modern-day framework. The engineering of the proposed framework is clarified in the segment IV. Phase V offers the examination of the proposed and present full snake. Segment VI depicts the quit.

II. GATE DIFFUSION INPUT TECHNIQUE

The GDI [7] cell is designed by one PMOS and NMOS transistor. GDI structure is like a CMOS inverter. The

difference between GDI and CMOS inverter, GDI contains two extra inputs is given in the Fig 1.

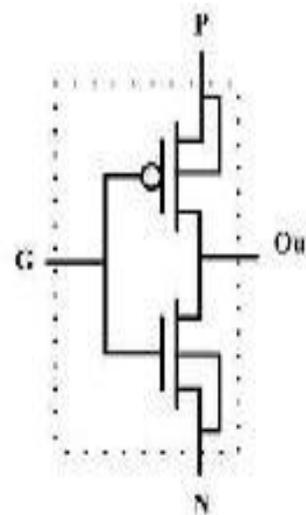


Fig. 1. Basic GDI cell [1]

The one of the two extra inputs is P and N. According to the input of two extra input, it determines which function that cell act. The source terminals of PMOS and NMOS are connected to supply voltage (vdd) and ground [1].

III. EXISTING SYSTEM

In existing system the full adder is modeled using GDI-MUX and pass transistor is given in Fig.2.

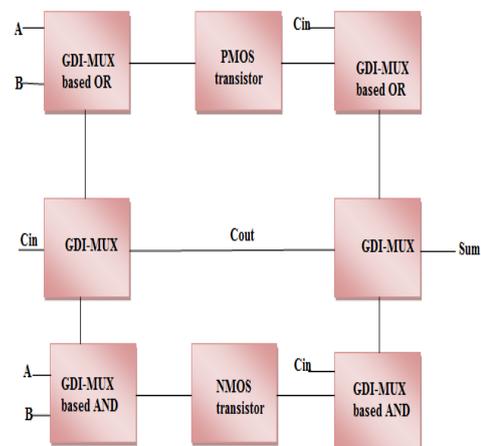


Fig.2. Block diagram of existing system [1]

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Table I and Table II shows the expression for cout and sum. Both functions are carried out by using GDI MUX. According to the input Cin, MUX decides whether it works as AND and OR.

TABLE I. EXPRESSION FOR COUT

Cin	Cout
0	A AND B
1	A OR B

TABLE II. EXPRESSION FOR SUM

Cout	Sum
0	A AND B AND Cin
1	A OR B OR Cin

Circuit diagram of the existing full adder shows in fig 3. There are 14 transistors used in existing system. The full adder designed using GDI and pass transistor^[11] logic allow low power consumption and delay

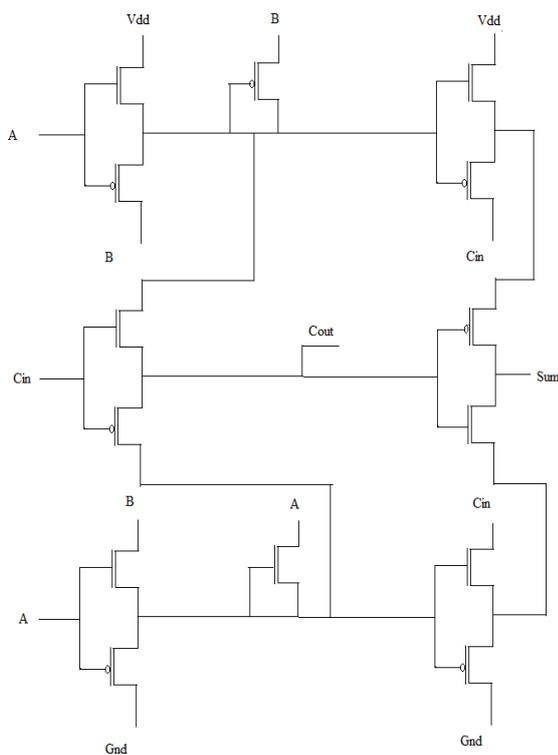


Fig.3. Circuit diagram of Existing system^[11]

IV. PROPOSED SYSTEM & RESULTS

Figure 4 shows the block diagram of proposed system. Consists of 2T XNOR using pass transistor logic and GDI based OR, AND.

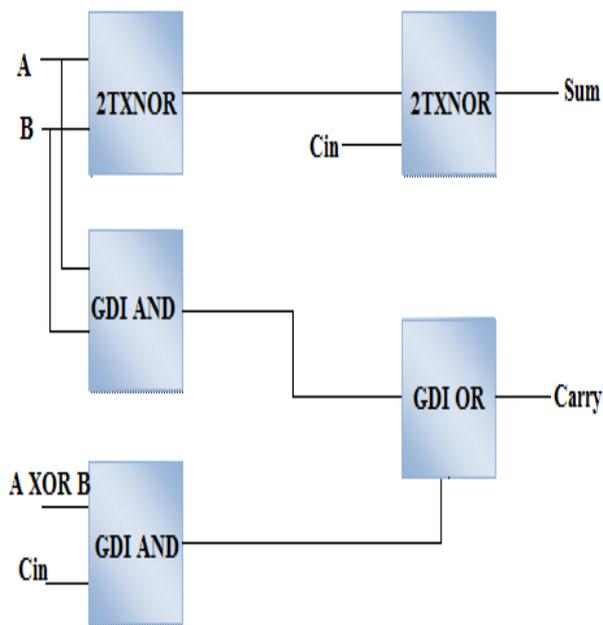


Fig.4. Block diagram of proposed system

A. Sum section

The output sum of the adder is carried out by two 2T XNOR shown in fig.5. The expression is given by,

$$Sum = A \odot B \odot Cin$$

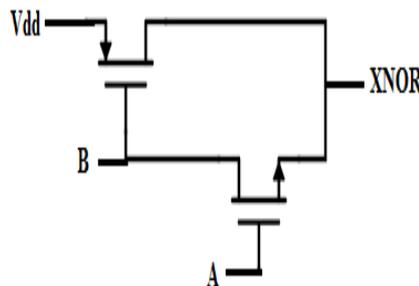


Fig.5. 2T XNOR^[6]

The XNOR function, when the input is AB=00, 01, 11 the output signal is perfect. When AB = 10, the output offer poor high impedance because NMOS is on.

B. Carry section

Output Cout is generated with the help of GDI technique. The expression for cout is given by,

$$Cout = AB + (A \oplus B)$$

So here GDI based OR and GDI based AND in the carry section is used given in the fig.6 and fig.7 respectively.

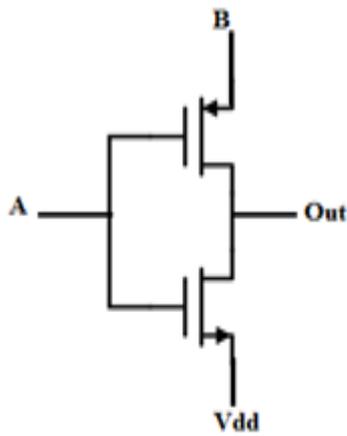


Fig.6.GDI based OR^[1]

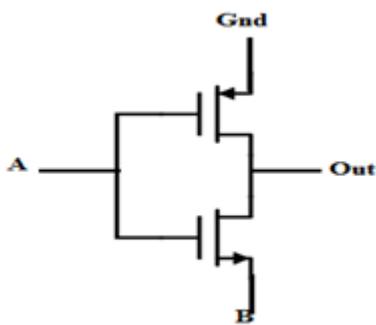


Fig.7.GDI based AND^[1]

V. SIMULATION RESULTS

The proposed system is synthesized using CADENCE 5.1.0 EDA tool and simulated using spectre virtuoso. Fig.8 shows the RTL schematic diagram of the proposed system.

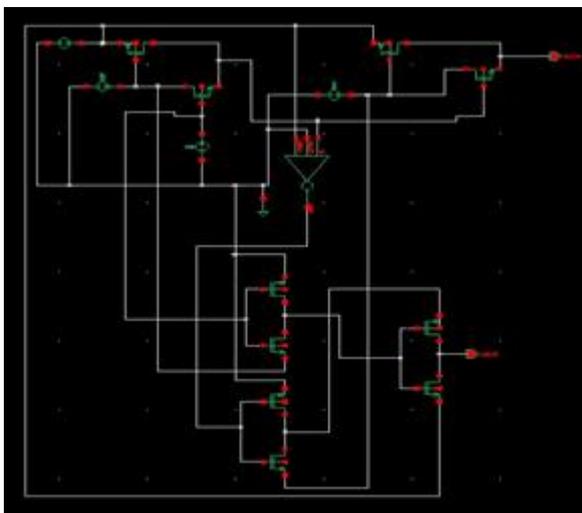


Fig. 8. Schematic diagram of proposed system

Fig.9 shows the transient response of the proposed full adder.

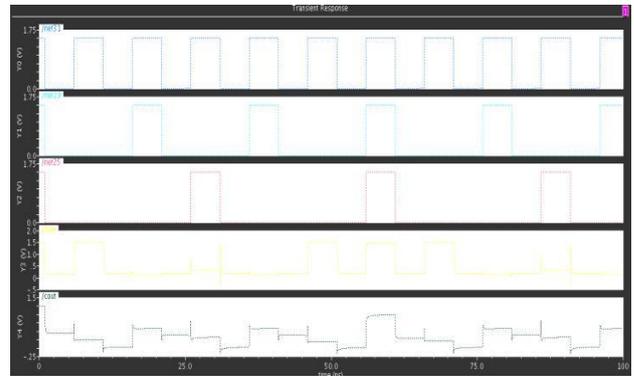


Fig.9. Transient response of proposed system

Fig.10 and Fig.11 shows the power and delay calculation in cadence.

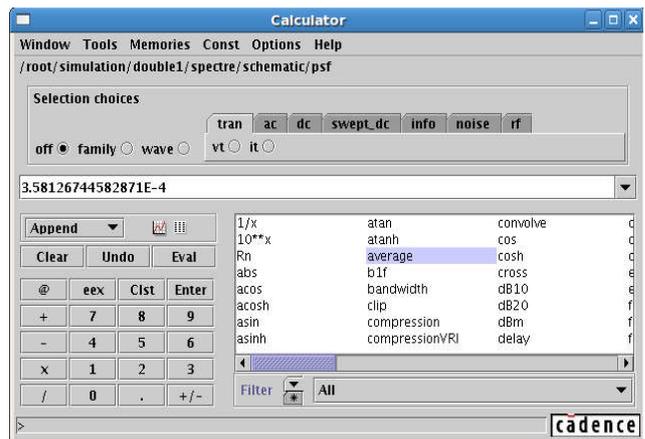


Fig.10.Power calculation in cadence

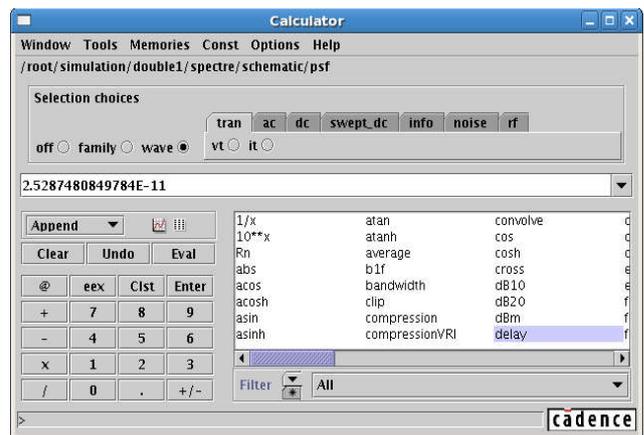


Fig.11.Delay calculation in cadence

Table III shows Comparisons between the proposed framework and existing framework. From this table it clears that the circuit multifaceted nature of proposed framework is less and furthermore the power utilization of the snake is 0.3408 μ W and furthermore the spread deferral of the proposed viper is 0.2231ps which is extremely less when contrast and the current framework.

TABLE III. COMPARISONS TABLE

Parameters	Existing System	Proposed system
Transistor count	14	10
Power(μ W)	0.3581	0.3408
Delay(ps)	0.2528	0.2231
Power delay product(pdp)	0.0905	0.0760

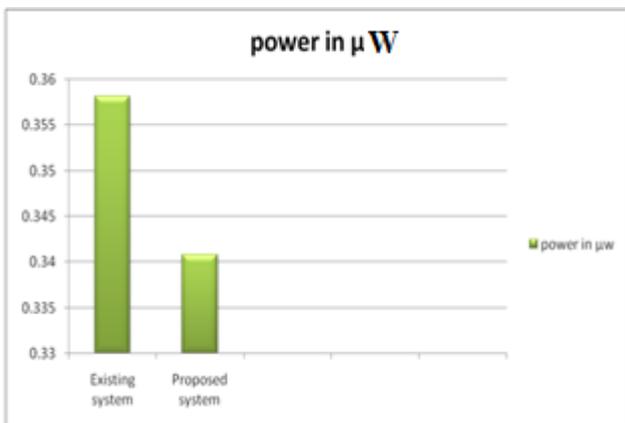


Fig 12. Graphical representation of power

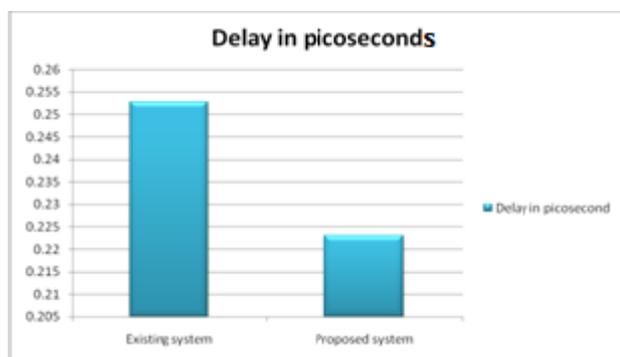


Fig 13. Graphical representation of delay

VI. CONCLUSION

Proposed a low power location effective full viper utilising GDI and 2T XNOR. In full snake, low power usage and least proliferation deferral are executed via pass transistor cause and door dispersion enter gadget. The proposed full viper has regular power utilization of 0.3408 μ W with a postponement of 0.2231ps which is much less when contrasted with present full snake plan. Complete snake has been dependent and recreated using CADENCE five.1.Zero EDA device and reenacted making use of apparition virtuoso.

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