

High Performance Reversible Vedic Multiplier Using Cadence 45nm Technology

S.Prema, Ramanan.S.V, R.Arun Sekar,Rajan Cristin

Abstract: Vedic science is an antiquated strategy of Indian arithmetic as it contains 16 Sutras. A fast 16 *16 multiplier configuration is designed utilizing Urdhva Tiryakbhyam sutra is introduced in this work. By utilizing this sutra the fractional items and entireties are created in single stage which decreases the structure of design in processors. By utilizing this method we can diminish the delay to the maximum extent when contrast with cluster or corner multiplier. By utilizing this strategy we lessen the inciting delay in connection with bunch based plan and parallel carry based use which are most normally used models. The essential significance of this paper is the delay and dynamic power usage is found to be diminished.

Keywords: Wallace tree multiplier, Vedic multiplier (VM), Reversible logic

I. INTRODUCTION

Augmentation is a central capacity in math activities dependent on several tasks. Adders form the fundamental basic structure of the multiplier. Generally subtraction is a two's complement addition. These arithmetic operations should be performed in the fastest manner for high speed applications. Once these operations are performed in high speed, then they can be used to speed up the operations of the complicated circuits. So designing the efficient adder is in the front line. Further due to the advancement in the technology, several parameters like wire length, number of fan outs are also taken into account. Reversibility in processing suggests that no data about the computational states can ever be lost, so we can recoup any prior stage by registering in reverse the outcomes. This is named as logic reversibility. The condition of inputs can be recuperated from the outputs by using the concept of reversible logic components. This reversible logic is used in adders and reversible adders are designed. The adder block in the Vedic multiplier are replaced by this reversible adders to form the reversible Vedic multiplier (VM). This proposed Reversible VM proved to be the best when compared with the existing Wallace tree multiplier and conventional VM in terms of delay and power consumption.

The operation and functionality of Wallace tree multiplier is described in the section II. VM methodology is described in the section III. The proposed reversible VM is described in the section IV. Implementation of proposed method in Cadence 45nm technology is explained in the section V. The result discussion for this work is explained in the section VI.

II. WALLACE MULTIPLIER

Eminent quick multipliers are Wallace multiplier [1,2] which uses carry save adders to decrease N-sections of fragmented things to two line lattice. The carry save adders are standard full adders whose carry are not related, with the objective that three words are taken in and two words are yield. The Wallace multiplier uses half adders and full adders in their decrease arrange. Here a balanced framework is shown that altogether lessens the half adders. In Wallace multiplier, in the second step of decrease the Wallace approach uses a couple of periods of full adders and half adders as carry save adders. In the Wallace multiplier the incomplete item decrease arrange uses carry save adder. The quantity of full adders and half adders used are 50 and 20 individually. Four phases are required for decrease. In the middle of the road stages and the last carry propagate phase of standard Wallace tree multiplier, the Carry propagate adder is associated.

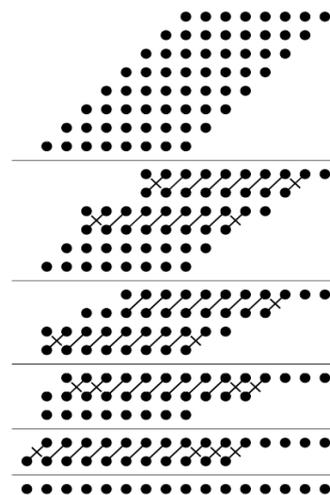


Figure 1 Schematic of Wallace multiplier

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III. VEDIC MATHEMATICS

The utilization of Vedic science is to decrease the regular figuring's in traditional science to exceptionally basic one. It additionally gives viable calculations that to be connected to different parts of designing, for example, registering.

A. Urdhva Tiryakbhyam Sutra

"Urdhva Tiryakbhyam" sutra is used in our proposed Vedic multiplier [3]. The augmentation of any two decimal formatted variables is performed by using this sutra. This sutra operates in both crosswise and vertical direction. This sutra is one among the 16 sutras and is based on the ancient vedic mathematics. Here all the partial products generation and the addition take place concurrently. Further this sutra is based on the addition equation which is utilized for the multiplication. Because of its normal schematic, it tends to be effectively format in microchips and planners can without much of a stretch bypass these issues to maintain a strategic distance from calamitous gadget disappointments. The Vedic multiplier (VM) module for different bits is explained as below.

B. VM for 2*2 piece Module

The operation of 2*2 VM where the 2-bit numbers X and Y are $X = x_1x_0$ and $Y = y_1y_0$. The minimum noteworthy bits are duplicated which gives the minimum huge piece of the last item (vertical). At that point, the multiplicand (LSB) is duplicated with the following multiplier upper piece and included with, the result of multiplier LSB and next multiplicand (across) Upper piece. The procedure goes on in a similar way. The operational structure of the two bit VM is given in the following equations.

$$p_0 = x_0y_0; \quad (1)$$

$$z_1p_1 = x_1y_0 + x_0y_1; \quad (2)$$

$$z_2p_2 = z_1 + x_1y_1; \quad (3)$$

The last outcome will be $z_2p_2p_1p_0$. This augmentation strategy is appropriate for all the cases. Generally four AND gates and two HA are utilized for implementing 2*2 VM module. Even though it is similar to the conventional array multiplier, the main purpose of designing 2*2 VM is, it can be used for designing 4*4 VM and so on.

C. VM for 4*4 bit Module

The schematic diagram of 4*4 VM module is shown in the figure 2. The operation is similar to 2*2 VM module. In the equations represented below the two 4-bit binary numbers $X_3X_2X_1X_0$ and $Y_3Y_2Y_1Y_0$ multiplication. Due to this multiplication nearly 8 bits namely $P_0P_1P_2P_3P_4P_5P_6Z_6$ are produced as the output.

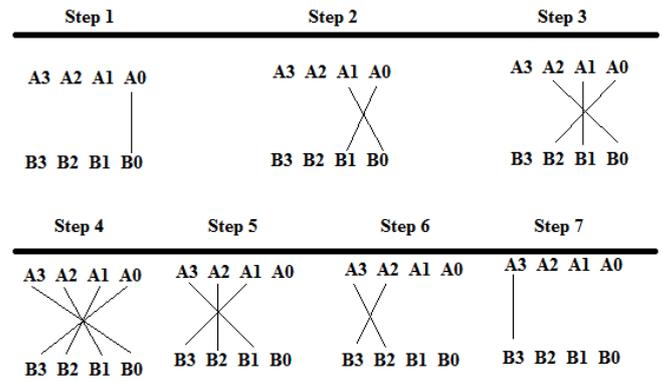


Figure 2 4*4 bit binary multiplication using Urdhva Tiryakbhyam

$$p_0 = x_0.y_0 \dots\dots\dots (4)$$

$$z_1p_1 = x_1y_0 + x_0y_1 \dots\dots\dots (5)$$

$$z_2p_2 = z_1 + x_1y_1 + x_2y_0 + x_0y_2 \dots\dots\dots (6)$$

$$z_3p_3 = z_2 + x_3y_0 + x_0y_3 + x_1y_2 + x_2y_1 \dots\dots\dots (7)$$

$$z_4p_4 = z_3 + x_3y_1 + x_1y_3 + x_2y_2 \dots\dots\dots (8)$$

$$z_5p_5 = z_4 + x_3y_2 + x_2y_3 \dots\dots\dots (9)$$

$$z_6p_6 = z_5 + x_3y_3 \dots\dots\dots (10)$$

D. VM for 16*16 bit Module

16*16 VM is designed using four 8*8 VM and three 16-bit Ripple Carry Adder (RCA). Here X and Y are 16-bit binary numbers.

$$X[15:0]:x_{15}x_{14}x_{13}x_{12}x_{11}x_{10}x_9x_8x_7x_6x_5x_4x_3x_2x_1x_0$$

$$Y[15:0]:y_{15}y_{14}y_{13}y_{12}y_{11}y_{10}y_9y_8y_7y_6y_5y_4y_3y_2y_1y_0.$$

The first stage has only a single 8-bit VM. The 8-bit VM is built using two 4-bit VM where the 4 bit is built up by two 2-bit VM. Here the output of the first stage is the 16-bit output. The LSB of the output [7:0] is taken directly whereas the MSB [15:8] is fed to the RCA. Segregation of the input bits at the upper stage takes place. The Schematic diagram of 16-bit VM is shown in the figure 3. Zero padding takes place in one of the RCA to the make the width of the bits equal to the RCA width. Figure 3 clearly explains about the operation of the conventional VM. Here the larger blocks are reduced to half and further reduced to the least level. For example if it is of 8x8 VM block, they are reduced to two 4x4 VM block and further each 4x4 VM block is reduced to two 2x2 VM block. Finally the product [31:0] is calculated.

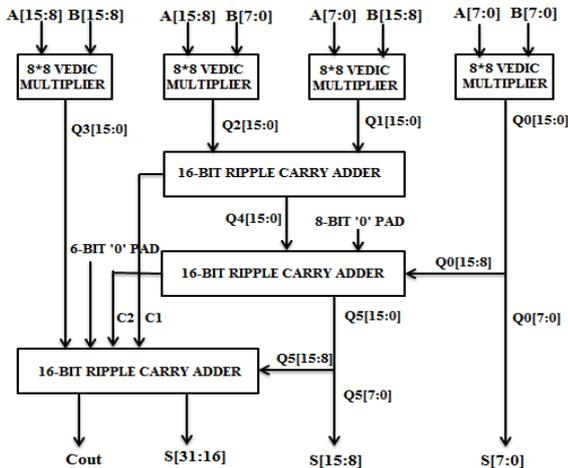


Figure 3 Schematic diagram of 16x16 normal VM

IV. REVERSIBLE GATES

An n input and n output logic is utilized in reversible gate. The representation is called as one to one mapping. The outputs can be easily determined from the inputs meanwhile the inputs can also be obtained from the outputs. Since one to many concept is not reversible, direct fan out is not allowed during the synthesis of reversible circuits. Any how we can achieve the fan out in the reversible circuits by utilizing additional gates. While designing the reversible circuit we must keep an eye on using the number of reversible logic gates to be minimum. The complexity and the performance of the circuit are determined by number of factors.

A. BME Gate

BME is a 4*4 reversible gate. It has four inputs and four outputs. The information is given by i(A,B,C,D) and the response is represented by o(P,Q,R,S). The output is defined by $P = A$, $Q = AB^{\wedge}C$, $R = A.D^{\wedge}C$ and $S = (A^{\wedge}B^{\wedge}C^{\wedge}D)$. Figure 4 shows the block diagram of BME gate. Figure 5 shows the schematic of BME reversible gate.

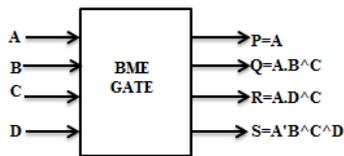


Figure 4: Block diagram of Reversible BME gate

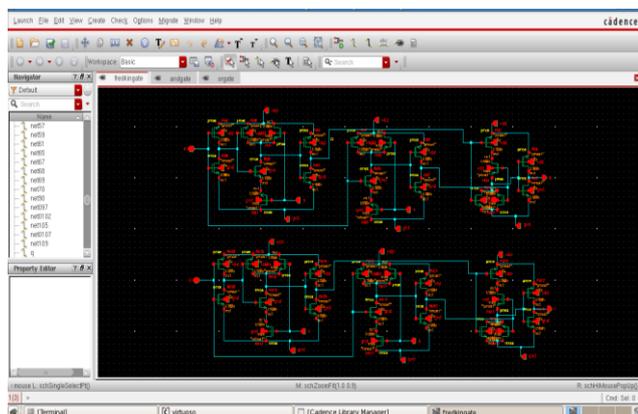


Figure 5: Schematic of Reversible BME gate

B. Peres Gate

One form of 3*3 reversible entryway is the Peres gate. It has three information sources and three output responses. The illustration of Peres entryway is indicated below in the Figure 6 and Figure 7 shows the schematic of reversible Peres gate by using Cadence tool. The response is given by A , $Y = A^{\wedge}B$, $Z = AB^{\wedge}C$. Peres gate has the Quantum cost of five.

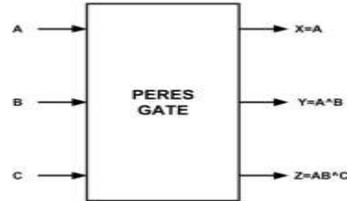


Figure 6 Block diagram of Reversible Peres Gate

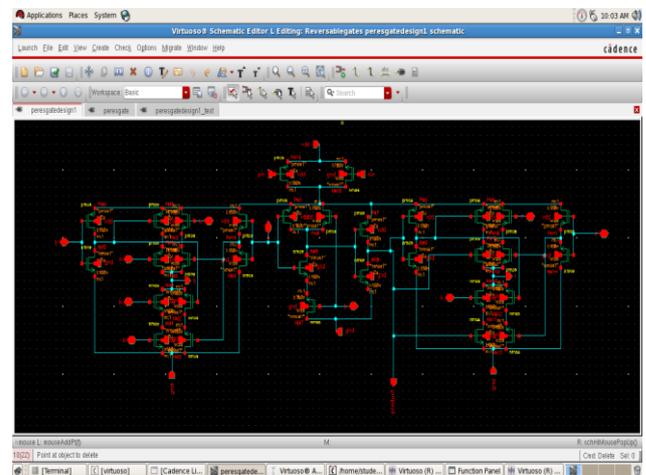


Figure 7 Schematic of Reversible Peres gate

V. REVERSIBLE 2*2 VM

While designing 4*4 Reversible VM [4-7], it is constructed using two 2*2 Reversible VM. The Block diagram of Reversible 2*2 VM is shown in the Figure 8. Reversible 2*2 multiplier is designed using two BME gate and two PERES gate. The first BME gate produces the sum p0 which is the product of the LSB x0 and y0. Both the two BME gate produces two garbage outputs. One of the outputs of both the BME gate are fed to the PERES gate and the higher order bits of the sum s1, s2 and s3 are generated.

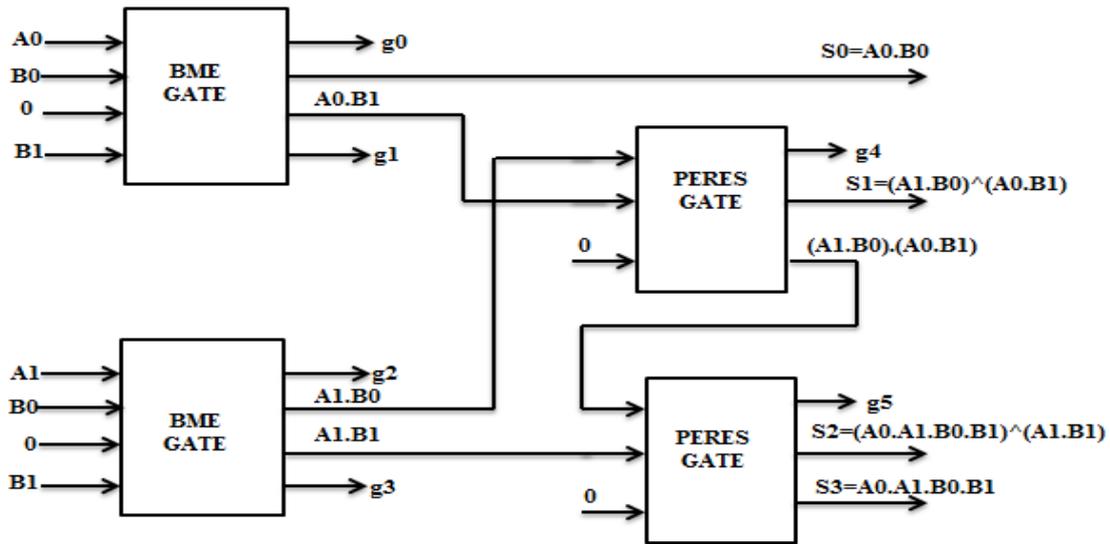


Figure 8 Schematic diagram of Reversible 2*2 VM

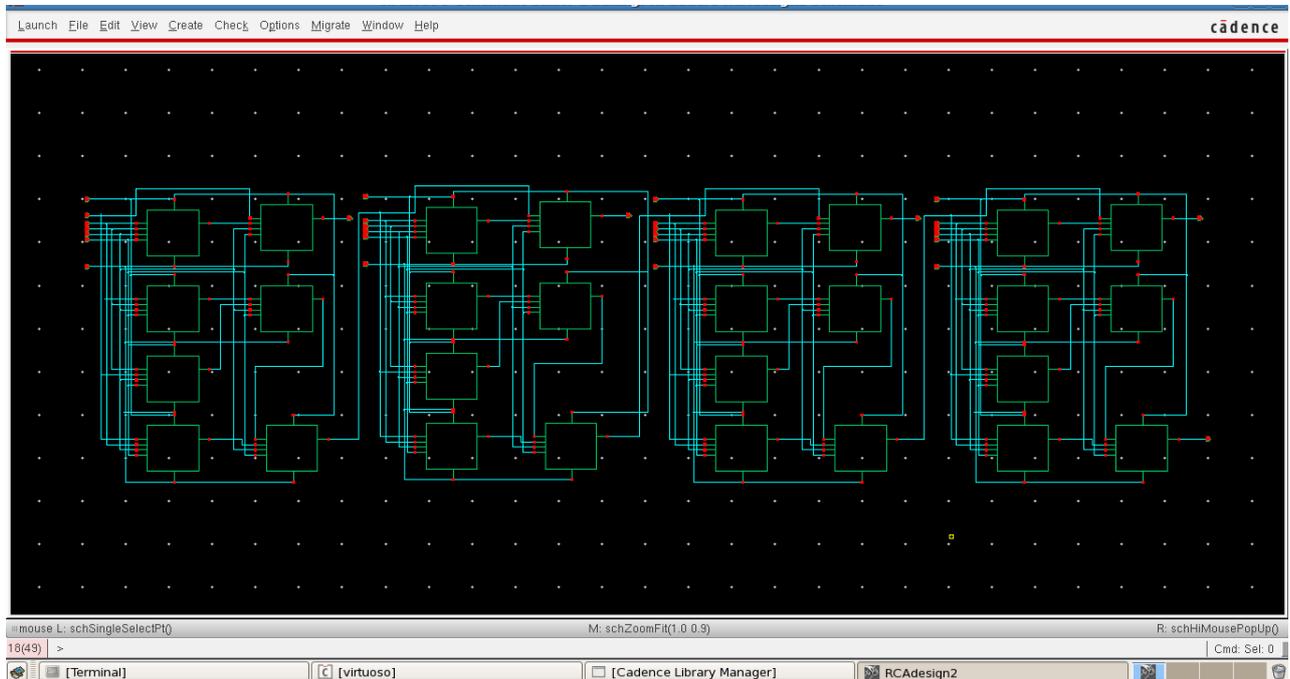


Figure 9 Schematic of Reversible 16*16 Vedic multiplier

Schematic of Reversible 16*16 VM [8-11] is shown in Figure 9. Reversible 16*16VM is designed using multiple stages of 8x8 reversible VM which is constructed from 4x4 Reversible VM and so on. The first stage has only a single 8-bit Reversible VM. The 8-bit Reversible VM is built using two 4-bit Reversible VM where the 4-bit is built up by two 2-bit Reversible VM. Here the output of the first stage is the 16-bit output. The LSB of the output [7:0] is taken directly whereas the MSB [15:8] is fed to the Reversible RCA.

Segregation of the input bits at the upper stage takes place. Zero padding takes place in one of the RCA to the make the width of the bits equal to the RCA width. Here the larger blocks are reduced to half and further reduced to the least level. Finally the product [31:0] is calculated.

VI. RESULTS AND DISCUSSION

Table 1 Comparison of Different Multipliers

MULTIPLIER	CELLS	AREA	TOTAL POWER(nW)	DELAY (pS)
WALLACE MULTIPLIER	3562	1873 2	7642414.8	12932
NORMAL VM	736	7125	363926.99	6024
REVERSIBLE VM	1945	9844	281869.6	5353

Table 1 shows the comparison result of different multipliers. It is generally noted that the VM has lowest delay and low power when compared to other types of multipliers. But when reversible logic is applied to this multiplier, it is seen that the power and delay are further reduced. The delay is reduced by 11.13% and the power is reduced by 22.54%. Figure 10(a) and Figure 10(a) shows the pictorial representation of the comparison result. Simulations are performed using Cadence 45nm technology.

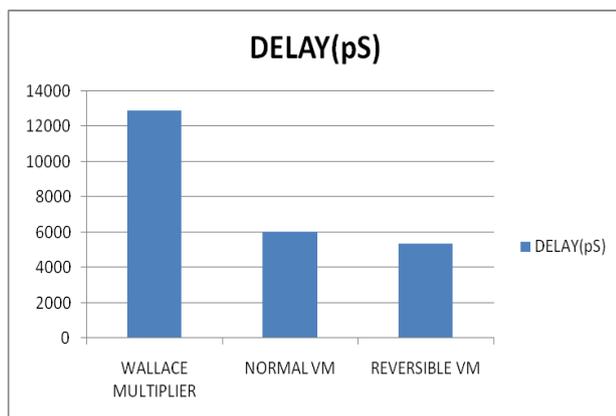


Figure 10(a) Delay comparison of different multipliers

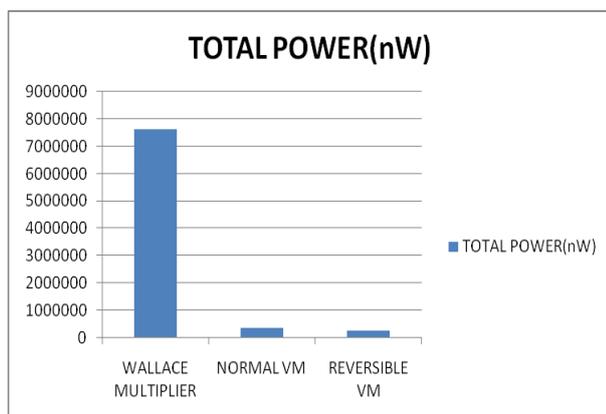


Figure 10(b) Power comparison of different multipliers

REFERENCES

- Wallace C.S, "A Suggestion for a Fast Multiplier", IEEE Transactions on Electronic Computers, Vol.13,1964, pp. 14-17.
- Waters R. S. et.al., "A Reduced Complexity Wallace Multiplier Reduction," IEEE Transactions on Computers, vol. 59, 2010, pp. 1134-1137.
- Sushma R.Huddar et.al., 'Novel Vedic mathematics multiplier using compressors', International Multi-Conference on Automation, Computing, Communication, Control and Compressed Sensing,2013.
- Rakshith S, Rakshith T, 'Optimized Reversible Vedic Multipliers for low power operations' IEEE Conference on Information and communication Technologies, 2013.
- Thapliyal, H and Srinivas, M, B, "Novel Reversible Multiplier Architecture Using Reversible TSG Gate", Proceedings on IEEE International Conference on Computer Systems and Applications, 2006, pp. 100-103.
- Shams, M, Haghparast, M and Navi, K, "Novel Reversible Multiplier Circuit in Nanotechnology", World Applied Science Journal, Vol. 3, No. 5, 2008, pp. 806-810.
- Koti lakshmi, Santhosh kumar and Rameshwar Rao, 'Implementation of Vedic Multiplier Using Reversible Gates', International Conference on Computer science and Information Technology, 2015, pp 125-134.
- Vijay K Panchal and Vimal H Nayak, 'Analysis of multiplier circuit using reversible logic', International journal for Innovative Research in Science and Technology, Vol 1, Issue 6, Nov 2014.
- Ratna Raju et.al., 'A High Speed 16*16 Multiplier Based on Urdhva Tiryakbhyam Sutra', International Journal of Science Engineering and Advance Technology, Vol 1, Issue 5,2013.
- Vishikha Sharma, Aniket Kumar, "Design, Implementation & Performance of Vedic Multiplier for Different Bit Lengths", International Journal of Innovative Research in Computer and Communication Engineering, Vol. 5, Issue 4, April 2017.
- R Arun Sekar, S Sasipriya, "Implementation of FIR filter using reversible modified carry select adder", Concurrency and Computation: Practice and Experience, Sep.2018, pp. 1-9.

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