Implementation of Low-Power 1-Bit Hybrid Full adder with Reduced Area

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Abstract: ***In this investigation a low power 1-bit hybrid full adder (FA) and 4-bit full adder circuits where designed with the proposed 1-bit full adder. By utilizing CMOS and Pass transistor logics a new XNOR logic is implemented. The voltage degradation problem can be overcome by employing the CMOS weak inverters. By using this power consumption can be improved. By utilizing two transistors, carry logic module is designed. The circuit is operated at 1.8v. The circuit is designed using 125nm technology and tanner EDA tool is employed to perform the simulations. For the proposed design of full adder the power consumed is of 763.5 nW and the delay is 41.03 ps.***

Index Terms*: Area, Full adder, Power, Tanner EDA software, XNOR.*

I. INTRODUCTION

The advancements in the VLSI technology and the demand for the low power, less delay and increasing the operating speed of the device [3]. The main goals in VLSI is minimizing the transistor count, increasing the speed and minimizing the power consumption. Arithmetic operations (Addition, Multiplication etc.) are used in many of the VLSI applications. In almost all algorithms full adder is used. The adder is a standout amongst the most basic segments of a processor that is included in the building block of Arithmetic logic unit [9]. Generally designs of adders are divided into two logic styles, static and dynamic logic styles [2]. The logic style is chosen based on the requirement. Requirement of less power makes the static full adders simple, and reliable. The main problem in static full adders is area required is more when compared to dynamic full adder [10]. Now in dynamic full adder, there are some advantages compared to the static logic styles, like fast switching speed, full swing at output etc. Hybrid full adders are utilized in the battery – worked minimal devices, for example, mobile telephones, PDA's, and note pads which require in VLSI, and Ultra Large Scale Integrated circuits (ULSI) plans with a superior power postpone angles [8]. It is utilized in the Processor chip like Intel Pentium for CPU part, which comprises of ALU. This is utilized to do the tasks like subtraction and so on [4]. In this research 1- bit full adder design is proposed using revised carry logic module and XNOR module, that consumes very less power than that of the existing circuits. Utilization of XNOR in the full adder reduce the power consumption by introducing a weak inverters.

Revised Manuscript Received on May 10, 2019

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TABLE I
1-Bit FA Truth Table

A	B	C_{in}	C_{out}	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

The yield convey is assigned as C_{out} and the typical yield is assigned as S.

$$SUM = A \oplus B \oplus C_{in}$$
$$C_{out} = A\,B + B\,C_{in} + C_{in}\,A$$
$$= C_{in}\,(A \oplus B) + A\,B$$

II. FIGURES

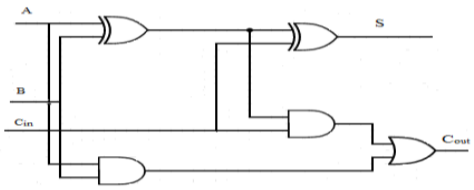

Fig.1 Full Adder circuit using logic gates.

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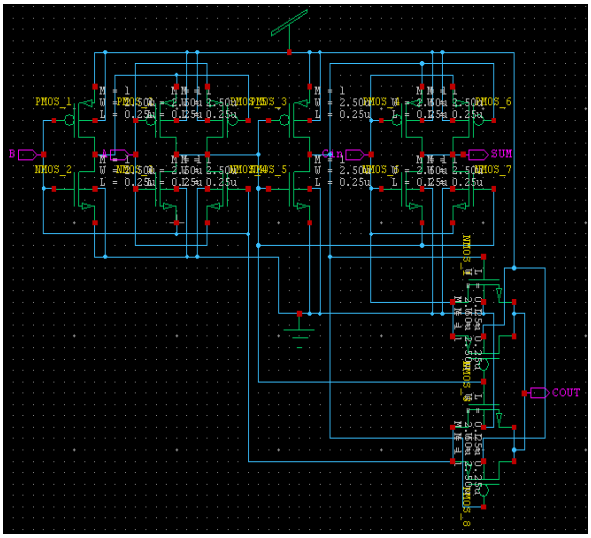

Fig.2 Existing Full Adder circuit using CMOS transistor circuit

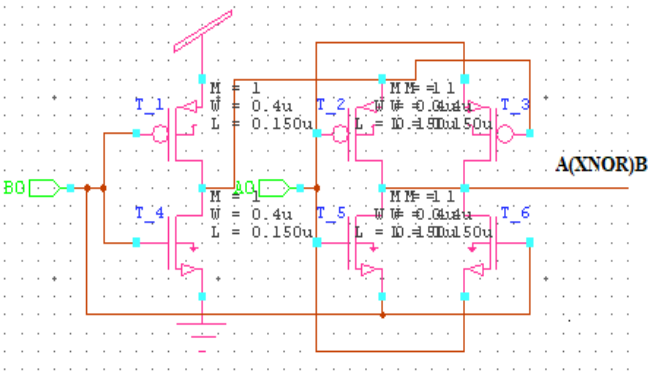

Fig.3 XNOR Module

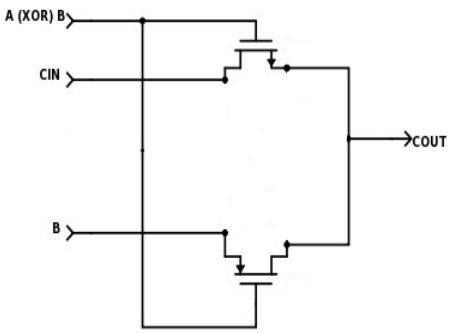

Fig.4 Modified Carry Generation Module

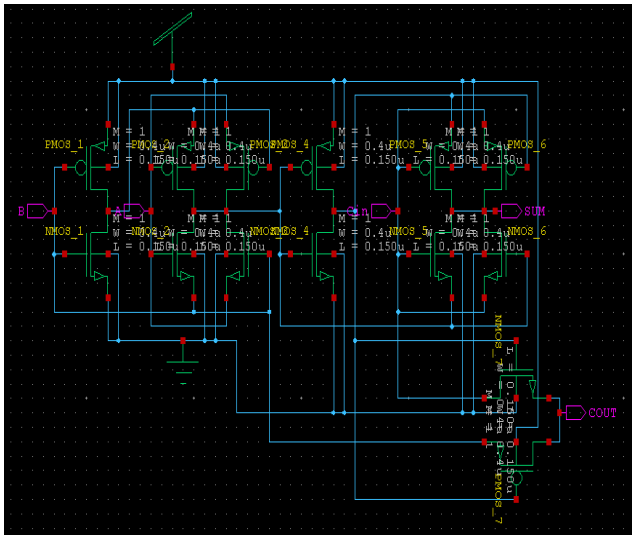

Fig.5 Modified Full Adder

XNOR Module:-

By using XNOR module the power consumption is also dominated with introducing a Buffer which have small channel width, consisting of T_1 (Transistor 1 PMOS) and T_2 (Transistor 2 PMOS). Buffer output is used to form a controlled inverter using T_3 (Transistor 3 PMOS) and T_4 (Transistor 4 NMOS) transistor. Whereas T_5 (Transistor 5 NMOS) and T_6 (Transistor 6 NMOS) form a level restorer that is responsible for full swing of the output signal [5-6]. XNOR module consists of six transistors in a manner that, the power is consumed less [7].

Modified Carry Logic Module:-

The Carry logic module is modified and shown in the Fig.4. Carry logic module consists of 2 transistors (i.e. 1-PMOS and 1-NMOS), carry signal is responsible to estimate delay.

1-Bit Full Adder:-

Adder is imperative component in PCs. Parallel expansion is one of the essential task in PC number juggling. Generally a 1–bit full adder is an arithmetic operation used for adding (A, B, C_{in}) three inputs of a full adder. The outputs are sum and carry. The existing (Fig.2) and proposed full adder (Fig.5) have two blocks. First one is two XNOR modules that will produce the SUM and one Carry generation module i.e. for producing C_{out}.The existing full adder consists 16 transistors in total i.e. 8-PMOS and 8-NMOS transistors. In proposed full adder 1-PMOS and 1-NMOS transistor is removed, resulting the total transistors count to 14. The 4-bit Full Adder is designed using 4 modified 1-bit full adders.

TABLE II
Transistor sizes

Transistors	Width (W)	Length (L)
All transistors	400nm	125nm

III. RESULT:-

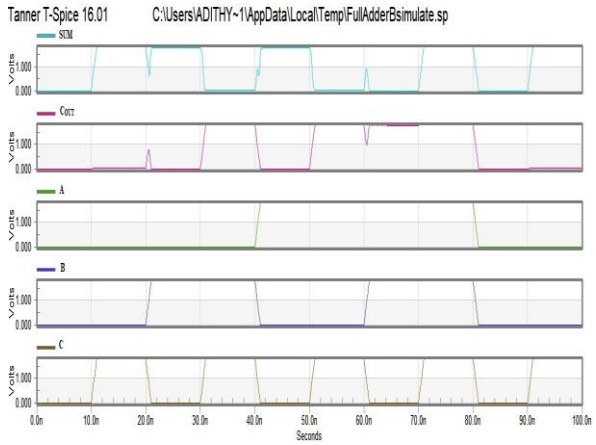

TABLE III
Parameters of Proposed Full Adder

Transistor count	Area (μm^2)	Power (nw)	Delay (ps)
14	88.31	763.5	41.03

4-Bit Full Adder:-

4 bit Full adder (FA) is an arithmetic (combinational) circuit that can be utilized to add 3 input bits to produce sum and carry outputs. A, B, C_{in} are inputs. The essential block for designing the 4- bit full adder (FA) is 1-bit full adder (FA) .The modified 1-bit full adder (FA) block is utilized to implement design.C_3 is the carry out of the circuit and sum(S_0,S_1,S_2,S_3). The first full adder (FA) C_{out} is given to the second full adder (FA) C_{in} .The second full adder (FA) C_{out} is given to the third full adder (FA) C_{in}. The third full adder (FA) C_{out} is given to the fourth full adder (FA) C_{in}. Simulation results are performed in tanner tools.

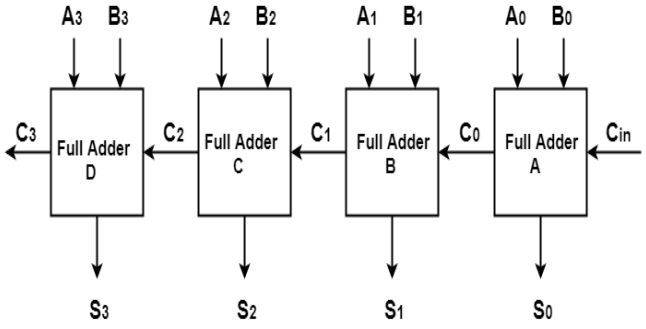

Fig.6 Ripple carry Adder

IV. CONCLUSION

A low power and high speed full adder circuit is designed and simulated in 125 nm technology, by introducing modified Carry generation and XNOR module into the circuit using Tanner EDA tool. From the simulated output it has been observed that the area of full adder circuit is reduced by 10% and the power consumed was found to be 763.5 nW which is less than the existing circuits and the delay is 41.03 ps.

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