Design Improvements in Power Amplifier for Making Energy Efficient Transceiver Blocks of Sensor Nodes

Saji. M. Antony, S. Indu, Rajeshwari Pandey

Abstract*: A wireless sensor network is an accumulation of sensor nodes in large quantities with limited energy resources. Thus, use of energy efficient power amplifiers is an essential requirement for sensor nodes as power amplifiers are responsible for the main power consumption in the transceivers of sensor nodes. The transceivers should operate at high data rate for better efficiency which allows many nodes to share same channel through time division multiplexing. Thus, wider band width is another important requirement for power amplifiers used in sensor transceivers. Reliability of a power amplifier can be increased by designing at smaller supply voltage.

This paper suggests improvements in design of power amplifier in class E configuration, for transceivers in wireless sensor nodes. In order to achieve wider band width, cascade of common drain followed by common source in class E configuration has been designed; and for more reliable operation with higher efficiency, class E in double cascoded has been implemented. The proposed designs are simulated in SPICE and higher efficiencies and band widths are achieved.

***Index Terms*: Class E power amplifier, Double cascoding; Low power transceivers, Power MOSFET, Switch mode power amplifier.**

I. INTRODUCTION

Current developments in computers, telecommunication and microelectronics have simplified the design of small size, multifunctional sensor nodes with low-power and low cost in large quantity. They can sense various information from the surroundings, like humidity, seismic vibrations, light, temperature, nature of biological organisms etc. Being very small in size, these nodes have embedded processing abilities. These nodes can have multiple sensors operating in infra-red (IR), seismic, acoustic and magnetic modes. A sensor network consists of densely deployed sensor nodes in a region to monitor a particular phenomenon. Sensor network is a fresh research area with applications in military surveillance, environmental/habitat monitoring, inventory tracking, medical monitoring, disaster management, traffic management and monitoring, smart home and more. Sensors are used to measure or monitor parameters that differ with time and location necessitating the need for the Dynamic Sensor Networks (DSN) [1]. Fig. 1 Shows Components of a Sensor Node.

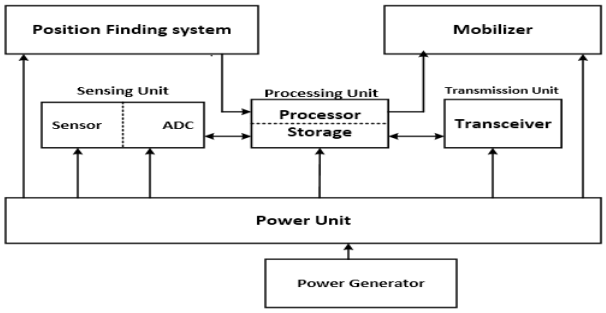

Fig. 1. Components of Sensor Node [2]

Life of a sensor network mainly depends on its energy consumption. Commercially available sensor nodes are battery driven devices. Due to plenty of sensor nodes installed in an isolated area and long lifespan requirement, replacing battery is not an option. So, energy optimization in sensor network is more complicated as it involves reducing the energy utilization and increasing the lifespan of sensor network.

In sensor nodes, power is consumed mainly in transceivers [3] and in transceivers, the most significant power consumption is attributed to power amplifiers [4]. This paper focuses on design of switch mode power amplifiers in class E configuration with high power efficiency. In [5], N O Sokal has introduced class- E amplifier with parallel capacitor and obtained ideal power efficiency value as 100%.

II. RELATED WORK

Due to the demand of low power sensor nodes in wide range of applications, recent research has been focussed on every block of sensor nodes. I F Akyildiz et. al focuses on the importance of power conservation and power management in sensor networks [3]. Being low in cost, sensor nodes are deployed, in hundreds and thousands, for tasks ranging from battlefield surveillance to environmental sampling. It is important to save battery power on these micro-electronic device, due to the inaccessible regions where sensor networks are mostly deployed. In most of the applications, renewing power resources may not be possible. So life time of sensors greatly relies upon lifespan of battery. In [6], W Dargie focuses on selective switching and voltage scaling. To achieve low power and long life time, circuit-level design procedures are focused in [7]. Importance of low power

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transceiver design is explained in [8]. This paper focuses on the design parameters which significantly influence energy consumption of transceiver unit. D G Rahn et.al have designed a transceiver for multiple input/multiple output wireless LAN applications in [9]. In RF transceivers, the major power consumption unit is power amplifier. Class AB operation is suitable for improved linearity and higher power added efficiency. Adaptive biasing schemes can be implemented for low power applications. Low power amplifier with adaptive biasing is designed in reference [10].

High linearity, greater average output power, wider operating bandwidths and reduced energy consumption are the key design aspects for power amplifiers. When power amplifiers working in switch-mode configuration, the transistor operates in saturation, and either voltage or current, is switched on and off, depending on class of amplifier. A switch can be used in place of transistor. Only voltage is present across an open switch and current flows through the closed switch. So class E power amplifier has zero overlap of time between voltage and current. It gives 100% theoretical efficiency. Class-E power amplifier is a compromise between switched configuration and linear class AB configuration [11, 12]. Reference [13] presents a two stage class E linear power amplifier with greater power added efficiency.

In order to achieve higher degree of gain, the cascode amplifier configuration can be used. For collecting neural data from implanted electrodes, an RFID reader with high resolution is proposed in [4]. In reference [14], S. Du et.al described single ended power amplifier for WLAN applications. Higher gain and better efficiency can be achieved with current reused technique in driver stage and self-biased technique in power stage. Design of self-biased class E amplifier is given in [15].

III. PROBLEM FORMULATION

The efficiency and bandwidth are the most important characteristics of power amplifier in sensor nodes. Low power sensor nodes must communicate with their neighbours at hundreds of kilobytes per second and have to operate at higher volumetric densities. High data rate requires wider band width. But wider bandwidth limits the sensitivity and range. Requirement of wider bandwidth and higher efficiency without reducing sensitivity demands new design strategies.

Power amplifier with low power supply gives more reliable operation. But overall gain and efficiency are decreased due to reduced power supply.

In class E power amplifiers, these combinations do not exist. So we are proposing modifications for basic class E amplifier to achieve improved band width and efficiency at lower power supply.

IV. POWER AMPLIFIER

Power amplifiers are mainly responsible for power consumption in transceivers. So recent research focussed on power amplifiers in switch mode configuration [8,16]. The RF power amplifiers are classified as classes A-F depending on method of operation. An RF power amplifier uses an active device (BJTS, JFETS, MOSFETS, GaAs MESFETS etc.), dc feed and output matching network.

V. CLASS E POWER AMPLIFIER

The research in switch mode configuration of power amplifier aims to increase efficiency and band width without reducing linearity. Class E designs are commonly used due to greater power efficiency. An amplifier in class E design is shown in Fig 2 [17]. It is designed with transistor Q as switch, a shunt capacitor Cp, and a series LC circuit. The L_F is a radio frequency choke, which has high impedance at operating frequency. The values of Cp, L, C, L_F and R_L are selected such that power switching losses of transistor are minimized. The shunt capacitor absorbs the parasitic capacitance at the output of transistor. Presence of larger shunt capacitor for same power, load and supply, enables to operate at high frequencies. When transistor is off, current bypasses through the shunt capacitor. LC series resonator circuit allows current of fundamental frequency to flow from output to load. Finite dc inductance gives efficient output matching network. It also provides many other benefits like reduction in size, supply voltage and cost.

For Class E amplifier output waveforms are analog in shape compared with the ideal pulse shaped form of other modes of operation. So class E amplifiers can be supported by slow switching transistors and are better suited to high frequency operation. Class E power amplifier with shunt capacitor gives 100% ideal power efficiency [9].

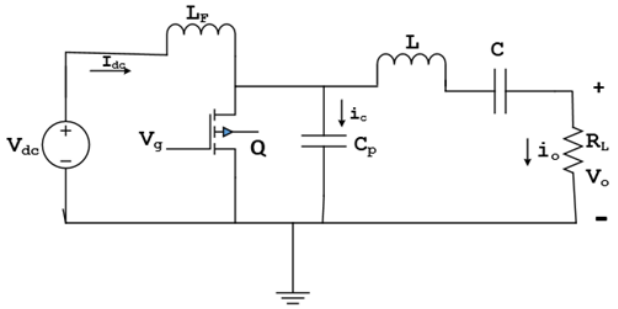

Fig 2. Class E power amplifier [19]

The design equations [14, 19-23] for class E power amplifier are as below:

The load resistance R_L is given by

$$R_L = \frac{8{V_{cc}}^2}{(\pi^2+4)P} \quad (1)$$

where V_{CC} and P represent dc supply voltage and power respectively.

The current drawn from dc supply (I_o) can be expressed as

$$I_0 = \frac{P}{V_{CC}} \quad (2)$$

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The shunt capacitance may be computed as:

$$C_P = \frac{I_0}{\omega R_L V_{CC}} = \frac{1}{\omega\pi\left\{\frac{\pi^2}{4}+1\right\}\frac{\pi}{2}} \quad (3)$$

The components L and C of series resonator are respectively given by (4) and (5).

$$L = \frac{QR_L}{\omega} \quad (4)$$

$$C = \frac{1}{\omega R_L\left\{Q-\frac{\pi(\pi^2-4)}{16}\right\}} \quad (5)$$

The radio frequency choke inductance may be computed as

$$L_{f(min)} = 2\left\{\frac{\pi^2}{4}+1\right\}\frac{R_L}{f} \quad (6)$$

Input power $P_{idc} = V_{cc} * I_{dc}$ (7)

Output power: $P_{oac} = I_{R_L(rms)}{}^2 * R_L$ (8)

Efficiency: $\eta = \frac{\text{Output power}}{\text{Input power}}$ (9)

VI. PROPOSED DESIGN

To make class E amplifier suitable for sensor nodes, two different configurations using basic class E amplifier are proposed in this work. The first configuration is class E amplifier with double cascoding and second design is class E amplifier designed using common drain followed by common source (CDCS) cascading. These configurations are discussed in the following subsections.

A. The Cascode Amplifier

A cascade of common source amplifier followed by common gate is termed as cascode amplifier. The basic idea behind cascode amplifier is to combine the high frequency response and current buffering properties of common gate configuration high input resistance and with large trans-conductance obtained in common source amplifier. Absence of Miller effect makes common gate high frequency response far superior to common source configuration [18].

The Cascode topology allows design of power amplifier at reduced V_G and V_{DS}, which leads to more reliable operation [19]. Higher output resistance and higher gain can be obtained by adding another level of cascoding. Here another transistor in common gate is added, and it results higher output resistance increased by a factor equal to voltage gain. Common gate configuration acts as current buffer. It takes input signal current at low input resistance and provides nearly equal current at very high output resistance. Presence of common gate configuration has resulted in increased load current thus increased efficiency and bandwidth [18].

B. Common Drain Common Source (CD-CS) Configuration.

Common drain common source cascading gives wider band width, compared with common source configuration. Transistor in common source configuration, will exhibit a Miller effect that results in large input capacitance. Buffering action of common drain configuration causes a low resistance across input capacitance of common source configuration.

Impedance match provided by the common drain configuration in CD-CS cascading results less loss across the load. It leads high load current and increases efficiency and bandwidth [18].

VII SIMULATION RESULTS

The performance of designed configurations is proved with PSPICE simulation. First, Class E amplifier with double cascoding as shown in Fig. 3(a) is simulated. Following design specifications are used for double cascode class E amplifier: Supply voltage = 12V, Output power = 10W, D = 0.5, Q= 10. For given specifications components values are computed as $R_L = 8.31\Omega$, $L_F = 57.6\ \mu H$, $L_S = 13.22\ \mu H$, $C_S = 2.17nF$. The R_D for CS configuration is considered as 30 Ω and R_S for CG configuration is 100 Ω. Power MOSFET IRF 510 is used for simulation purpose. Transient output of double cascode class E amplifier is as shown in Fig. 3(b). Load current measured is $I_{RL\ (RMS)} = 1.71$ Amp , with DC current $I_{DC} = 2.1$Amp. The efficiency for the observed values is computed as 96.43%.

Frequency response of double cascode class E amplifier is as shown in Fig. 3(c). Band width for this configuration is obtained as 284.4 KHz.

The CD-CS configuration is implemented as shown in Fig. 4(a). switching transistor IRF 510 is used for both CD and CS configuration. Supply voltage = 12V, 1MHz square pulse of amplitude 1V is applied as V_G. This configuration is also simulated for same design specifications as used for double cascoding amplifier. For given specifications components values are computed using design equations as $R_L = 8.31\Omega$, $L_F = 57.6\ \mu H$, $L_S = 13.22\ \mu H$, $C_S = 2.17nF$. The value of R_D for CS configuration is chosen to be 30 Ω and the R_S for CD configuration is considered to be 100 Ω.

Transient output of class E CD-CS configuration is shown in Fig. 4(b). The rms value of load current $I_{RL\ (RMS)}$ is obtained as 4.39 Amp and the dc current is observed to be I_{DC} 14.1 Amp. Hence, the efficiency is computed as 94.65%.

Frequency response of CDCS class E configuration is as shown in Fig. 4(c) and the band width obtained is 391 KHz.

The existing class E circuit shown in Fig. 5(a) is also simulated for same simulation settings to compare the performance of proposed designs. The transient output is showed in Fig. 5(b) where the peak switch voltage is obtained as 43.8V and current is observed as 1.65 Amps. From these simulated values the efficiency is computed as 91.67%.

It is thus observed that proposed designs outperform in terms of efficiency and bandwidth. The results are summarised in Table 1. It is found from the table that the proposed class E double cascoded configuration is suitable for wide band width and increased efficiency. The CD-CS Class E amplifier gives Maximum bandwidth.

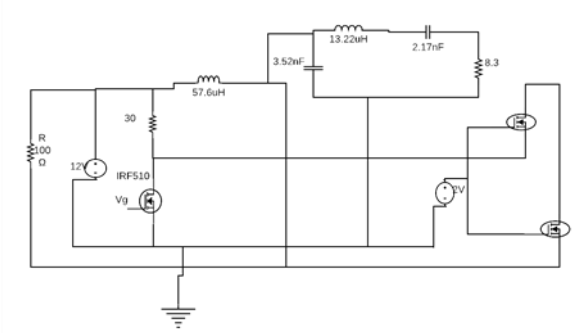

Fig 3(a): Class E amplifier with double cascoding.

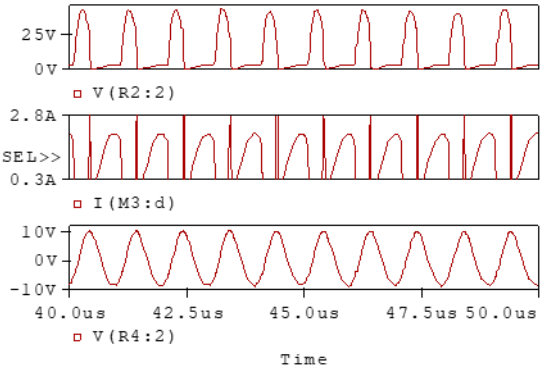

Fig 3(b): simulation results of class E amplifier with double cascoding.

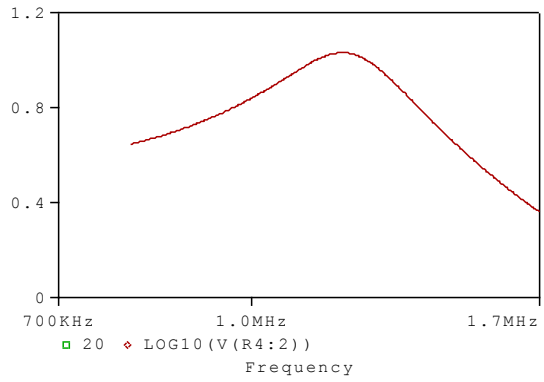

Fig 3(c): Frequency response of double cascode amplifier

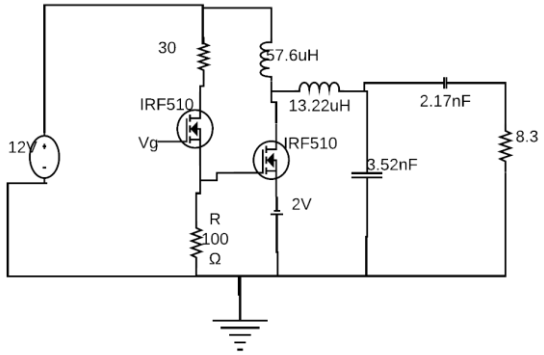

Fig 4(a): class E amplifier with CD-CS cascading

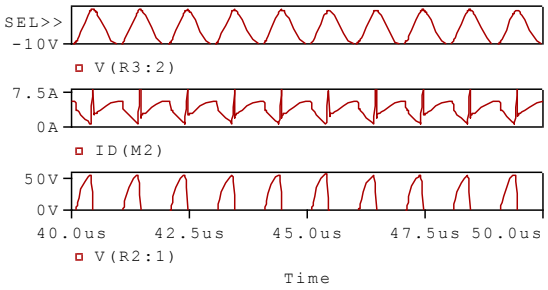

Fig. 4(b): simulation results of class E amplifier with CD-CS cascading.

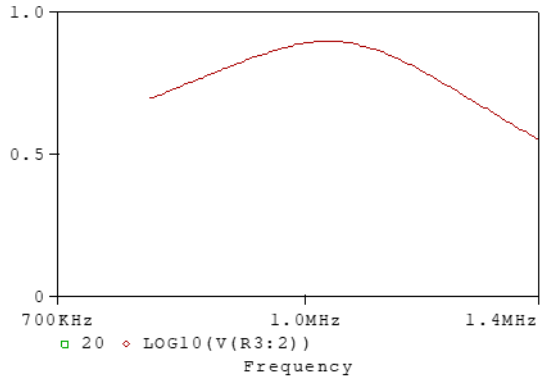

Fig 4(c): Frequency response of CD-CS cascading

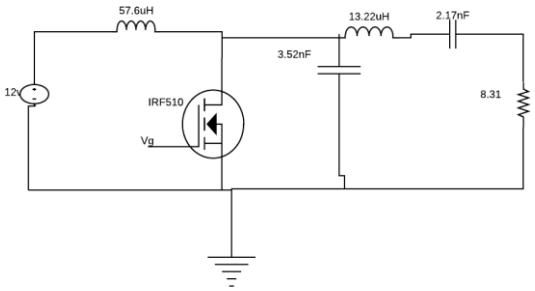

Fig 5(a): Simple class E amplifier circuit.

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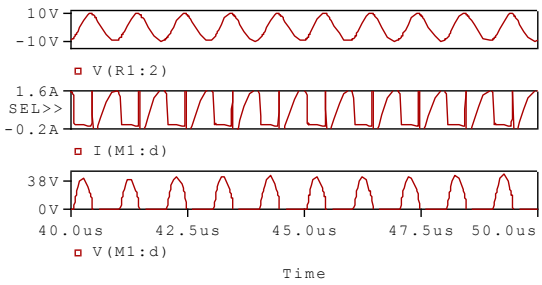

Fig. 5(b): Simulation results of simple class E amplifier circuit.

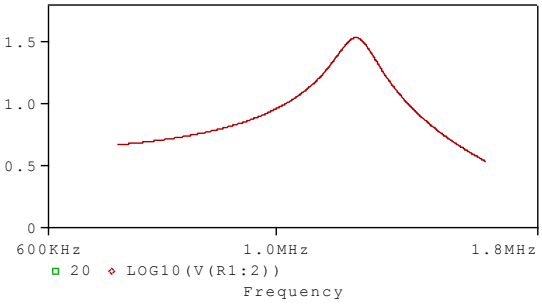

Fig 5(c): Frequency response of class E amplifier

TABLE 1.

PERFORMANCE COMPARISON TABLE

Circuit	DC Current (I_{DC})	RMS current (I_{RL})	Efficiency	Band Width
Simple Class E Amplifier	0.52A	0.83A	91.67%	97.3KHz
Proposed double Cascode Class E amplifier	2.1A	1.71A	96.43%	284.4KHz
Proposed CD-CS Class E amplifier	14.1A	4.39A	94.65%	391KHz

VII. CONCLUSION

Design of power amplifiers for sensor nodes requires extensive research to meet requirements for linearity, efficiency, output power, band width. Class E power amplifiers are designed and simulated with double cascoding and CD-CS cascading. Simulated results show better efficiency and band width as compared to existing class E amplifier.

Further low power and high accuracy can be achieved using optimal pulse bias. To reduce supply voltage and DC power consumption, Darlington configuration can be employed. To improve the efficiency, self-bias can be implemented in double cascoding and CD-CS configurations.

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