High efficient CMOS rectifier with reduced leakage for low powered bio-implantable devices

Damarla Paradhasaradhi, G.L.V.Sai Kumar Reddy, G.Manideep, Y.L.N.D.V.Amar Kumar

Abstract- ***To support the operation of supplying power to biomedical devices is a challenging task. Rectifiers guarantee the efficient voltage conversion and power conversion chains. This paper presents the comparison among different architectures of CMOS rectifiers to have a hold on the power supply problem of low-voltage biomedical implantable devices. The presented rectifier utilizes bootstrapped capacitors to decrease the effective threshold voltage and a CMOS inverter to reduce the reverse leakage. The designed architecture gives high Power Conversion Efficiency (PCE) at the expense of low dropout voltage. Accordingly, this proposed design is a decent option for low-voltage power supplies and large load current applications. The proposed rectifier is implemented in generic 0.25 µm CMOS technology. Simulated results show that the proposed rectifier has improved voltage and power conversion efficiency compared with the other CMOS rectifiers provided.***

Keywords- Bio-implantable devices, Bootstrapping capacitor, Differential drive, Reverse leakage, Threshold cancellation

I. INTRODUCTION

Providing power to biomedical devices, for example, pacemakers, forged hearts, useful electrical simulators, observing devices and retinal simulators for their long term action is a challenging task [1]. To help their task, it is important to give enough energy. It is a challenging task to make sure proficient power conversion chains capable of extracting required power from the limited available energy or power. Classical controlling methods include embedded batteries and power harvesting strategies [2,3]. These strategies are normally constrained regarding power density, device life time, integration, structural constraint, and potential dangers to human wellbeing. To overcome these constraints, late research focussed on the wireless systems covering short ranges [4,5]. Despite promising execution, these methods experience the ill effects of very low power transfer effectiveness because of poor coupling, skin ingestion, also, narrow band-pass. In this manner, it is important to utilize a resourceful rectification method to process the power got from the secondary winding of the coupling coil.

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The execution of a CMOS rectifier, Voltage Conversion Efficiency (VCE), and Power Conversion Efficiency (PCE) are inclined by the circuit topology, diode-device parameters, input RF signal frequency, amplitude and output stacking conditions. The VCE is the portion of the output DC voltage VOUT and the information peak voltage capability |VAC|, which can be given as:

$$VCE = \frac{V_{OUT}}{|VAC|} = \frac{V_{OUT}}{V_{OUT} + V_{d0}}. \quad (1)$$

Where V_{d0} is the entire dropout voltage along the rectifier conducting path. Further, PCE is defined as the ratio of the output power POUT and the input power PIN. In fact, the PCE of the rectifier is generally given as:

$$PCE = \frac{P_{OUT}}{|P_{IN}|} = \frac{V_{OUT}}{|VAC|} \times \frac{I_{OUT}}{I_{IN}}. \quad (2)$$

Where IOUT is the output DC current and IIN is the total input current of the rectifier. Different threshold and reverse cancellation strategies have been proposed as of late for MOS-based diodes to improve the overall performance. A Self-VTh- Cancellation (SVC) strategy has been proposed in [6,7]. In this technique, the threshold voltage of the MOSFETs is cancelled by applying an gate bias voltage produced from the output voltage of the rectifier itself. This strategy offers basic design at the expense of high reverse leakage. An improved addition of the SVC strategy is given in [8]. The cross-coupled differential CMOS architecture results in preferable PCE over the SVC approach [8]. However, it doesn't give the assured VCE. In [9], a CMOS inverter based dynamic rectifier design is presented. It gives the ideal VCE and PCE by decreasing both the reverse leakage and threshold voltage. Bootstrapped capacitor-based strategy is provided [10,11]. It decreases the effective threshold voltage of the main pass transistor, by increasing the VCE and PCE values.

The contents of the paper are organized as follows: Section 2 provides conventional rectifier topology. Section 3 describes the low power based rectifier topologies alongside by their functioning study. Section 4 presents simulation results of the projected devices, as well as a comparison among diverse designs. Finally, the conclusion is presented in Section 5.

II. CONVENTIONAL RECTIFIER TOPOLOGY

A conventional CMOS rectifier circuit Fig. 1, which

is composed of series connection of diode-connected NMOS and PMOS transistor is publicized below. The voltage input is applied through the coupling capacitor(C). During the positive half cycle of voltage signal, forward current flows to the output load. When the negative half cycle of the voltage signal is applied, almost no current flows. The majority of the power losses of the built-in rectifier circuit start from the ON-resistance of the transistor. The PCE of the rectifier circuit is inclined by circuit topology, diode parameters, and input voltage level. Small ON resistance and small reverse leakage current are the standard parameters of the MOS diode which can improve the PCE of the rectifier. Usually, small ON-resistance of the MOS-diode is realizable by small turn on voltage of the transistor that is the threshold voltage of the transistor, So as to reduce the losses in the rectifier circuit.

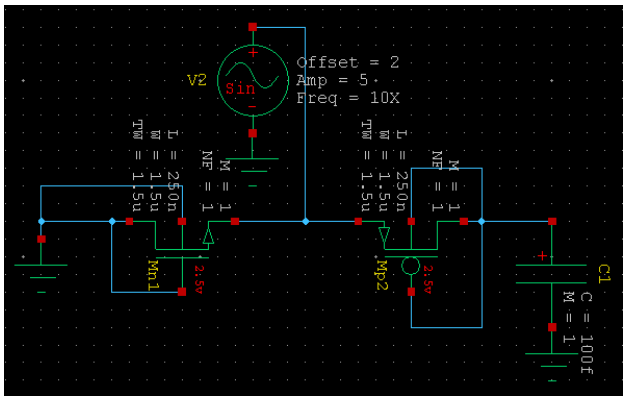

Fig. 1. Conventional rectifier configuration.

The voltage drop across a MOS diode is given as,

$$V_{d0} = V_{TH} + \sqrt{\frac{2LI}{C_{ox} W \mu}}. \qquad (3)$$

Where, L and W are the length and width of the transistor, I is the current flowing and *Cox* is process related product and *Vth* is the threshold voltage of the transistor. The voltage drop not only linked to the threshold voltage, but also depends on the excess voltage, which linearly increases with square root of the current. As the threshold voltage is the key parameter which can degrade the performance of the rectifier, suitable Vth-cancellation mechanism is applied.

III. LOW POWER BASED RECTIFIER TOPOLOGIES

The designed self-Vth-cancellation (SVC) CMOS rectifier circuit is appeared in Fig. 2. In self-Vth-cancellation rectifier, the gate of the PMOS and NMOS transistors are cross-connected with the end goal that the NMOS transistor and the transistors are connected to the ground terminal and output terminal respectively. This connection increases the gate-source voltage of the transistor which constantly decreases the threshold voltage.

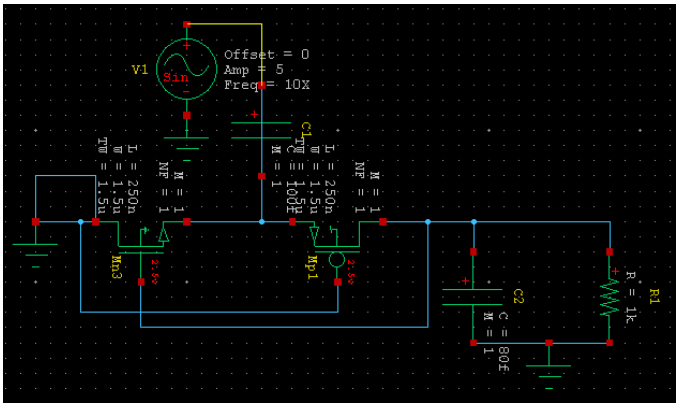

Fig. 2. Self-Vth-Cancellation (SVC) rectifier configuration

This configuration is basic and does not require any extra power circuitry. Gate-source voltages of the PMOS and NMOS transistors are statically one-sided utilizing the output DC voltage, in this manner decreasing the effective Vth of the MOS transistors, which result in broad PCE. In this design, the energy loss for the most part relies upon the on-resistance of the transistor. At the point when the threshold voltage is too small, it might cause reverse leakage current which will decrease the PCE. Consequently it is impractical to accomplish small on-resistance and small leakage current in self-Vth cancellation rectifier. Therefore, PCE of the SVC rectifier circuit will primarily increase with the increase in input power, yet then decrease with the additional increase in input power, exhibiting some peak value in the middle.

As per SVC configuration rectifier it is not possible to carry out small on-resistance furthermore, small leakage current at the same time. So as to deal with the issue differential drive

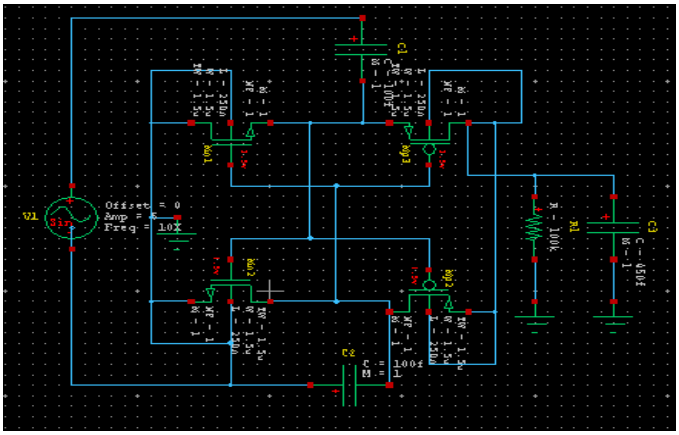

Fig. 3. Differential drive CMOS rectifier configuration

CMOS rectifier circuit is shown in Fig. 3. has been designed. It involve of a cross-coupled differential CMOS with a bridge structure. In this differential structure, the gate of the transistor is influenced by a differential flag.

This sort of rectifier performs superior to the MOS-diode based rectifier. It is likewise called four-transistor cell and called negative voltage converter. The structure comprises of blend of two cross-connected gate structure which give complimentary bridge rectifier. In the circuit, the

PMOS transistor delivers highest voltage to the load, while the NMOS-transistor gives the least voltage. To increase the output voltage, N cells of the structure can be cascaded. Differentials signal of the first stage is directly connected to the RF source whereas, the proceeding stages are capacitively coupled to the RF source .This structure behaves as a charge pump voltage multiplier, as the expected output voltage at the N'th stage is *Vout* but in practice the output voltage is lower because the *Vdrop* increases with the increase of the number of cells due to increase of the body bias of the transistor.

A full wave bridge rectifier converts over the two polarities of the input signal to a DC signal. The architecture requires four diodes as appeared in Fig. 4. Whereby, a couple of diodes oversee correction of each signal cycle. This structure profits by high power efficiency and smaller output ripple compared to half wave rectifier. However, threshold voltage drop of two diodes are lost in each signal cycle. The rectified output voltage is given by,

$$V_{out} = 2V_{in} - 2V_{th} \quad (4)$$

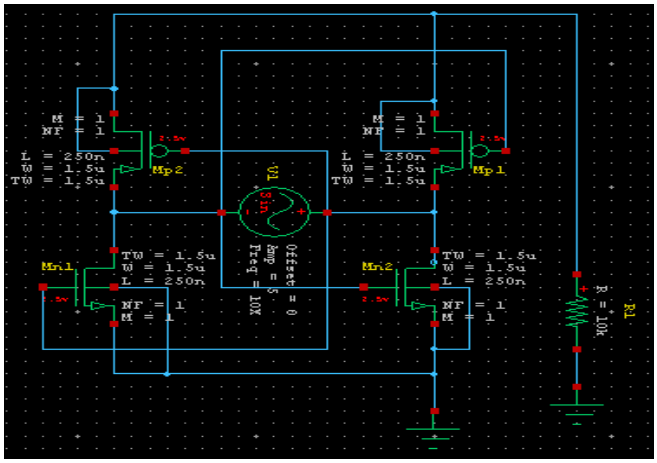

Fig. 4.CMOS bridge rectifier configuration

As the MOS transistor is the main part of the rectifier structure, it is worth to analyze the equivalent circuit of the MOS transistor the power consuming elements in the equivalent circuit are mainly substrate-drain diode, substrate source diode and channel resistor. So most of the power is consumed by the channel resistance which is the resistance between the source and the drain, to increase the power efficiency of the rectifier, the turn on voltage of the transistor should be small and the channel resistance also should be decreased. To obtain small channel resistance, larger transistor size is required which contribute to large CMOS diodes and parasitic capacitances which can introduce greater leakage current and parasitic losses.

So as to improve the VCE and PCE, we propose another design for a full-wave rectifier. It is executed by using a couple of pMOS switches that realize the threshold cancellation method to replace the diodes or diode-associated pMOS transistors utilized in a few previous attempts. The chose nMOS transistors profit by the advantages of the cross-coupled differential structure. Fig. 5 demonstrates the design of the proposed full-wave rectifier. This design minimizes the reverse leakage current and cancels the effective threshold by using the facilities of bootstrapping capacitor [11], Full Threshold Cancellation (FTC) [9], and differential drive CMOS rectifiers. Subsequently, this design offers high VCE and PCE at the load.

At the positive half cycle (VRF+) of the power source VAC, the inverter works by using M7, M8, M13, and M14 transistors. M13 is a DCT and M14 is associated in the differential-mode. The motivation behind the inverter is to turn off M3 totally at the negative half cycle (VRF-). Accordingly, this technique minimizes the reverse leakage brought by the main pass transistor M3. The reverse leakage through the main pass transistor of the proposed rectifier during the switching operation among VRF+ and VRF-is similarly lower than that got through different models. Thus, a higher PCE is accomplished by the proposed rectifier. During VRF+, the inverter assists the threshold cancellation operation. At VRF+, M8 is ON, charging C1 through the DCT M11. This initiates the in-circuit threshold cancellation for M3. Additionally, at VRF-, M7 is ON through the differential-mode transistor M14. Accordingly, the drain to gate voltage of M3 is zero, which reduces the reverse leakage through M3. M13 monitors the ON and OFF exchanging of the M7 and M8 transistors as appeared:

$$when, VRF + < VOUT, M7 = ON, M8 = OFF$$

$$VRF + > VOUT, M8 = ON, M7 = OFF$$

At VRF+, M8 is ON and the Capacitor Discharging MOS Transistors (CDT) M17 and M18 are OFF. In Fig. 4, the DCT M5 creates an auxiliary path to charge the output capacitor CL during the rising time of VRF+ until

$$VOUT = (VRF +) - VTh, M5. \quad (5)$$

As the output node is charged, the bootstrapping capacitor C1 charges as on form through the DCT M11 and the voltage across C1 rises in the direction of

$$VC1 = VOUT - VTh, M11 - VTh, M8. \quad (6)$$

From (5)

$$VC1 = (VRF +) - VTh, M5 - VTh, M11 - VTh, M8.$$

Since the threshold voltage of the same type of transistors are nominally the same for a particular process technology,

$$VC1 = (VRF +) - 2 \times VTh\,(PMOS) - VTh, M8. \quad (7)$$

Eqs. (8a) and (8b) define the source to gate voltage of M3 as follows

$$VSG, M3 = (VRF +) - VTh, M8 - VC1. \quad (8a)$$

$$VSG, M3 = VTh, M11 + VTh, M5. \quad (8b)$$

Since the voltage across V*SG*, *M*3 is twice threshold voltage, As a result, M3 will start to conduct and charge the output node. M3 remains in the cut off mode before the V*SG*, *M*3 reaches V*Th*, *M*3. Thus, by using (6a), we can write:

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$(VRF+) - VTh, M8 - VC1 \geq VTh, M3.$ (9)

Substituting VC1 from (5) into (8), we obtain:

$VTh, M3 = (VRF+) - VTh, M8 - VOUT + VTh, M11 + VTh, M8.$

$VOUT = (VRF+) - (VTh, M3 - VTh, M11).$ (10)

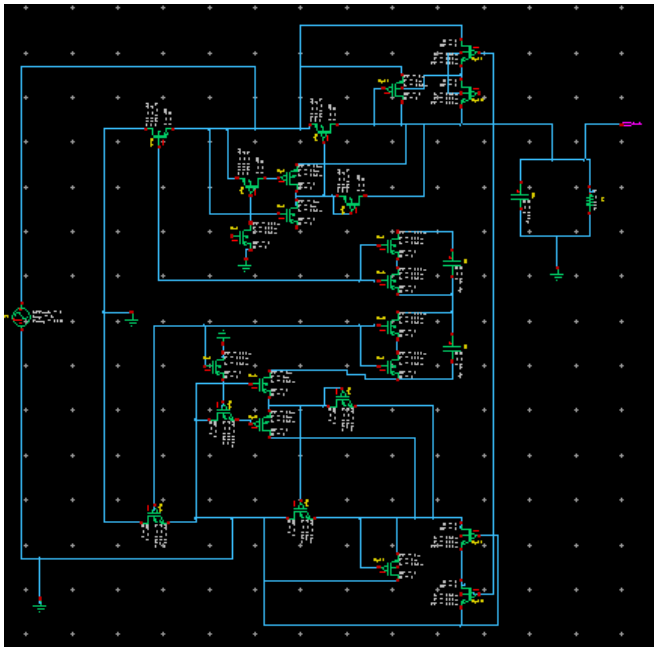

Fig. 5.proposed full wave rectifier configuration

Eq. (9) demonstrates that the effective threshold voltage of M3 is reduced. A low impedance return path is formed for the current charging CL by the nMOS transistor (M2), which is connected in the differential mode gate cross-coupled design. The gate of M2 is actively biased by a differential-mode signal.

At VRF+, the gate voltage of M2 is positively biased and effectively decreases the turn-on voltage of M2, bringing about a little ON-resistance. M5 contributes to the output current too, however, it is of little significance in the overall power enhancement on the because of its small size compared with that of the main pass transistor. The source of M5 is connected to the floating power supply and its voltage varies greatly overtime. In this way, the exposed terminal could inject leakage current in the substrate and induce latch up. A Dynamic Bulk Switch DBS is formed by utilizing M21 and M22 transistors. In a prolonged simulation, it is seen that, VC1 increments step by step, and this influences the VCE by decreasing VOUT. To keep VC1 constant, highly resistive CDTs are utilized to discharge C1 by a very small amount at VRF-. Accordingly, C1 keeps up a steady VC1 over time. At VRF-, the double circuit consisting of M1, M4, M6, M9, M10, M12, M15, M16, M23, M24 and C2 will rectify the input voltage in a parallel way.

IV. RESULTS AND DISCUSSION

The average output voltage, VCE, and PCE are common execution measurements to compare different rectifier circuits. The proposed rectifier is implemented at the schematic of generic 0.25 µm CMOS process and simulated with the tanner tools. A shunt load of CL=20 pF and RL=10 kω is considered. The size of main pass pMOS transistors M3 and M4 are 45/0.18 µm, and the main pass nMOS transistors M1 and M2 are 40/0.18 µm. Auxiliary path transistors M5 and M6 are associated as a DCT with a size of 1/0.18 µm, while another arrangement of DCT, M11 and M12, are actualized utilizing 15/0.18 µm measure transistors. The nMOS transistors M8 and M10 of the inverter comprises of 5/0.18 µm size transistors while the pMOS transistors M7 and M9 are three times bigger than the nMOS transistors. Small size (0.4/0.18 µm) transistors (M13, M14, M15, M16) are used to monitor the proper switching operation of the inverter. The CDTs (M17, M18, M19, M20) are actualized using small size (0.4/0.18 µm) transistors. Small size pMOS transistors (0.4/0.18 µm) are used for DBS structures. The selected capacitance of the bootstrapping capacitors C1 and C2 is 35.6 pF.

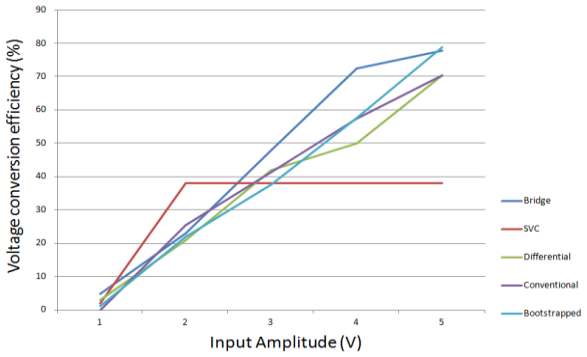

Fig. 6. Voltage Conversion Efficiency versus input peak amplitude.

To verify the performance of the proposed full-wave rectifier, we compare the simulation results of the SVC, differential drive, CMOS bridge rectifier and bootstrapping capacitor based rectifiers. The schematics of the past designs are actualized utilizing their sizes gave in [7,8,11].

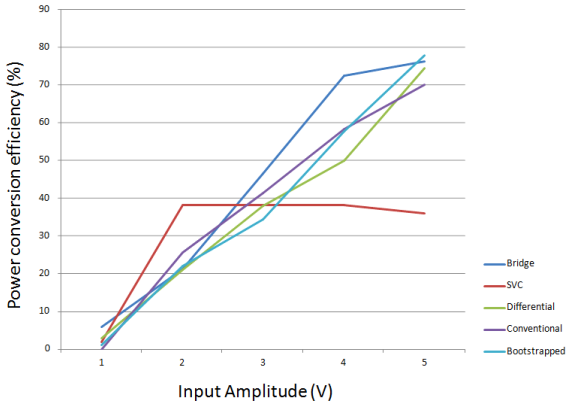

Fig. 7. Power Conversion Efficiency versus input peak amplitude.

Fig. 6.shows the simulation results comprising the VCE variation versus the peak input amplitudes for different architectures. The projected architecture presents extensively higher VCE over a wide range of input peak amplitudes. Fig. 7.shows the simulation results comprising the PCE variation versus the peak input amplitudes for different designs.

Table 4 Performance of various rectifiers

	Conventional	Bridge	SVC	Differential	Boot strapped
Process (µm)	0.25	0.25	0.25	0.25	0.25
No. of transistors	2	4	2	4	24
Input Amp.(v)	5	5	5	5	4
Load Cap.(pf)	0.1	-	0.1	0.45	20
V out (V)	2.12	3.9	1.15	2.12	3.17
Load Res. (ohm)	1k	10k	1k	100k	10k
Power (pw)	0.025	0.025	0.97	0.025	0.0025
Max VCE (%)	70.6	78	38.3	70.6	79
Max PCE (%)	70.2	76.3	36	74.6	78

However, among the designs utilizing standard CMOS forms with the given component size, the result of the comparison affirms that the proposed rectifier topology offers the advantages of high performance in a small area. The proposed rectifier topology performs agreeably working at low source voltages. Table 4 lists the performance of various rectifiers.

V. CONCLUSION

This paper presents a full-wave rectifier suitable for different applications, including RFID tags and wireless biomedical implantable systems. The architecture of the proposed rectifier offers a small area, which is the major design constraints to be followed in the modern-day integrated circuits. The new proposed design includes differential-mode gate cross-coupled nMOS switches along with pMOS switches are implemented with minimized reverse leakage and reduced effective threshold voltage technique to achieve efficient AC to DC conversion. The schematic simulations confirm reportedly higher voltage and power conversion efficiency compared with the previously worked rectifier architectures.

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