Analysis of Inverter using Single Electron Transistor

NitinBansal, Brijendra Mishra, Pankaj Kumar Mishra, Vivek Singh Kushwah, Sanjay Jain, Rishi Sharma

Abstract:This paper presents an analytical model Inverter based on the theory of single electron transistor(SET).The proposed design is very flexible such that it can be used for single gate, multi-gate, symmetric, asymmetric devices and most importantly it can also consider the effect of background charge. It can also be used for large voltage range of drain-source voltage irrespective of the bias conditions. The proposed design has been simulated with SPICE and the characteristics produced by the proposed design have been verified against Monte Carlo simulator SIMON.

Index Terms:Coulomb Blockade,Monte Carlo Simulator SIMON, Single-Electron Transistor

I. INTRODUCTION

The present Electronics industry is based on conventional MOSFET transistor which is a three terminal device. There are so many uses of transistors in electronics industry but the first and most important application of MOSFET transistor is a switch, which is used in almost all electronics devices. Moore's Law states that as the years gone the no of transistors increasing manifold and now the days has come that conventional MOSFET industry is now looking to think substitute because of the problems associated with it is increasing continuously especially leakage current which consumes the battery and nowadays all the portable devices are dependent on battery. To meet out these challenges Single Electron transistor comes out strongly as an alternative because of its fast operating speed and low power consumption[1].The process was started in 1968 when the process of quantization is experimented and observed in tunnel junctions. But it was in 1987 when Fulton and Dolan made the first metal based SET. Theymade astructure by connecting two metal leads by tunnel junctions and on the top of the structure they placed an insulator and a gate electrode is placed underneath. In 1989 the first semiconductor SET was fabricated by Scott-Thomas [2]. Since then a number of SETs has been made with different combinations of materials. Today most of the research is focused on the Coulomb blockade region because it is region which is responsible for conductivity in single electron transistor. In this paper, an analytical model for SET Inverter has been proposed. The model is based on the phenomena of single electron tunneling. It is applicable for single gate, multi-gate, symmetric and asymmetric devices. SET Inverter circuit is simulated under different biasing conditions, and for different range of temperatures. The results are compared with those obtained by Monte Carlo simulator SIMON over a wide range of drain to source voltage.

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NitinBansal, Amity School of Engineering and Technology Amity University Madhya Pradesh, Maharajpura Dang, Gwalior (MP)-474005
Brijendra Mishra, Amity School of Engineering and Technology Amity University Madhya Pradesh, Maharajpura Dang, Gwalior (MP)-474005
Pankaj Kumar Mishra, Amity School of Engineering and Technology Amity University Madhya Pradesh, Maharajpura Dang, Gwalior (MP)-474005
Vivek Singh Kushwah, Amity School of Engineering and Technology Amity University Madhya Pradesh, Maharajpura Dang, Gwalior (MP)-474005
Sanjay Jain, Hindustan College of Science & Technology,Farah, Mathura, India
Rishi Sharma, MEMS and Microsensor Group, CEERI, Pilani, Rajasthan, India

II. SINGLE ELECTRON : A CONCEPT

The concept of single electron transistor is based on transfer of only one electron through an island at a time and hence utilizing the coulomb blockade effect[3]. It is also a three terminal device named as drain, source and gate. The drain and source are connected through tunnel junctions with a low self-capacitance common electrode known as island. The electrical potential of the island can be controlled by the gate electrode as shown in the Fig.1. The electron travels from drain to source electrode one by one through an island which is controlled by gate electrode

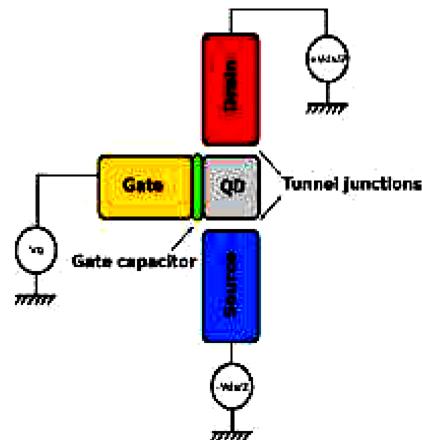

Figure 1: Schematic of SET

In the blocking state no flow of electrons takes place from source region to drainregion due to tunneling phenomena and coulomb blockage effect. When a positive gate voltage is applied then the transfer of electron from source to island takes place due to lowering of island energy. After that it travels towards drain electrode and then finally swept by electric field applied

at drain terminal. Thus the conduction of electrons from source to drain results in the charging of the nearby quantum dot[4]. Due to the charging there is an increase in the electrostatic energy of the quantum dot which is given by

$E_C = \frac{e^2}{2c}$ (1)

Where C denotes the effective capacitance of the Quantum Dot, and it is given by

$C = \frac{e^2}{\Delta E}$ (2)

andEc is known as coulomb blockade energy. Here ΔE is the separation of the energy levels in the island. Generally the capacitance of the island is small and its value must be < 10^{-17} According to equation (1) there is an increase in the E_C (coulomb energy) and Increased Coulomb blockade energy is the energy of the electron already available in the conducting channel to another electron coming towards the channel. Thus coulomb blockade energy is responsible for flow of electron one by one through island and the phenomenon is called “Coulomb Blockade”.

The Coulomb Blockade can be achieved if these criteria would meet:

1. Relationship in the bias voltage, the electronic charge and the capacitance of the channel must fulfill the following criteria:
   $V_{bias} < \frac{e}{C}$
2. The Coulomb energy E_C must be greater than the thermal energy K_BT i.e. $K_BT < Ec$ otherwise the electrons will pass the quantum dot simultaneously.

From ‘Heisenberg’s uncertainty principle’ i.e. $R_T > h/2\pi e^2$,the Tunneling resistance should be greater than $h/2\pi e^2$.

The flow of electrons in SET environment is basically due to the difference of the two Fermi level functions in contacts. The work of one is to keep filling up the level(s) while the work of other is to empty them, and as a result of this process there is a net flow of currentfrom drain to source [3]. Here, all the levels do not conduct, only some levels support the flow of electrons. The process can be seen through Fig. 2.

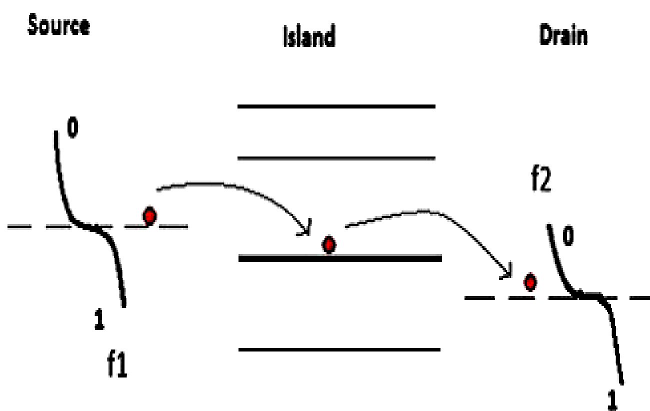

Figure 2: Tunneling of Electrons through fermi levels

The maximum conductance of SET is also called as the Quantum of conductance, $G_{max} = \frac{2q^2}{h}$. Correspondingly, the minimum resistance value is $R_{min} = \frac{h}{2q^2}$. The expression for the flow of current in the single-electron transistor can be given by

$I = \frac{q}{h}\frac{\gamma_1\gamma_2}{\gamma_1+\gamma_2}(f_1-f_2)$ (3)

Here $\gamma_1$and γ_2 are the parameters which is responsible for escaping of electrons from source and island respectively.

III. I-V CHARACTERISTICS OF SET

I-V characteristic of SET is drawn under the assumption of symmetric junction is shown in Figure 3 when capacitance $C_1=C_2$ and $R_1= R_2$. C_1 and R_1 are the source capacitance and island tunnel junction resistance respectively. Similarly C_2 and R_2 are the channel e and resistance of drain tunnel junction respectively[6-8]. From the figure it is clearly shows that current is zero till the voltage reaches$\frac{e}{C_\Sigma}$. The region where current is zero is called coulomb blockade region[5]. When bias voltage is applied greater than the threshold voltage i.e. $\frac{e}{C_\Sigma}$ then coulomb blockade effect is removed and current will flow.

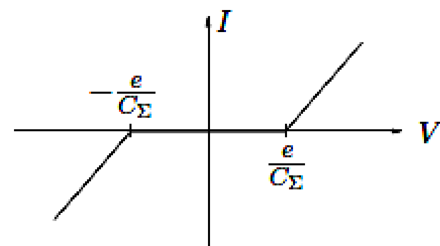

Figure 3: I-V Characteristic of SET

Figure 4 show the I-V characteristic for an asymmetric junction i.e. $R_1 \ll R_2$

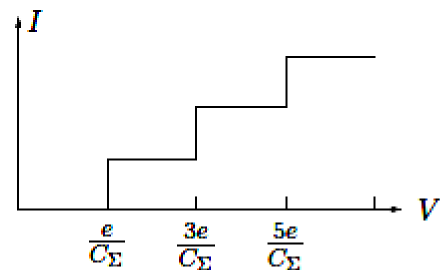

Figure 4 : I-V Characteristic for an Asymmetric Junction

In this case electrons move from one junction to another junction very rapidly which in turn increase the total charge of the island [9-11]. As a result there is a more electrons will present in the island and a current will raise in a staircase manner as the no of electrons increases in the island.

IV. PROPOSED DESIGN

The proposed model has been simulated in SPICE in order to simulate the SET circuits with other devices.

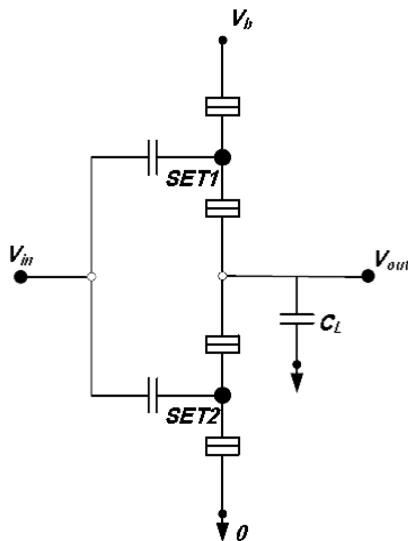

Figure 5: Schematic diagram of single electron inverter

Figure 5 shows a circuit diagram of an inverter circuit constructed with the help of Single Electron Transistors. It consists of two SETs with a common input gate terminal. To be more specific it can be seen as placing two single electron transistors in series with a common input gate terminal. The output capacitance $C_L$should be very highotherwise it would not be able to reduce the effect of the single-electron tunneling on the output node terminal.

V. RESULTS AND DISCUSSION

Figure 6is showing the input-output characteristics of the proposed inverter which is compared with SIMON simulator. Theresults of the SPICE simulator arenearly same as that of the SIMON.

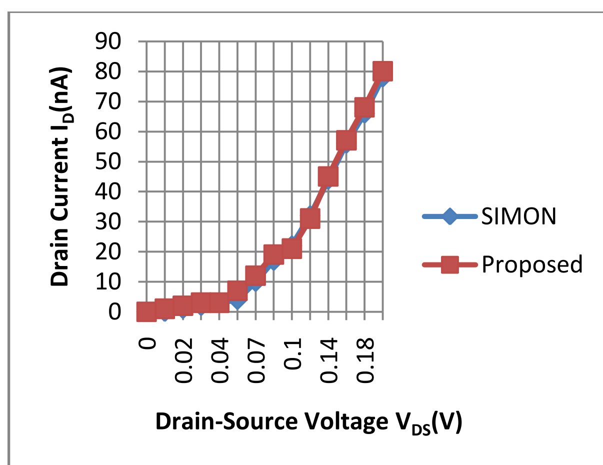

Figure 6 : Input –Output Characteristics

Also, the proposed design is capable of simulating the inverter under variety of different operating temperatures which is shown in figure 7. From input-output characteristics of the inverter, it can be clearly observed that the rate of change of output voltage is faster than the input voltage. At High temperature the voltage gain of the inverter decreases. It can also be seen from the simulation results that the high voltage gain at room temperature is not possible

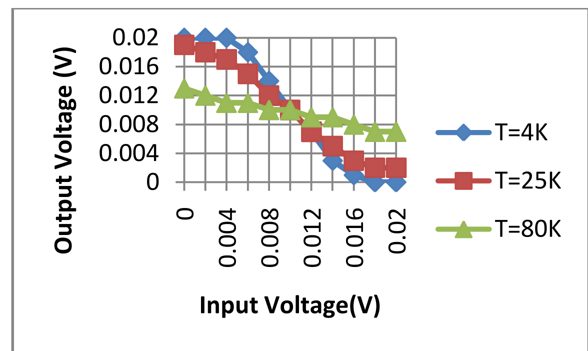

Figure 7: Input -Output Voltage Characteristics at different temperatures.

VI. CONCLUSION

The SET Inverter design has been verified against the Monte Carlo simulator SIMON The Inverteris so designed that it can also be manipulated for multi-gate SET. It takes the effect of background charge into consideration which is the most important source of leakage current. The Inverter is implemented in the circuit simulator SPICE its input-output characteristics showsa encouraging results.

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