A Novel Low-Power 5th order Analog to Digital Converter for Biomedical Applications

Aditya M, I Veeraraghava Rao, B. Balaji, John Philip B, Ajay Nagendra N, S Vamsee Krishna

Abstract: ***This paper implements sigma delta analog to digital converters that play a key role in ECG acquisition. In this paper we have implemented both fifth and sixth order sigma delta analog to digital converters and compared the parameters like SNR, Nodal spectrum analysis, Integrated power analysis with respect to same frequency given to both fifth and sixth order circuits. In this paper we observed the increase in power consumption as the order increases. For 5th order Sigma Delta ADC, we observed SNR of 74.8532 dB. Similarly for 6th order ADC the SNR observed was 75.5813 dB.***

Keywords: Sigma-Delta, ADC, ECG, SNR, acquisition

I. INTRODUCTION

In electronics, an analog-to-digital converter (ADC, A/D, or A-to-D) is a system that convert an analog signal, such as a sound selected by a microphone or light inflowing a digital camera, into a digital signal. An ADC may also offer an isolated measurement such as an electronic device that converts an input analog voltage or current to a digital number demonstrating the magnitude of the voltage or current. Typically the digital output is a two's complement binary number that is proportional to the input, but there are other possibilities.

There are several ADC architectures. Due to the complexity and the need for precisely matched components, all but the most specialized ADCs are implemented as integrated circuits (ICs). A digital-to-analog converter (DAC) performs the reverse function; it converts a digital signal into an analog signal [1]. There are different types of ADCs. Like Flash ADC, Sigma-delta ADC, Dual slope converter, Successive approximation converter.

Sigma-Delta ADC: Sigma-delta adjustment is a technique for encoding simple signals into computerized motions as found in a simple to-advanced converter (ADC).

In an ordinary ADC, a simple flag is examined with an inspecting recurrence and in this manner quantized in a staggered quantizer into an advanced flag. Sigma Delta ADCs are exceptionally impervious to simple circuit flaws and consequently considered as a financially savvy elective for high goals converters. Delta Sigma Analog to Digital Converters execute oversampling and quantization clamor forming. The high goals of late sigma-delta simple to computerized converters (ADCs) have made conceivable the immediate procurement of a scope of bio potential signals. Customarily 12 lead electrocardiogram (EGG) obtaining frameworks have been perplexing and equipment concentrated. Sigma-delta ADCs can possibly decrease the measure of equipment by about 60% [2], in this way lessening framework cost, volume and power utilization. The simple DS converter is a 1-bit testing framework. A simple flag connected to the contribution of the converter needs to be moderately moderate so the converter can test it various times, a system known as oversampling. The testing rate is many occasions quicker than the computerized outcomes at the yield ports [3]. Every individual example is collected after some time and arrived at the midpoint of with the other information flag tests through the advanced/destruction filter.

The Delta Sigma modulator is the core of the Delta Sigma Analog to digital Convertor. It is capable for digitizing the simple information flag and lessening clamor at lower frequencies. In this stage, the engineering executes a capacity called clamor molding that pushes low frequency clamor up to higher frequencies where it is outside the band of intrigue [4]. Clamor molding is one reason that Delta Sigma converters are appropriate for low-recurrence, high accuracy estimations. The information flag to the Delta Sigma modulator is a period differing simple voltage. With the prior Delta Sigma Analog to digital converters, this information voltage flag was principally for sound applications where AC signals were imperative [5]. Since consideration has swung to exactness applications, transformation rates incorporate DC signals. In a Delta sigma converter, the simple information voltage flag is associated with the contribution of an integrator, delivering a voltage rate-of-progress, or incline, at the yield relating to input greatness [6]. This inclining voltage is then looked at against ground potential (0 volts) by a comparator.

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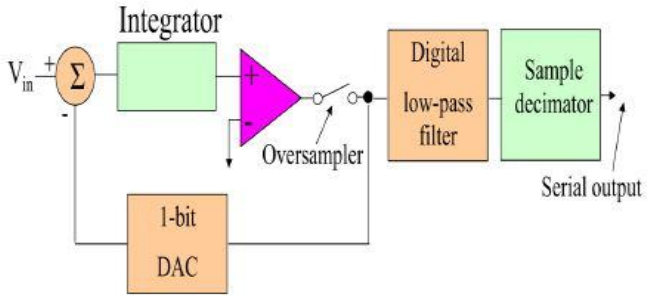

Fig.1 Basic block diagram of Sigma Delta ADC

Sigma-delta ADC Architecture is having an integrator and a comparator and 1-bit digital to analog convertor placed in a negative feedback loop. An integrator circuit is encouraged the entirety of the info flag and the refuted yield of the DAC. Sigma-delta ADCs execute oversampling, demolition sifting, and quantization clamor forming to accomplish high goals and fantastic antialiasing separating. Numerous SC Express, DSA, and C Series sensor estimation gadgets from National Instruments exploit 24-bit sigma-delta [7] ADCs for superior estimations. Sigma-delta ADCs execute oversampling, devastation sifting, and quantization clamor molding to accomplish high goals and superb antialiasing separating. Numerous SC Express, DSA, and C Series sensor estimation gadgets from National Instruments exploit 24-bit sigma-delta ADCs for superior estimations.

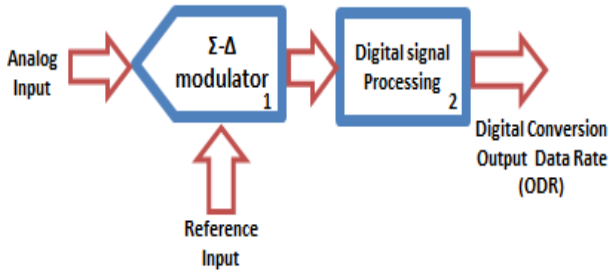

Fig. 2 Architecture of Sigma Delta ADC

Working of Sigma-Delta ADC: Typically there are two blocks: the Σ-Δ modulator and the digital signal processing block, usually a digital filter. This high level block diagram and the key concepts of the Σ-Δ ADC.

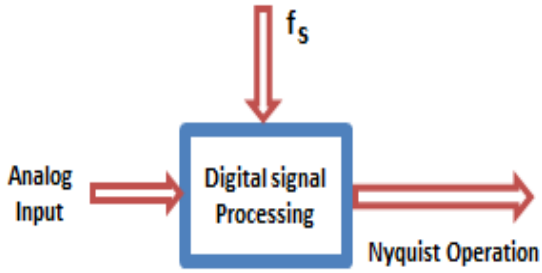

Fig. 3 Nyquist Comparision

As the Σ- Δ modulator is an oversampled architecture, let's start with the sampling theory and the scenario of Nyquist and oversampled ADC operation. Fig 3 illustrates the comparison between the Nyquist operations of an ADC with the oversampled case and finally with the Σ- Δ modulated (also oversampled) case.

II SIGMA DELTA ADC'S IN ECG

ECG flag is a critical reference for finding of coronary illness, and its obtaining straightforwardly influences the precision of the patient's disease conclusion and ensuing treatment impacts. 12-lead synchronous ECG information procurement framework dependent on ADS1298 incorporates the obtaining module and the remote transmitter module. The previous is in charge of the ECG information procurement and pressure, while the last is for the remote transmission of ECG information. M051 is a superior and low value MCU, embedded with the Coterx-M0 center. In this framework, M051 is utilized to control the obtaining, precession and transmission of ECG information. The center piece of the ECG flag obtaining module is ADS1298 [8]. ADS1298 is a most recent 16-channel 24-bit Analog to Digital Converter (ADC) made in TI Company, which has the characters of high-precision, low power and low commotion, with the incorporated info multiplexers, simple low-pass channel, and computerized channel.

III METHODOLOGY

5th Order ADC Architecture

A typical delta-sigma ADC for wireless applications has been used to demonstrate the decimation filter design flow. The CT Delta-sigma modulator was designed to satisfy the specifications of the next-generation wireless applications by incorporating a 5th-order loop-filter and a 1-bit quantizer [9]. Fig 4 shows the block diagram of the modulator employing a 5thorder, feed-forward, continuous time loop-filter.

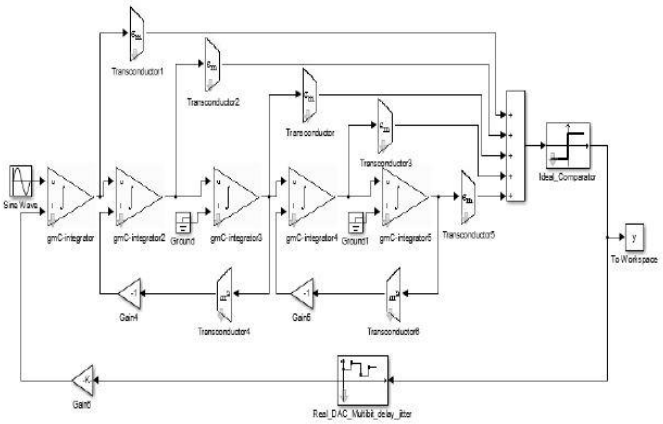

Fig. 4 Fifth order Sigma Delta ADC

The block diagram given in the Fig 4 shows an Σ-Δ ADC of order 5.The simulation is carried out using Simsides/Simulink . The output of sine wave generator is led to a five level circuit comprising of an integrator and gain to a summer [10]. The output from the summer is led to a single bit quantizer. A

digital to analogue convertor is provided in order to convert the digital output from the comparator in to analogue form which is fed back to the integrator. Node spectrum analysis: The Fig 5 shows node spectrum analysis of above Simulink model for signal bandwidth of 1.5625 MHz, M=40 and sampling frequency of 500 MHz

6th Order ADC Architecture:

By analyzing the results of 5th order ADC, higher order (6th) ADC is proposed to overcome the limitations of 5th order ADC. The block diagram given in the Fig. 5 shows an Σ-Δ ADC of order 6.The simulation is carried out using Simsides/Simulink The output of sine wave generator is led to a six level circuit comprising of an integrator and gain to a summer. The output from the summer is led to a single bit quantizer [7]. A digital to analogue convertor is provided in order to convert the digital output from the comparator in to analogue form which is fed back to the integrator.

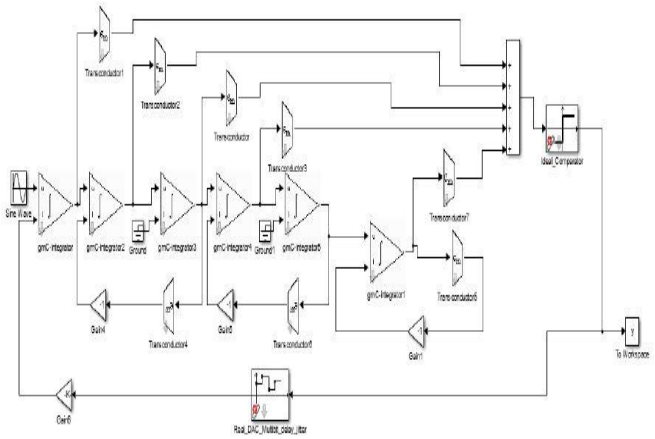

Fig.5 Simulink model for 6th order ADC

IV RESULTS

The below results are obtained from 5th order ADC using MATLAB SIMULINK in SIMSIDES.

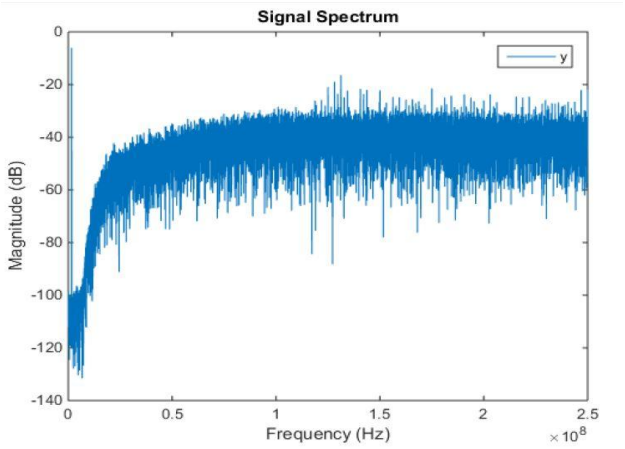

Fig. 6 Node spectrum analysis of Fifth order Analysis

Fig 7 shows integrated power noise with signal spectrum and harmonics in noise power. We have compared the following parameters like SNR i.e.,(Signal to noise ratio), NODAL SPECTRUM ANALYSIS and INTEGRATED POWER NOISE with respect to both fifth and sixth order sigma delta ADC's. Here we have given the same frequency to both the circuits and the observed difference in the above parameters as shown in the experimental results. As compared to 5th order there will be increase in SNR in 6th order.

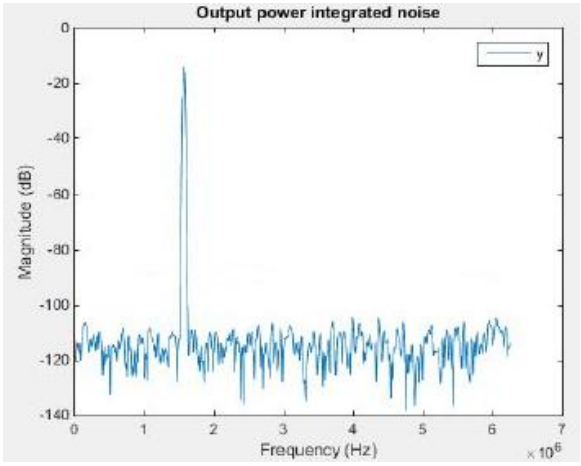

Fig.7 Integrated power noise spectrum of 5th order ADC

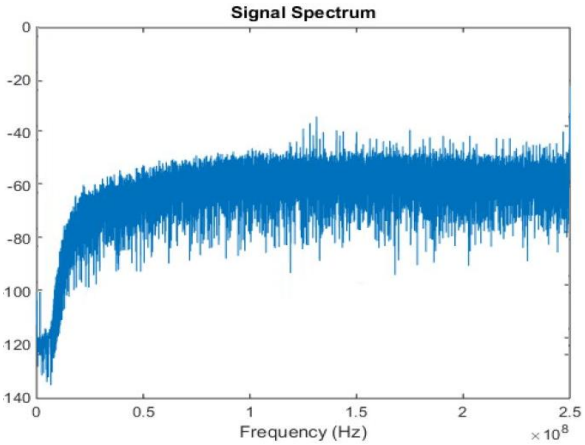

Fig. 8 Node spectrum analysis of Sixth order Analysis

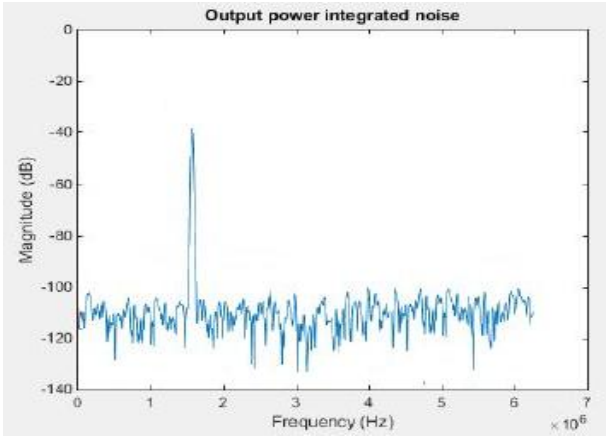

Fig.9 Integrated power noise spectrum of 6th order ADC

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V CONCLUSION

We presented the design and simulation of a fifth order and sixth order Delta-Sigma modulator using SIMSIDES/SIMULINK. The measured SNR for Fifth order sigma delta ADC at 1.5625 MHz signal bandwidth is 74.8532 dB and Effective Number of Bits is 12.1421 bits. The measured SNR for Sixth order sigma delta ADC at 1.5625 MHz signal bandwidth is 75.5813 dB and Effective Number of Bits is 12.2482 bits. We have compared the both circuits and observed that there will be increase in SNR and power consumption while order increases.

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