Efficient 1024-Point Low Power Radix-2^2 FFT Processor with MFFMD

Sai Kumar Kayam, K.Raghava Rao, Srinivasakumar Ch, Gurram narender, A Sreenivasa rao, Sk Hasane Ahammad

Abstract*: *The presence of radix-2^2 be an achievement in the structure of pipe-lined F/F/T equipment models. Afterward, radix/2^2 was stretched out headed for radix-2^k. In any case, radix/-2^k was anticipated in favour of solitary way defer input (S/D/F) structures, yet not in support of feed/forward ones which is likewise as described multi-way postpone commutator/(M/D/C). This manuscript displays the radix-2^k feed forward (M/D/C)-F/F/T designs. In feed forward models, radix-2^k container be utilized on behalf of any figure of equivalent examples which is an intensity of two. Moreover, mutually obliteration in recurrence (D/I/F) along with pulverization in occasion (D/I/T) disintegrations preserve be utilized. What's more, the structures can accomplish elevated throughputs, which create them appropriate for the mainly requesting submissions. Without a doubt, the projected radix-2^k/feed/forward designs necessitate less equipment assets than corresponding input ones, additionally named multi-way defer criticism (M-D-F), whilst a few examples in similar should be prepared. Subsequently, the planned radix-2^k feed forward models not just suggest an alluring answer in favour of flow requests, yet additionally open up another exploration line on feed forward structures.

Index Terms*: (*MFFMD) Modified Feed-Forward Multiple Delay, Low Power, Radix-2^2 FFT Processor

I. INTRODUCTION

In the current innovations, while the through-put compulsory is in the request of giga tests every moment, there emerges a requirement on behalf of pipe/lining, parallelism also proficient F/F/T models. Pipe-lined structures were generally utilized so as to accomplish towering throughput as well as small idleness alongside little region also low authority utilization. Pipelined design is of 2 kinds. They are criticism design along with feed familiar engineering. Input models be portrayed beside their criticism circles. In criticism engineering, a few yields of butterflies resolve be bolstered reverse as contributions to a similar butterfly. Criticism engineering is of II sorts. They are solitary way defer input engineering and multi way postpone criticism design. Single way postpone input engineering forms ceaseless stream of one example for every clock cycle though multi way defer criticism design or parallel criticism design forms a few examples in equivalent. Feed/forward design, likewise described as multi-way/defer/commutator-(M/D/C) do not contains criticism circles.

Revised Manuscript Received on May 07, 2019.

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It forms information moreover sends them to progressive phases. It can progression a few examples in similar. At there, continuously requests, high throughput arranged by giga tests every second is required in applications, for example, ultra wide band (UWB) and
Orthogonal recurrence division/multiplexing-(O/F/D/M). Progressively applications, there are 2 fundamental difficulties. Initial one is to compute the quick
Fourier/transform-(F/F/T) of various information successions received one subsequent to other. 2nd test is to compute the quick Fourier change (F/F/T) when a few examples of a similar grouping are gotten in equivalent. The second test approaches keen on image when the necessary throughput is superior to the clock recurrence. Together the difficulties are viably met beside the feed-forward F-F-T engineering through short zone. . Radix-2^k feed-forward engineering container obtain every number of parallel examples to the intensity of 2.The projected engineering is progressively effective as far as equipment and execution than parallel criticism structures. Henceforth, it develops as an alluring answer in support of the most requesting applications.

II. FEEDFORWARD FFT ARCHITECTURE

2.1 RADIX-2^2FFT ALGORITHM

N_point discrete fourier change of info grouping “x(n)”_is characterized as Where, the quantity of components N in information arrangement is an intensity of II. Cooley tukey calculation on separate Fourier change, additionally described as Fast/fourier change lessens the quantity of activities starting O (N^2) in isolated Fourier change to O/(N*log N(base2)) in quick fourier change.

$$X[k] = \sum_{n=0}^{N-1} x[n] W_N^{nk}, \quad k = 0, 1, \ldots, N-1$$

$$W_N^{nk} = e^{-j(2\pi/N)nk}$$

Cooley tu_key calculation comprises of n= log(N)/base(p) phases wher”e ‘p’ is stand of radix_r of F/F/T. Radix-2^2-F/F/T calculation exploits by separating the points at odd periods hooked on inconsequential ground non insignificant revolution ω‟ also transitory the non-minor pivot to the accompanying smooth phase. At odd phases, the separating of edge pursues the accompanying calculation. If(Ø>N/4) at that point Ø(stage) = N/4 elseØ(stage) = 0 end if The non-unimportant pivot Ø‟ which motivation be left as well as summed behind among turn of the progressive period is specified by Ø‟ = Ø mod N/4. In this way at even stages, the revolution point spirit be Ø (stage) = Ø (stage) + Ø‟ Simplification is communicated in condition organization as

$$Ae^{-j\frac{2\pi}{N}\phi'} \pm Be^{-j\frac{2\pi}{N}(\phi'+}$$

2.2 investigation/oF/RADIX_2^2/FLOW_GRAPH

The exceeding possessions are gotten commencing the radix-2^2 stream chart. These belongings are the necessities to facilitate several radix-2^2 FFT equipment design should satisfy. Assets for the most part rely upon the list of the data(binary). In the Radix-22 condition, the contribution to B/F's should be isolated by right separations, which is finished by info schedulers in the commutator.

Table: 2.1 FFT parameters

No. of points)or samples" in a sequence s(n), N	Complex multiplications in direct computation of DFT NN =A=	Complex multiplications in FFT algorithms N/2 log2 N = B	Speed improvement Factor -A/B
4- 22	16	4	=4.0
8 -23	64	12	=5.3
16 - 24	256	32	=8.0

The main direct also understood booking move towards is utilizing postpone appearance among exchanging systems as appeared in Fig./8. In this model, two approaching information are separated by 16 as well as the yield have the separation of 4. An information defer row utilizing 4 move records is set at the inferior contribution to delay the information by 4 cycles. Amid Phase I (P1), the postponed information enters the lesser M/U/X whilst the greater info enters the upper MUX for 4 cycles. After 4 cycles, M/U/X's change to Phase II (P2) where the higher M/U/X obtains information starting the subordinate input as well as the lower MUX yield information commencing the upper information. Together with the information turning out from the upper yield postpone line, the lower yield is isolated by a separation of 4. Above tabel shows an information stream precedent utilizing this information booking strategy. The usage of this information scheduler necessitates just F/I/F/O's to make the defer lines as well as M/U/X's among a manage flag to understand the exchanging system. In any case, all information are moved inside the postpone arrange each clock cycle and these exercises devour huge powerful vitality. This is especially evident when the framework works at elevated recurrence in support of towering throughput. Along these lines, we suggest a narrative info planning calculation to facilitate takes out the defer positions along with information moving to diminish the general exchanging exercises and the design territory.

Table: 2.2 algorithms for DIF FFT and DIT FFT

Properties Radix-2^2	DIF	DIT
Butterflies	b_{n-s}	b_{n-s}
Trivial rotations (odd s)	$b_{n-s} \cdot b_{n-s-1} = 1$	$b_{n-s} \cdot b_{n-s-1} = 1$
Non-trivial rotations (even s)	$b_{n-s+1} + b_{n-s} = 1$	$b_{n-s-1} + b_{n-s-2} = 1$

Related work:

We present a novel F/F/T design named Radix-22 feed/forward different way defer commutator (R22FFMDC) to improve the throughput of the past M/D/C topologies in addition to diminish vitality utilization through using Radix-22 calculation. The probable F/F/T workstation accomplishes the most extreme throughput of 1.2/G sample/s at 600 MH'z also 1 V bring. At 0.6 V, it creates a through_put of 800.00 M samples/s also expends just 60.3 m W (77.2 n J/FFT), which is the most excellent vitality/change for superior space FFTs.

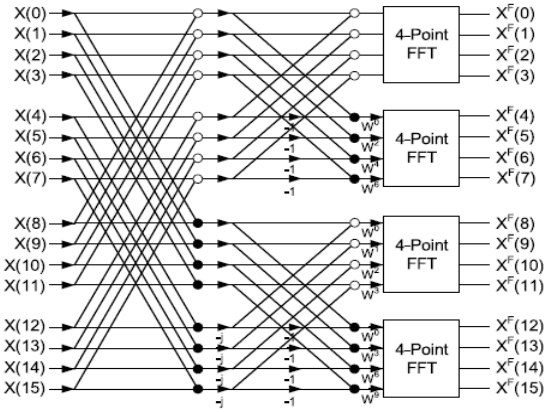

Fig. 1. stream/grid of 16.00-point/Radix-4 F_F_T algorithm.

The Radix-22 calculation was created to acquire the basic organize organization of Radix-2 however embrace task along with equipment sparing system from Radix-4. This makes Radix-22 appropriate in favour of V/L/S/I execution of short power F/F/T. In [9], by allowing for the initial 2 disintegration's of Radix-2 mutually, condition(3) canister be written in an additional structure as in condition (4)

$$X[k] = \sum_{n=0}^{N-1} x[n].W_N^{kn}, \quad k = 0, 1, \ldots, N-1 \qquad \text{--(3)}$$

$$X[k_1 + 2k_2 + 4k_3] = \sum_{n_3=0}^{\frac{N}{4}-1} [H(k_1, k_2, k_3)].W_{\frac{N}{4}}^{n_3 k_3} \qquad \text{----(4)}$$

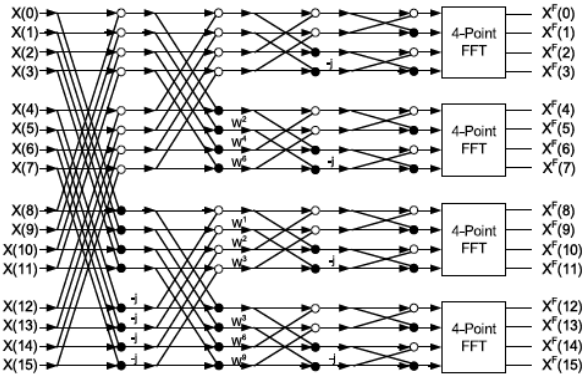

Fig. 2. Flow-graph of 16.0-point-radix-22 F/F/T_algorithm

N/point F/F/T is acquired beside emphasizing the technique in (3) as well as (4) larger than (log2N – 1) times. This lessens the quantity of tasks along with equipment execution charge (multipliers also adders).

This technique preserve be connected to acknowledge Radix-4 otherwise elevated radix calculations through breaking down X [k] keen on at least 4 sub-F/F/T [8]. Condition (5) demonstrates the decay of the Radix-4 F/F/T calculation and Fig. 1 clarifies the stream chart of it. The dark dabs speak to multifaceted subtractions along with the white spots speak to complex increases. Among Radix-4 or else superior radix/F/F/T, the quantity of multipliers moreover adders additional abatements

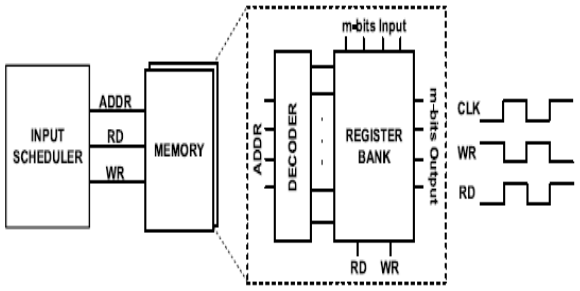

Figure: 3 Register-based memory design

Built in Self-Repair (BISR) incorporates repetition circuits related with fizzled column address stores to drive excess line word lines, along these lines deterring the supply and typical translating of a substitute locations. NOT comparator rationale looks at a fizzled column address created and put away by BISR circuits to a line address provided to the memory cluster. A TRUE comparator arranged in parallel with the NOT comparator at the same time thinks about blemished column address flag to the provided line address. Since NOT correlation is performed rapidly in unique rationale without setup and hold time requirements, timing sway on an ordinary (non-excess) push disentangle way is unimportant, and since TRUE examination, however conceivably slower than NOT examination, itself distinguishes a repetitive column address and in this way need not utilize a N-bit location to chose word-line unravel, repetitive line tending to is fast and does not antagonistically corrupt execution of a self-fixed semiconductor memory exhibit.

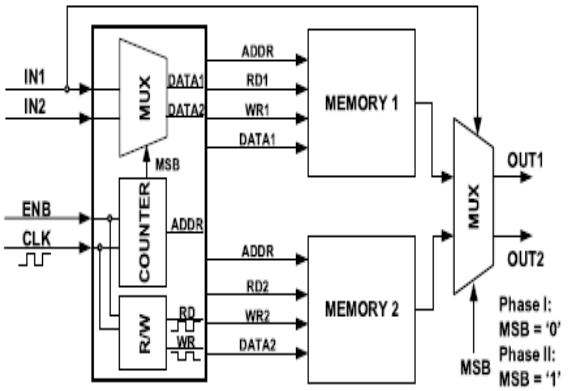

Figure: 4 input scheduler

By giving excess dealing with at the predecode circuit level, as opposed to at a starter address substitution arrange, get to times to a BISR memory exhibit as per the present innovation are improved

		CLK	In1	In2	Mem1	Mem2	Out1	Out2
Phase I	Out1 reads from Mem2	0	0	16	0	16	~	~
	In2 writes to Mem2	1	1	17	1	17	~	~
	Out2 reads from Mem1	2	2	18	2	18	~	~
	In1 wrtie to Mem1	3	3	19	3	19	~	~
Phase II	Out1 reads from Mem1	4	4	20	20	16	0	4
	In2 write to Mem1	5	5	21	21	17	1	5
	Out2 reads from In1	6	6	22	22	18	2	6
		7	7	23	23	19	3	7
Phase I	Out1 reads from Mem2	8	8	24	8	24	16	20
	In2 writes to Mem2	9	9	25	9	25	17	21
	Out2 reads from Mem1	10	10	26	10	26	18	22
	In1 wrtie to Mem1	11	11	27	11	27	19	23
Phase II	Out1 reads from Mem1	12	12	28	28	24	8	12
	In2 write to Mem1	13	13	29	29	25	9	13
	Out2 reads from In1	14	14	30	30	26	10	14
		15	15	31	31	27	11	15
	...	.	.	.	.	.	.	.

Figure: 5 input scheduling algorithm

A booking calculation is utilized to arrange the crossbar switch, choosing the request in which parcels will be served. Past outcomes have appeared with an appropriate planning calculation, 100% throughput can be accomplished. In this paper, we present a booking calculation called iSLIP. An iterative, round/robin calculation, iSLIP container accomplish 100% throughput on behalf of consistent traffic, yet is easy to execute in equipment. Iterative and no iterative adaptations of the calculations are introduced, alongside adjusted variants for organized traffic. Reproduction results are introduced to demonstrate the execution of iSLIP under considerate and bursty traffic conditions. Model and business executions of iSLIP exist in frameworks with total data transmissions going from 50 to 500 Gb/s. At the point when the traffic is non uniform, iSLIP rapidly adjusts to a reasonable planning strategy that is ensured never to starve an info line. At last, we depict the execution intricacy of iSLIP. In light of a two-dimensional (2-D) exhibit of need encoders, single-chip schedulers have been developed supporting to 32 ports, and settling on around 100 million planning choices for each second.

Proposed work

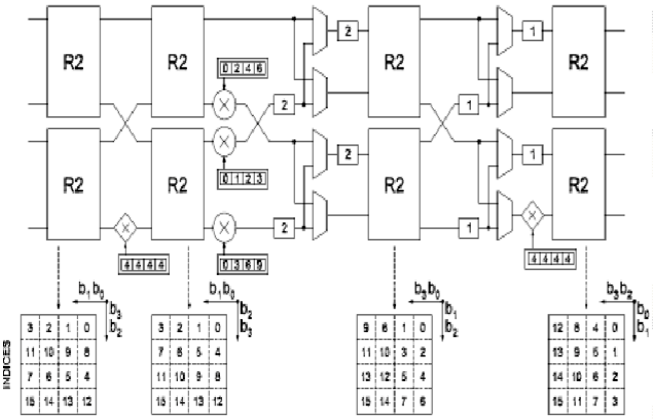

Figure 6: proposed architecture

The higher than outline demonstrates 4-parellel radix - 2^2 feed-forward engineering in favour of demolition in recurrence quick Fourier change (D/I/F-F/F/T). This engineering forms 4 tests in parallel moreover preserve procedure the various info arrangements one subsequent to other to provide the yields.

The request of the information appeared at the base of every phase speaks to the request of the information in which the information ought to survive sustained. The information ought to subsist agreed in the correct request as referenced in the outline along with the yield motivation be gotten in the request referenced in the chart. An essential favourable position of feed-forward F/F/T design is 100% butterfly usage proportion. So it requirements fewer figure of butterflies which implies small territory along with low authority.

III. RAD_IX_2^KFEEDFORWARD FFT

CONSTRUCTION

In Radix-2^k feed/forward engineering, there are III conceivable revolutions. They are inconsequential turns, non-minor pivots also universal revolutions. Minor turns are revolutions in favour of which the estimation of Ø is also 0 or N/4 or else N/2 or 3N/4 for example the examples should be turned through either 0 otherwise 270.00 if not 180^0 or 90^0. They described trifling in light of the fact that these turns should be possible by trading the genuine and fanciful parts as well as additionally altering the indication of them. In this way, multifaceted augmentation preserve be kept away from in actualizing such revolutions. Inconsequential revolution resolve be completed at odd stages alone. Non trifling turn's determination be finished presently in even periods. By and large, for advanced estimations of „k " in radix-2^k feed-forward engineering, the non-insignificant turns canister be streamlined hooked on revolutions by W(8) also W(16), which incorporate diminished arrangement of points, in addition to universal pivots in favour of residual edges. These revolutions through W(8) moreover W(16) can disentangled through the utilization of trigono_metric characters, multiply of coeffi.. Along with portrayal of coefficients in canonical\ signed\digit\(C\S\D). Turns by W/(8) consider just the points of π/4. Revolutions by W/(16) believe just the edges of π/8. In favour of Radix-2^k feed/forward F/F/T engineering, the kind of revolution rehashes each k phases For instance, radix 2^3 feed/forward engineering necessitates non-minor revolution each 3 phases.

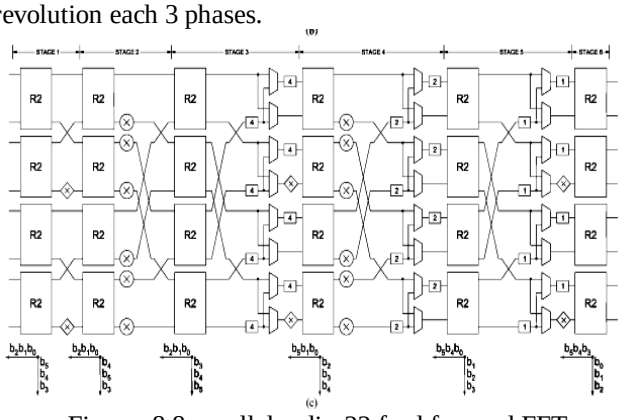

Figure :8 8-parallel radix-22 feed forward FFT

3.1 CONDITIONS

The stipulations of several P/parallel_/N/point radix-2^k feed*forward structural design are exposed beneath. Number of parallel_samples=P= 2^p Number/of/butterflies=(P/2) * log N(base 2)= P * log N(base 4) Number of complex adders =2 * P * log N(base 4)=P * log N(base 2) Number of rotators = ((3 * P)/4) * (log N(base 4) – 1) for P > 2 2 * (log N(base 4) – 1) for P = 2

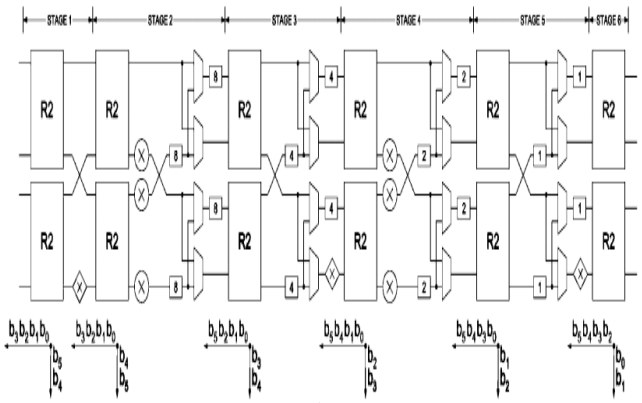

Figure :9 4-parallel radix-22 feed forward FFT

Throughput is the quantity of yield tests got in element occasion. Throughput_per/clock/cycle = P = Number of equivalent examples Latency is the occasion span flanked by the primary information connected moreover the main yield got for example it specifies the occasion occupied through the framework to procedure a contribution to provide the individual yield. In the projected engineering, inactivity = N/P At every stage„s", Distance end to end of the cushion in rearranging organization L = N/2^(s+1) Total example recall required = N–P Maximum recollection expected to carry out contribution reallocation alongside FFT=N–(N/P) Maximum recollection expected to achieve yield rearrangement alongside FFT = N greatest remembrance expected to execute together info rearrangement as well as yield reorganization alongside F/F/T = N Where, N is the quantity of contributions to a solitary arrangement P is the quantity of similar information tests in the current phase of activity a quantity of different certainties concerning feed forward design are 1. Memory dimension motivation be same in support of every figure of equivalent examples. 2. Both D/I/F F/F/T also D-I-T F-F-T necessitate similar digit of equipment segments 3. Most extreme recollection required is N, anywhere N is the quantity of tests in an information succession. 4. Mainly reasonable design resolve be chosen dependent on the throughput as well as inertness prerequisites of the necessary submissions

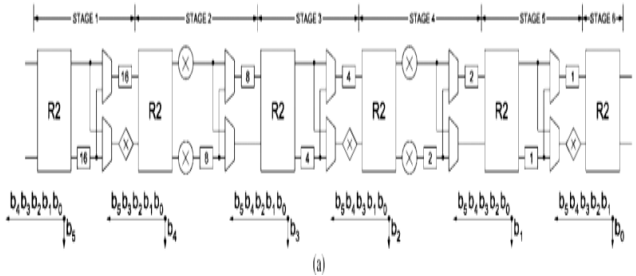

Figure: 10 2-parallel radix-22 feed forward FFT.

IV. IMPLEMENTATION

4.1 COMPONENTS

4.1.1 RADIX-2/BUTTERFLY

The 2contributions to the butterfly dependably vary in their turn point moreover beside 0 or else by N/4. Additionally at every phase..s‟, the II information sources which contain records contrasting just in the bit b(n-s) determination be prepared mutually in a butterfly

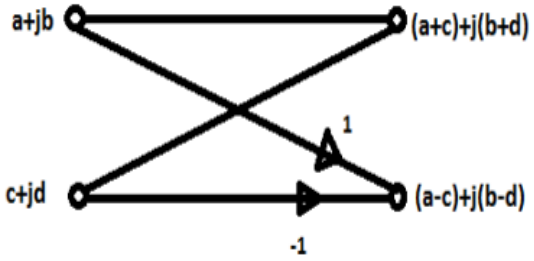

Figure :11 butter fly arch

4.1.2TRIVIAL ROTATION

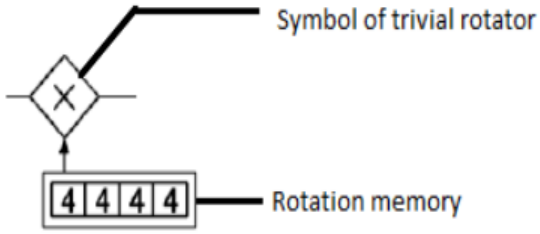

Figure :12 memory flow

Here the unimportant revolution happens just through N/4 for example multifaceted augmentation by (- j). The essential activity of minor turn preserve be executed by exchanging the genuine and fanciful segments and additionally varying the indication of them.

4.1.3 NON-TRIVIAL ROTATION

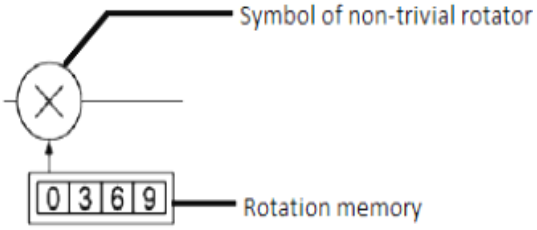

Figure :13 Non trivial rotation

Non inconsequential revolutions motivation is completed just in smooth phases. In destruction in recurrence quick Fourier/change, the contributions among lists to facilitate fulfills b(n-s+1)+b(n-s)=1 will unaccompanied experience non inconsequential pivot though in annihilation in occasion quick Fourier change, the contributions among files to facilitate fulfils b(n-s-1)+b(n-s-2)=1 resolve unaccompanied experience non insignificant turn.

4.1.4 DATA_SHUFFLER

Information shuffler comprises of II parts. They be supports also multiplexers. In the outline underneath, L signifies the distance end to end of the support. In support of initial L/clock/cycles, the multiplexer's determination procession will be locate to 0. At that point on behalf of next L*clock/cycles, the choice row spirit be put to 1 as well as the modify will occur at the same time for each L clock cycles.

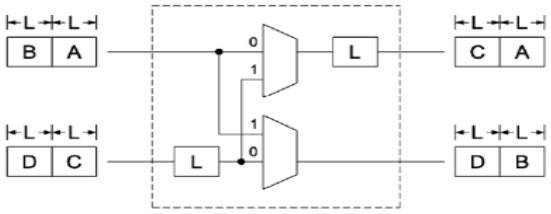

Figure :14 data suffuling

In the exceeding chart, for initial L/clock cycles, A determination be put away in yield cradle as well as C resolve be put away in information cushion. In favour of the continuous L_clock/cycles, multi/plexer's choose appearance motivation subsist put to 1. In this way, B spirit be straightforwardly send to the inferior yield. The esteem A commencing the yield cradle will be send to the higher yield. The esteem C determination be stimulated commencing information cushion to yield support. The esteem D willpower is enthused to the info support. At long last in yield, An also B resolve be accessible in the subsequent clock cycle along with C as well as D determination be accessible in the following clock/cycle. Therefore, the data sources are rearranged to obtain the ideal request. The estimation of L is dependably an intensity of II. The manage signs of the multiplexer be able to specifically gotten beginning the bits of a counter. VHDL language is picked for programming since it bolsters part of circle activities and genuine operands. The writing computer programs was completed as a fundamental L/S/M (limited/state/machine) demonstrate. At first, the whole circuit be partitioned into seven squares. Every individual square is checked for legitimate working and afterward, the squares are assembled step by step in F_S_M representation moreover they are checked plus blunders also coherent mix-ups were corrected.

V. RESULTS

At that point, the yield was acquired in favour of a solitary 17 point input arrangement through inactivity of 19.

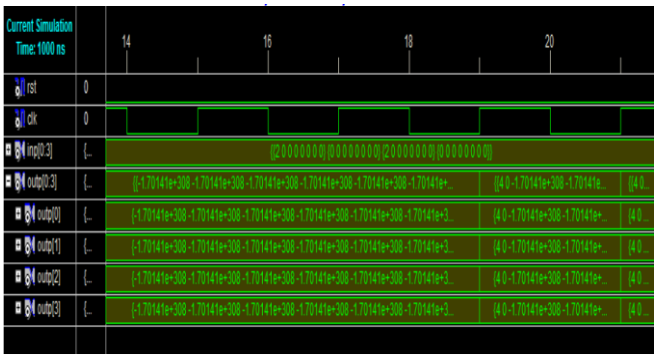

Figure: 15 1024 FFT processor output

At that point, the squares are consolidated so as to accomplish the hypothetical dormancy for example idleness = N/P = 4. It be seen to facilitate every phase in F/S/M display obtains single clock sequence on behalf of implementation. Along these lines, it was presumed with the intention of the hypothetical idleness (for this situation, inactivity = 4) canister be gotten just by decreasing the whole circuit hooked on a solitary square.

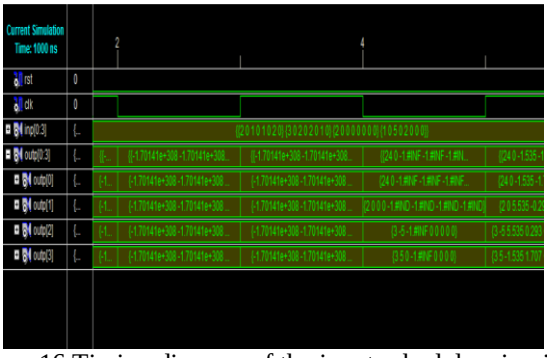

Figure: 16 Timing diagram of the input scheduler circuit

5. After that, the program is distorted in command to procedure the incessant stream of inputs by recurrence of convinced periods in F/S/M.

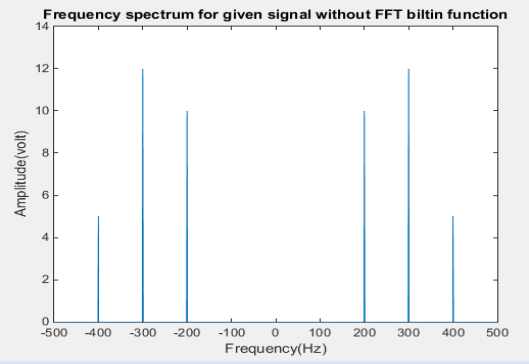

Figure : 17 FFT frequency vs amplitude

The whole model is executed in Xilinx 9.2i utilizing genuine information type. In any case, the genuine information category can't be combined as well as subsequently net list insincerity be made. In this way, the difference in information kind commencing genuine to Q(m.n) position is creature finished. Q(22.10) is chosen so as to give most extreme exactness.

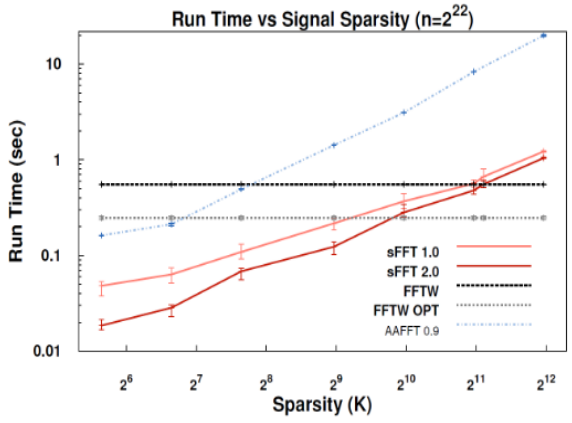

Figure :18 high speed FFT processor

The two attempts to be done are, initial an orchestrated net list is to exist acquired through actualizing the regulation utilizing Q(22.10) configuration also figure of adders multipliers moreover reminiscence are to be broke down. The moment one is towards diminish non paltry turns utilizing diverse properties and in this manner further decreasing the quantity of segments expected to execute the engineering.

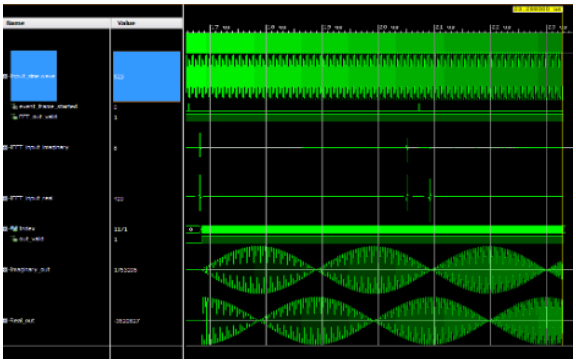

Figure : 19 simulation results

Figure :20 RTL schematic of proposed model

VI. CONCLUSION

Feed forward design spares more region than different structures as N end up bigger. Likewise, feed/forward engineering is more effective than parallel criticism models when a few examples are handled in parallel. The proposed structure additionally accomplishes high throughput. In this manner, it is effective as far as both region and execution. Another favourable position of the proposed engineering is that, the use proportion of the butterflies is 100%. In this way, no piece of design stays inactive along these lines playing out the task quicker and lessens the authority utilization also it necessitates fewer numeral of segments because it accomplishes 100% use proportion. Utilizing this projected engineering, it is conceivable to accomplish the through-put arranged by giga tests every instant at exceptionally little latencies.

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