Design of a combinational circuit by optimizing EX-OR gate

Jahnavi. Ratnam, E. Raghuveera

Abstract*: *Full Adder is one of the effective structural blocks and basic elements in many of the architectures available in VLSI and DSP domains. Adder is an adaptable element and it is mainly known for addition and multiplication as its principal functioning element. In VLSI it is used in ALU design, Address generation in processors, Multipliers etc... In DSP it is used for conversion, Signed addition and Signed multiplication, Transformations and Signal processing applications. So, designing of an adder in an effective manner is an essential factor. The recent circuit designing in VLSI is mainly to concentrate on power and delay reduction. In this paper a full adder is designed by optimizing XOR gate in mentor graphics 130nm and 45nm technology. Transistor count, power, delay are compared with the existing adder.

Index Terms: Full adder, Mentor graphics, Hybrid full adder, CMOS full adder, Novel full adder, Transistor count, Power, Delay.

I. INTRODUCTION

Digital electronics has become an essential part in everyone's life in the form of mobile phones, Laptops, sensor nodes and major portable devices. The circuit delay is scaled down by 30% while performance and transistor density are increased by two times with a threshold voltage reduction of almost 15% roughly for every two years. The increase in resources is directly proportional to rise in IC temperature and affects battery life. So, the battery life of these devices has to be improved by reducing the power consumption and area. This can be done by designing optimized low power[1][6][8] VLSI circuits such as adders, multipliers etc… As full adders are very important because they are the basic building blocks of many signal and image processing algorithms[6], it is required to design adders that occupy minimum area and consume minimum power.

The effectiveness of digital applications relate to the performance of the arithmetic circuits such as adders, multipliers, and dividers. Because of the basal role of addition in all the arithmetic operations, number of efforts has been made to explore efficient adder structures, for example carry select, carry skip, conditional sum, and carry look-ahead adders. In all these adders full adder is at the centre of attention.

Full adders are mainly made of two modules, including 2-input XOR 2-to-1 multiplexer (2-1-MUX) gate. The XOR/XNOR [5] gate is the major consumer of power in the FA cell. Therefore, the power consumption of the FA cell can be reduced by optimum designing of the XOR/XNOR gate. The XOR/XNOR gate has also many applications in digital circuits design.

In this paper a full adder is designed by optimizing the EXOR gate. The EXOR plays a major role in the generation of sum in any full adder; optimization of EXOR gate makes significant variations in power, delay and transistor count. The design is verified for its functionality in mentor graphics 180nm technology. Power and delay analysis is carried out in the simulation environment. The results are compared with the existing adders like hybrid full adder and CMOS full adder[9][10]. Initially the full adder was designed with 28T using CMOS technology as shown in below figure.

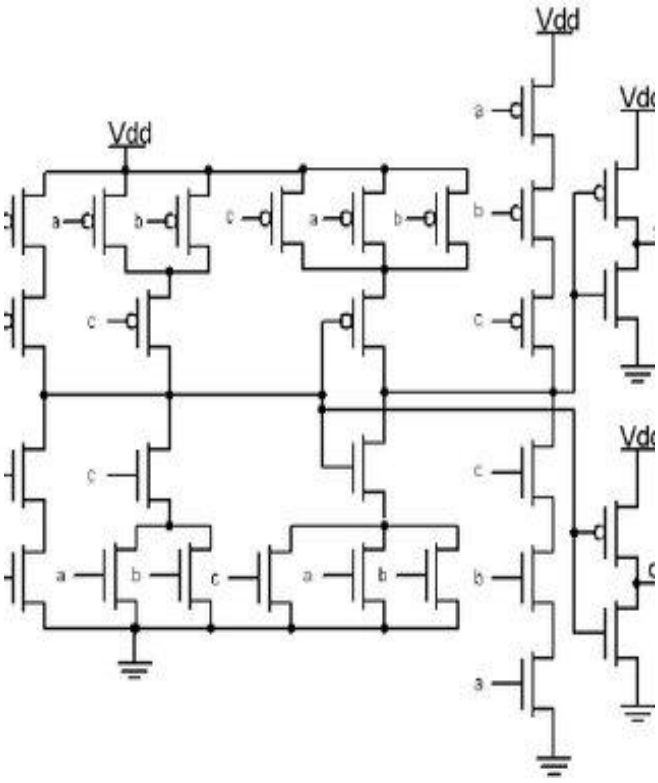

Figure 1. Conventional CMOS full adder

The arrangement of the paper is as follows. In section II, design work for the proposed work is elaborated. The discussion of results is presented in section III. The conclusion of the paper is in section IV.

II. DESIGN APPROACH

The implementation started with the basic CMOS full adder[9] which consists of 28 transistors.

Revised Manuscript Received on May 06, 2019

Jahnavi. Ratnam, Department of ECE, Koneru Lakshmaiah Educational Foundation, Vaddeswaram, Guntur, Andhra Pradesh, India.

E. Raghuveera, Department of ECE, Koneru Lakshmaiah Educational Foundation, Vaddeswaram, Guntur, Andhra Pradesh, India.

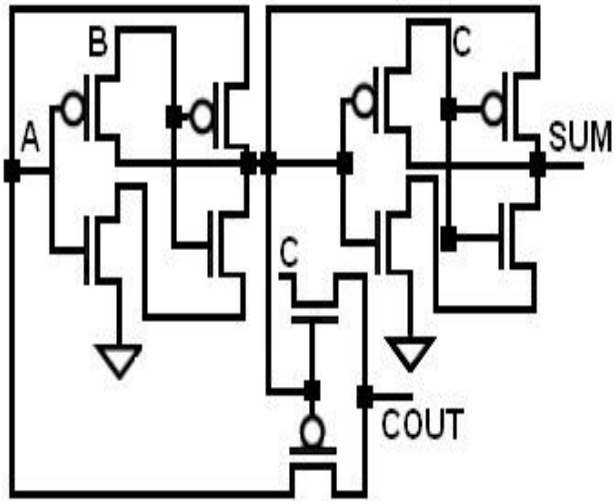

Figure 2. Designed Full Adder

The designed full adder consists of 10 transistors shown in the figure 1. It consists of two XOR gates and a 2:1 MUX. The first gate performs two input XOR operation and the result is again XORed with the third input to generate the output sum. The XOR gate was designed using two NMOS and two PMOS transistors. The 2:1 MUX has two inputs with a select line S which generates output carry.

$$SUM = A \oplus B \oplus Cin \quad (1)$$

$$CARRY = A.B + B.Cin + Cin.A \quad (2)$$

The digital logic gate XOR in figure 3 performs the 'exclusive OR' function. If both the inputs are HIGH (1) or LOW (0) then the output of the gate is LOW (0). If one of the inputs is HIGH (1) then the output is HIGH (1).

$$A \oplus B = \bar{A}B + A\bar{B} \quad (3)$$

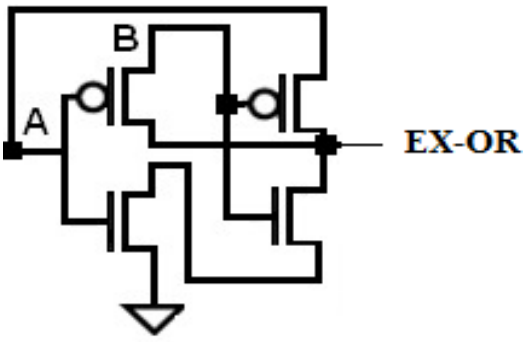

Figure 3. An Ex-Or Gate

A multiplexer is a combinational logic circuit which selects no. of analog or digital signals and gives the selected input signal to a single output line. The required input signal is selected using a select channel S.

$$CARRY = (\bar{C}inS + A\bar{S}) \quad (4)$$

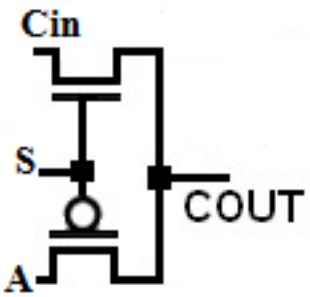

Figure 4. A Multiplexer

III. RESULTS AND DISCUSSION

The basic CMOS 28[10] transistor full adder is compared with the designed full adder in terms of power, delay and transistor count. The circuit schematics are designed and simulated in mentor graphics 45nm technology using pyxis schematic.

The output of the full adder varies for different patterns. For all possible input patters the simulation has been performed. The delay for 28 transistor full adder is 0.1759us. The delay for the designed full adder is 4.81ns.

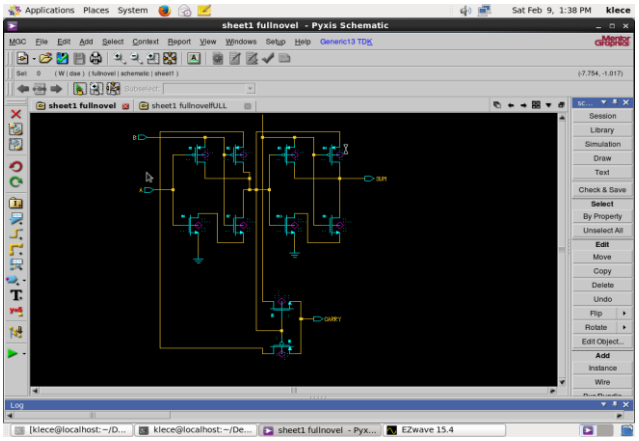

Figure 5. Schematic of designed Full Adder

The power dissipation for 28 transistor full adder is 26.497nW. The power dissipation for the designed full adder is 103.2nW.

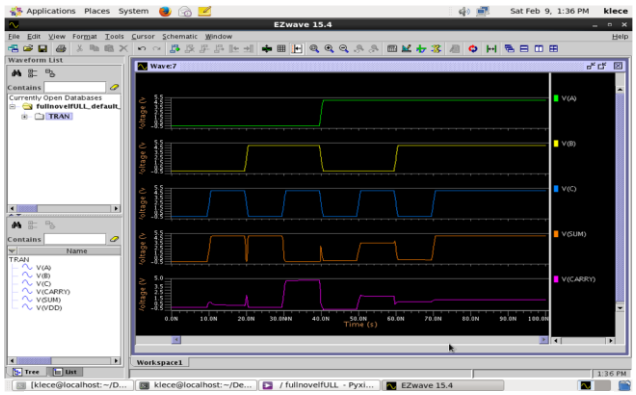

Figure 6: Simulation Result of Proposed Full adder.

The reduction in power consumption for the designed full adder enables building large systems which depends on full adder whose performance in terms of battery life can be extended for portable devices. Miniaturization of the system is also possible due to the reduction in area as the transistor count is also reduced.

No. of transistors	28	22	10
Power (uW)	26.497	24.187	103.2
Delay (ns)	0.1795	0.1825	4.81
PDP (e^{-12})	4.756	4.414	$4.96e^{-8}$

Table 1: Comparison of simulation results (No. of transistors, Power (uW), Delay (ns), PDP (e^{-12})) with 0.6-V power supply voltage at 100MHz.

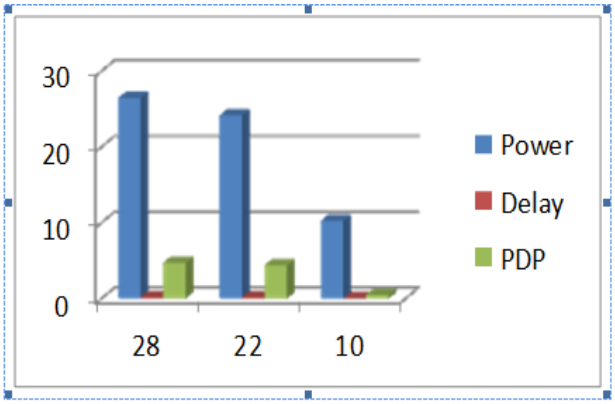

Figure 7. Comparison graph for Power, Delay and PDP.

IV. CONCLUSION

The design and simulation of basic CMOS full adder with 28T, hybrid full adder with 22T is performed initially in mentor graphics. The power, delay and PDP of the two designs are analyzed. The designed structure which consists of 10T is also simulated in mentor graphics 45nm technology with a supply voltage of 0.6V at 100MHz frequency. It is observed that the delay and power consumption is reduced when compared to the 28 and 22 transistor design. As the no. of transistors decreases the area consumed also decreases. But always there will be a trade-off between power and delay as delay decreases power increases and if delay increases power decreases. The proposed design can be used in DSP applications in the optimization of area, power and delay.

REFERENCES

1. Hamed Naseri et.al., "Low-Power and Fast Full Adder by Exploring New XOR and XNOR Gates", IEEE Tranactions Very Large Scale Integration. (VLSI) Syst., Vol. 26 ,8, pp. 1481-1493, Aug. 2018.
2. A. Kumar et.al., "Design of robust, energy-efficient full adders for deep-submicrometer design using hybrid-CMOS logic style," IEEE Transactions Very Large Scale Integration. (VLSI) Syst., vol. 14, no. 12, pp. 1309–1321, Dec. 2006.
3. H. Wu et.al., "A new design of the CMOS full adder," IEEE Journal of Solid-State Circuits, vol. 27, no. 5, pp. 840–844, May 1992.
4. R. K. Sharma et.al., "Low voltage high performance hybrid full adder," Engineering Science. Technology., Int. J., vol. 19, no. 1, pp. 559–565, 2016.
5. W.-S. Feng et.al., "New efficient designs for XOR and XNOR functions on the transistor level," IEEE Journal of Solid-State Circuits, vol. 29, no. 7, pp. 780–786, Jul. 1994.
6. Yingtao Jiang et.al, "Design and Analysis of Low–Power 10-Transistor Full Adders Using Novel XOR-XNOR Gates", IEEE Transactions on Circuits and Systems—II: Analog and Digital Signal Processing, Vol. 49, No. 1, January 2002, pp. 25-30.
7. Dr. Shaik Meeravali et.al., "Implementation of CMOS Full Adder with Less Number of Transistors for Full Swing Output", International Journal of Engineering Research & Technology, Vol. 4 Issue 06, June 2015, pp. 1172-1175.
8. Md. Anis Alam et.al., "A New Design of Low Power High Speed Hybrid CMOS Full Adder", 2014 International Conference on Signal Processing and Integrated Networks (SPIN), March 2014, pp. 448-452.
9. N. Weste, and K. Eshranghian et.al., "Principles of CMOS VLSI Design: A System Perspective," Reading MA: Wesley, 1993.
10. W. Fichtner et.al., "Low-power logic styles: CMOS versus pass-transistor logic," IEEE Journal of Solid-State Circuits, vol. 32, no.7, pp. 1079–1090, Jul. 1997.
11. Y-H. Hung et.al., "Novel 10-T full adders realized by GDI structure", IEEE Symp. Integrated circuit, pp. 115-118 Sep.2007.
12. Pradeep Kumar et.al., "Analysis and Comparison of Leakage Power Reduction Techniques in CMOS circuits", 2015 2nd International Conference on Signal Processing and Integrated Networks (SPIN), February 2015, pp. 936-944.

AUTHORS PROFILE

Jahnavi Ratnam is pursuing M. Tech (VLSI), Department of Electronics and Communication Engineering from Koneru Lakshmaiah Educational Foundation (Deemed to be university), Guntur, Andhra Pradesh, India.

E. **Raghuveera** received the M. Tech. In VLSI System Design of Electronics and Communication Engineering from VNT VJIET, Hyderabad, Telangana India, in 2012 and B. Tech. in Electronics and Communication Engineering, from RGMCET, Nandyal, Andhra Pradesh, India, in 2006. He was a Faculty Member with the Department of Electronics and communication Engineering, JNT University, Ananthapuramu, Andhra Pradesh, India, He joined in the Department of Electronics & Communication Engineering KLEF(Deemed to be University), Green Fields, Veddeswaram, Guntur, Andhra Pradesh, India. In 2016, where he is currently a Asst. Professor. His current research interests include VLSI designs, video/image signal processing, and low-power VLSI circuit designs.