Implementation Of Most Appropriate Leakage Power Techniques In Vlsi Circuits Using Nand And Nor Gates

M.Siva Kumar, Syed Inthiyaz, P.Venkata Krishna ,Ch. Jyothsna Ravali, J.Veenamadhuri, Y.Hanuman Reddy, Sk. Hasane Ahammad

Abstract: ***The speedy boom of semiconductor generation and growing call for portable devices powered gadgets via battery has led the constructors to scale back the capabilities size resultant decreased threshold voltage in addition to there by way of enabling integration of relatively complex capability on a single chip. In each technological and implementation components Chip's most strength method is adopted. Sleepy stacked with LECTOR technique. This includes leakage control transistor introduced between pull up and pull down circuit.The Stack effect might be brought through substituting every current transistor with two half of sized transistor. It supplies the challenge of the location because of utilization of greater transistor toward keeping the circuit kingdom at some point of sleep mode. As CMOS era scales down, the supply voltage must be decreased such that dynamic energy may be kept at realistic degrees.***

Keywords: ***LECTOR technique, CMOS.***

I. INTRODUCTION

In this contemporary international, due to development of battery-based totally devices with the restrained electricity competencies which desires important requirement of strength performance and power-put off product. This factors are of top notch task to the electronic designers[1]. Similarly, in VLSI circuit design strength consumption of circuit is of situation. [2]. The hassle of strength consumption is main issue earlier than the evolution of mobile technology. Standard method is developed for factors to overcome problem of area consumption, delay and power usage of the designed circuit. [3].Based on the product and alertness requirement person need to pick out maximum appropriate method. In case of high performance transportable gadgets electricity dissipation is the foremost problem. Three components performs essential role for energy consumption which can be all leakage present day, brief circuit and dissipation of energy from dynamic switching[4].

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In CMOS circuit overall strength dissipation turns into and dominant components due to continuous scaling of threshold voltage.

Even in adiabatic method dissipation of energy took place for constant enter values. However, energy dissipation takes place even for consistent input alerts of the adiabatic circuits where electricity-clocks is used for charging and discharging of output nodes [6]. Due to continuous scaling in CMOS generation in adiabatic manner dissipation because of Leakage within the be circuit design will carry out as dominant thing for overall dissipation of strength same as conventional good judgment characteristic of the CMOS devices. In adiabatic circuit electricity gating approach is followed for minimizing leakage and dynamic power of the gadget. In this approach at idle nation strength gating device shut down the devices. The adiabatic circuit is notably differing from CMOS circuit due to signal waveforms and clocking schemes in conventional procedures. In this scheme it is vital that their want to be enough distinguish among switch with Power-gating and strength clock utilized for turning-off. In adiabatic schemes various power gating are applied, [7]. Among the several gating methods voltage scaling method outperforms in case of adiabatic based CMOS good judgment circuits. In the mid performance ranges from (5MHz to 100MHz) deliver voltage scaling in medium-voltage area plays correctly [8]. Based on this numerous adiabatic –circuit with close to-threshold has been proposed without the use of gating power. Due switching strength dissipation is minimized to quadratic on this scenario minimization of energy intake by using deliver voltage technique. This strategies has the extreme problem of performance degradation. Subsequently, the excessive overall performance requirement have been fulfilled by means of scaled cost of threshold voltage. But this approach has the serious drawback of elevated leakage modern which positioned forth the predominant issue for high overall performance circuit with low electricity usage [9].In this paper, proposed a new technique, as a result choice to leakage electricity VLSI designers. Further extra, summarized the present technique as well as diagnosed the problem towards energy reduction.

RELATED WORK:

In existing, most of them have suggested a different method towards control leakage power consumption. Few of them focused on Lector technique. We implemented different techniques such as Lector, Sleepy keeper, sleep transistor, leakage feed-back approach for nand and nor

gates ,lector is taken in a way that one nMOS and pMOS are kept between the pull-up and pull-down transistors and sleepy keeper is having sleep and sleep bar modes, which becomes active and inactive one nMOS and one pMOS are connected in series and same at the bottom but alternatively and in the middle a pull up and pull down networks are kept. In sleep transistor is having sleep and sleep bar modes, which becomes active and inactive pull-up and pull-down networks are kept in between the pMOS and nMOS. Leakage feedback method is also having sleep and sleep bar other than that the circuit is some critical where pull-up and pull-down networks are connected between the two pMOS and two nMOS and also at the outpoint the nMOS and pMOS is connected parallel and given to the one pMOS and one nMOS The circuit design for proposed techniques are done by using tanner tool and At the final by comparing all the power values we come up with the best technique in terms of power consumption.

Lector Technique: The method of effective stacking transistors had been delivered among the Vdd and the Gnd for leakage electricity discount. In this approach it is having two leakage manipulated transistors i.e. P-type and N-kind which are inserted among the pull up and pull down network of a circuit, in which the source of other is used to manage the LCT gate, consequently termed as self-controlled stacked transistors. Since it's far a self-controlled approach so in this approach no outside combination circuit is required for controlling purpose. This technique has totally low leakage however there's no supply of sleep mode operation. The massive characteristic of LECTOR is that it works correctly in both lively and idle states of the circuit. The main idea to work on lector technique is while reading previous generals we got common point on lector technique is ,it is the best technique for calculating the amount of leakage power when contrasted with other techniques

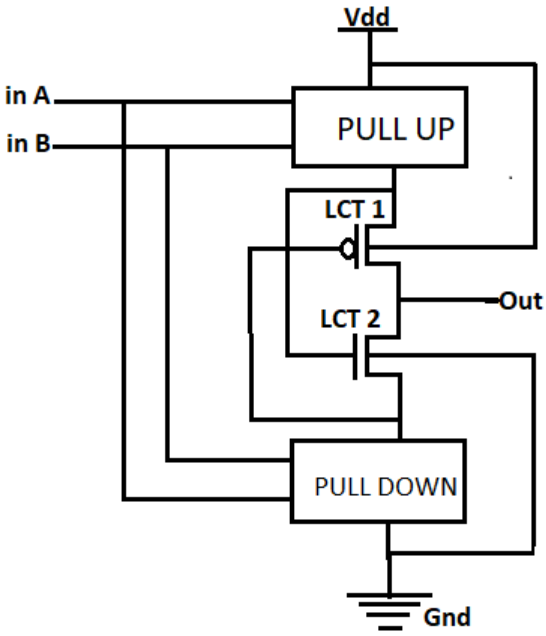


Fig1:Lector Technique

Sleepy Keeper: In this method parallel combination related to pMOS and nMOS transistor is inserted among pull up network and VDD and pull down network and GND. When in the sleep mode this extra nMOS transistor is the only to deliver the Vdd to drag up network and extra pMOS transistor is the only deliver of GND to drag down network due to the fact that transistor off.

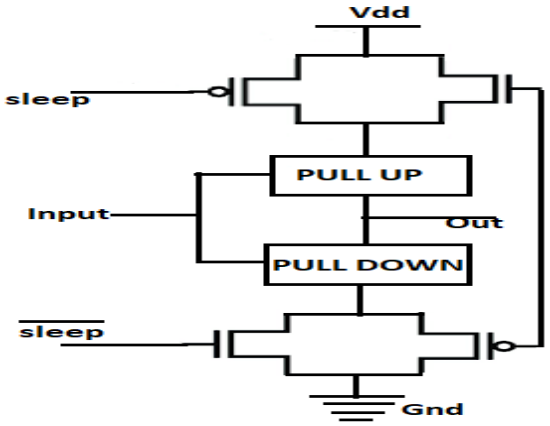


Fig2:Sleepy Keeper

Sleep Transistor: A sleep transistor can be a pMOS or nMOS excessive VT transistor used as a switch to close power off ,materials to components of a design in standby mode. The pMOS sleep transistor is used to replace Vdd supply and so it's miles known as a"header switch". The nMOS sleep transistor controls Vdd supply and so it's miles referred to as a"footer switch."Due to numerous effects of superior sleep transistor the design and implementation are a undertaking. By the concept of sleep transistor it is going for the implementations, on design overall performance, usual power dissipation, region, rout ability, and signal power integrity. Optimal sleep transistor depends on design unique and pick CMOS era manner. The investigations of various sleep transistor techniques in the strength-gating design are based totally on SPICE evaluation. Device modeling turns into so complex in sub-90nm technology .The parameter based device models are the great analysis tool for a fine commercial layout. Quality of a snooze transistor design is especially measured on the bases of three parameters-location performance ,switch efficiency and IR drop. The sleep transistor is optimized in gate period, width, finger size and frame-bias to achieve high transfer and region efficiencies, and coffee leakage cutting-edge and IR drop.

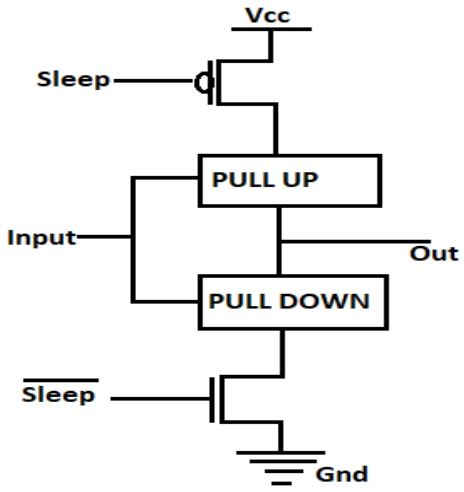
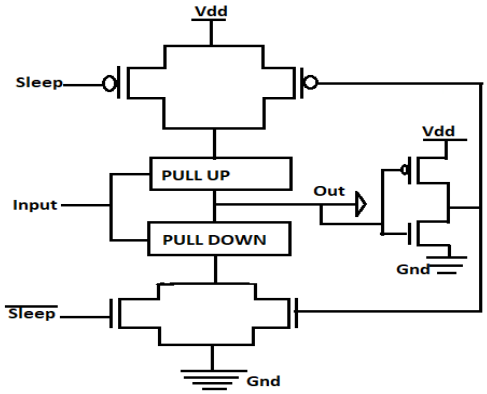


Fig3:Sleepy Transistor

Leakage Feedback Approach: Leakage power dissipat- ion became an

heavy difficulty task for VLSI circuit designers. The ITRS reviews states that leakage power dissipation may result in the influence of total strength intake. The leakage remarks good judgment is based on sleep method. It uses two transistors to hold good judgment at some point of the sleep mode, and are controlled by using the output of an inverter that's fed with the aid of the output of a circuit the usage of leakage comments. A pMOS and nMOS transistor is been brought in parallel to the sleep transistor. The two transistors are operated by way of the output of an inverter of the circuit. In the process of sleep mode, the sleep transistors are became off and one of the transistors which is in parallel to the sleep transistors hold the connection with the right strength rail. In this technique we decreased strength consumption by way of maintaining a fixed of transistors in both the nMOS and pMOS pair. On this approach we use parallel pMOS transistor above pull up community and Vdd. To provide the inverting output of the circuit. We join inverter at the output, an inverter provides the proper good judgment remarks to both pull down nMOS(S') and pull up pMOS(S')sleep transistor as shown in fig. This two transistor beautify the circuit overall performance and maintain the proper common sense of the circuit throughout standby mode.



TECHNIQUES	POWER CONSUMPTION VALUES(watts)	
	NAND GATE	NOR GATE
LECTOR	8.01498e-005 watts	8.151500e-005watts
SLEEPY KEPER	9.26879e-006watts	10.965249e-004watts
SLEEP TRANSISTO	9.5544e-007wattts	11.557436e-007watts
LEAKAGE FEEDBA	11.18969e-006watts	12.119842e-005watts
NORMAL GATES	5.56136e-005 watts	6.25624e-003watts

Fig4:Leakage feedback approach

Results:

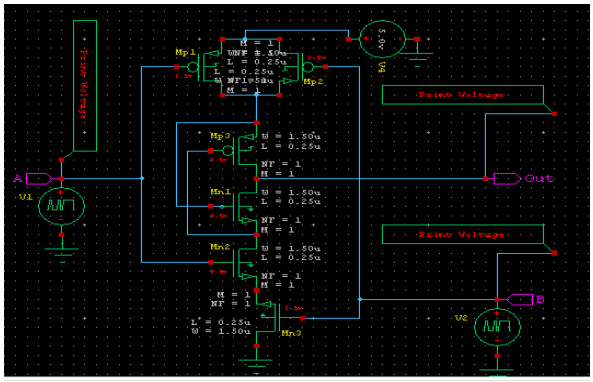


Fig5: The above figure describes lector method using nand gate.

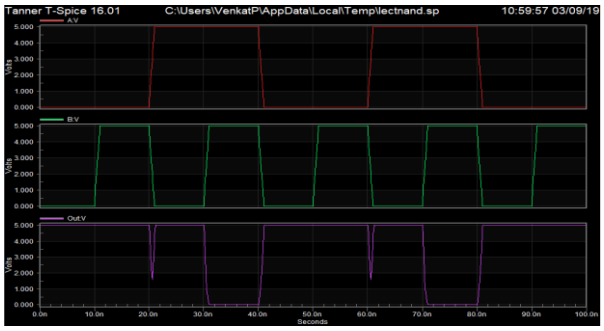


Fig6: The above figure is about Lector with nand gate output graph.

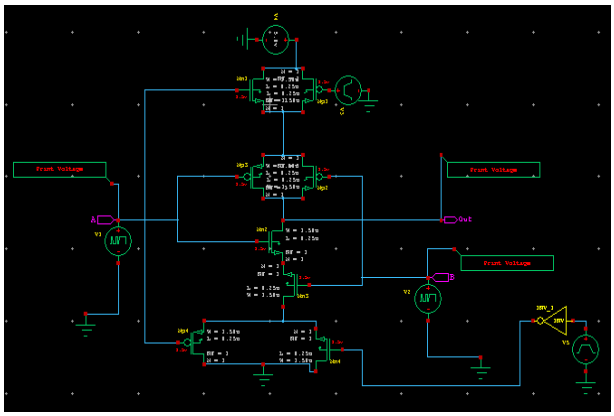


Fig7: The above figure describes sleepy keeper method using nand gate

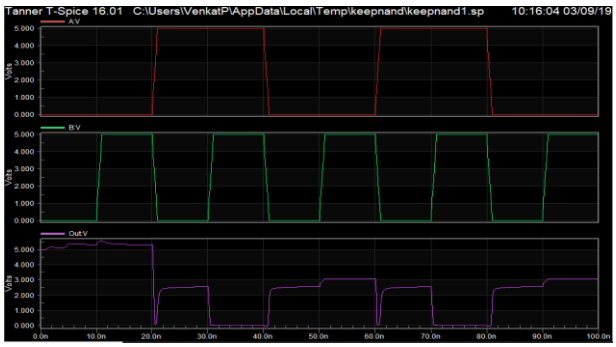


Fig8: The above figure is about sleepy keeper method with nand gate output graph.

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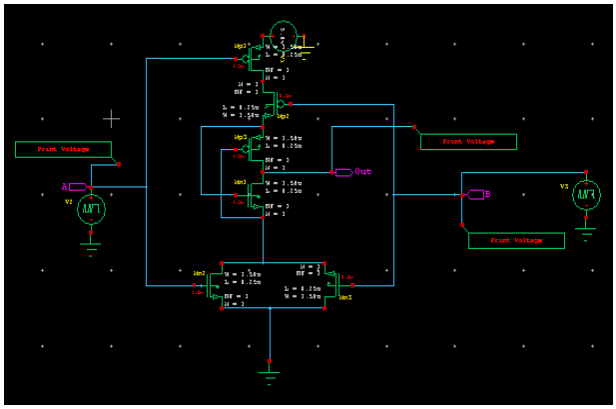

Fig9: The above figure describes lector method using nor gate.

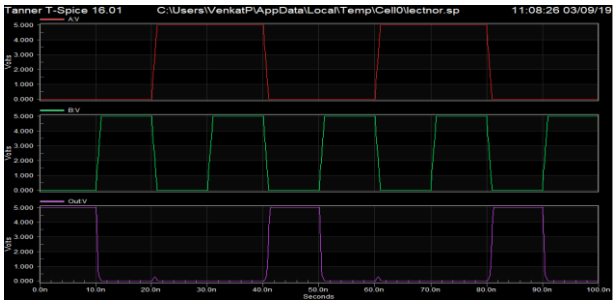

Fig10: The above figure is about Lector with nor gate output graph.

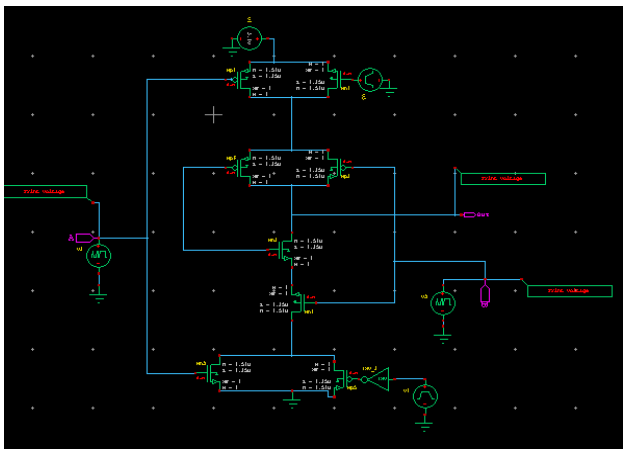

Fig11: The above figure describes sleepy keeper method using nor gate.

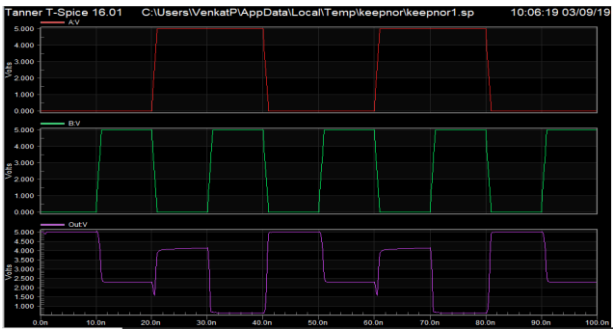

Fig12: The above figure is about sleepy keeper method with nor gate output graph

CONCLUSION

Now a days the main task for designers is to reduce leakage power. There are plenty of techniques to reduce leakage power based on the efficiency of technique if the designers design leakage currents may reduce. From our side lector and sleepy keeper are the best techniques compared to others and also factors like complexity in circuit may also leads to high leakage power

APPENDIX

It is optional. Appendixes, if needed, appear before the acknowledgment.

ACKNOWLEDGMENT

It is optional. The preferred spelling of the word “acknowledgment” in American English is without an “e”

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