Verification of Analog & Mixed Signal Ips Using Sv-Uvm Methodology

Subhranshu Shekhar Padhee , Anil Arora

Abstract: ***UVM Based methodology (UVM) is one of the broadly utilized check system to upgrade the confirmation nature of Simple and Complex IPs Configuration so as to accelerate the check procedure. A check situation to confirm the usefulness of IP by utilizing Framework in System Verilog - UVM based methodology. Simulator used to check the Complex IPs was Cadence Incisive. With the proper test plan and verification plan verification of IPs became easier. Analog and mixed signal IP structure are among the fastest developing need and market demand. Most frameworks on-chip (SoC) plans today are complex and mixed signal .The main goal of this project is to Verify the Functionality of Analog IPs like LDOs and the Functional Coverage.***

Keywords: Universal Verification Methodology, LDOs, Self-Checking Test bench.

I. INTRODUCTION

Low dropout controllers (LDOs) are a direct modest way to deal with control a yield voltage that is filled from a higher voltage input. They are definitely not hard to structure with and use. For most applications, the parameters in a LDO datasheet are commonly astoundingly clear and direct. In any case, extraordinary applications require the designer to break down the datasheet even more close choose if the LDO is sensible for the specific circuit conditions. datasheets can't give all parameters under all possible working conditions. To the organizer must interpret and extrapolate the available information to choose the execution under non-showed conditions. LDOs is one of the Simple IPs in which dropout voltage is the base voltage required across the regulator to look after guideline. A 3.3V required regulation at the output with 1 V of dropout at the input voltage of at least 4.3 V. Functionality of the LDOs are checked using UVM Methodology by Cadence Incisive and Synopsys VCS .

II. OVERVIEW

All the Functional Features have been checked using System-Verilog and Universal Verification Methodology(UVM). The simulation and the Coverage evaluation of the IPs are done using Cadence Incisive and Synopsys VCS. The Checking Methodology has been done by Self-checking Test-Bench. We have evaluated the Coverage by Incisive Metrics center. Our main objective is to come up with a reusability of Test-Bench written in UVM Methodology. So the proposed methodology has Less complexity, High Functional Coverage, Less time Consuming.

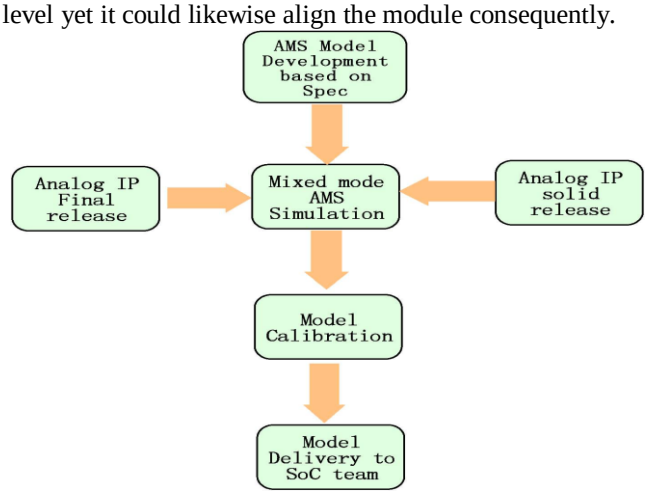
Revised Manuscript Received on May 10, 2019

Subhranshu Shekhar Padhee pursuing bvvbvn M. Tech Degree in VLSI Design stream Thapar Institute of Engineering and echnology,P Technology, Patiala

Dr.Anil Arora Assistant Professor at Thapar Institute of Engineering and Technology,Patiala.

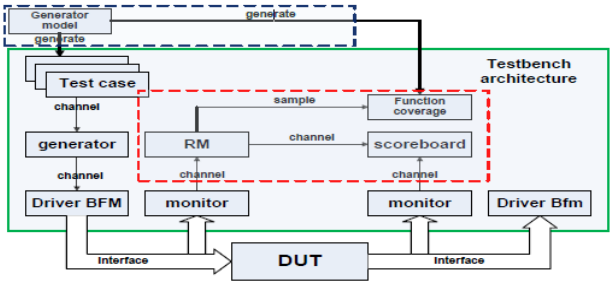
III. LITERATURE SURVEY

An integrated test bench is presented which proved unable just confirm the Analog and Mixed Signal IP at subsystem level yet it could likewise align the module consequently.



Fig[1]

Fig. 1. In the SOC level or then again subsystem level Complex IP Check Flow.The basic Analog IP confirmation was done right off the underlying complex Model. The Analog IP recreation was done with advanced Register Transfer Logic and basic transistor level netlist after straightforward structure solid release. By then Analog IP show arrangement were done by the comparable testbench to support the great model movement to the Analog IP setup gathering.



Fig[2]

At present, the nonexclusive test situate is expected to a different leveled building, it contains three guideline levels, to be explicit Driver ,generator and the testplan portion. As is showed up in The Fig2 exhibits that reference model and scoreboard may reuse in different endeavors or particular test arranges in a comparable endeavor. In case the interface indications of DUT are the standard shows, the screen and expert can be reused, for instance the VIP got from EDA merchants.

Above Figure generally discusses trials and incorporation show reused in the standard shows and conventional down to earth circuits.

FUNCTIONALITY OF LDO

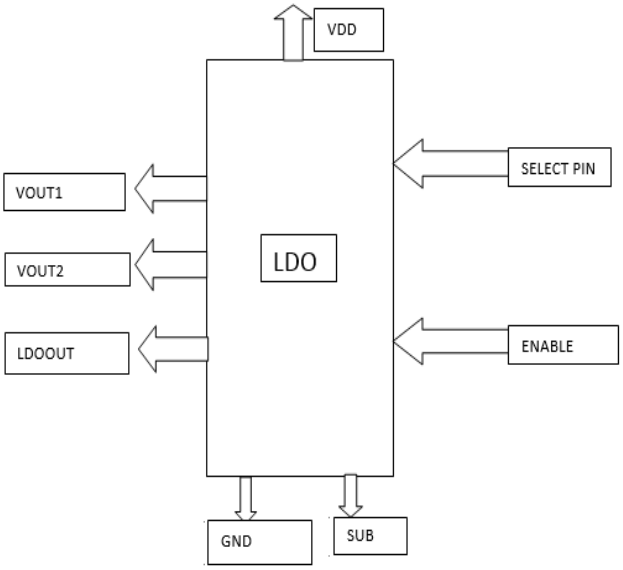


Fig [3]

Operation of LDO depends on the status of supply pins, ENABLE and SELECT pin. Logic High stands for 'H', Logic LOW stands for 'L' and Invalid stands for 'X'. With Valid supply and valid Enable signal LDO outputs are active after 80us .80us is called as startup time of LDO.

VDD	GND	SUB	ENABLE	SELECTPIN	VOUT1	VOUT2	LDOOUT
H	L	L	L	L/H	X	X	X
H	L	L	H	L	H(3.3V)	H	H
H	L	L	H	H	H(3.8V)	H	H
L	L	L	H	H/L	X	X	X

IV. RESULT

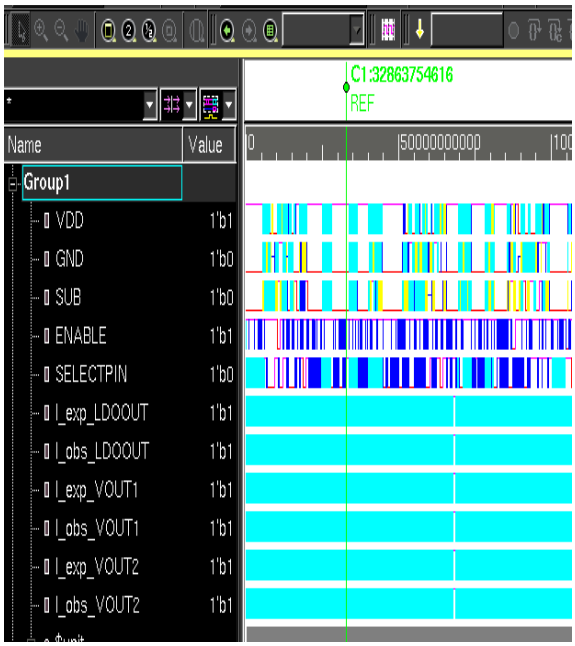
MODULE NAME	Code Coverage	Functional Coverage	Cross Coverage
LDO	96%	98%	90%

SIMULATION RESULTS

Simulation Result of Incisive Tool.

Fig[4]

Simulation Result of VCS Tool.



Fig[5]

V. CONCLUSION

The simulation results clearly reveal that by SV-UVM Methodology verified the functionality of LDO successfully. Functional as well as code coverage also achieved high. Expected and Observed value of DUT are matched. Next our future plan to used assertion based verification to reduce the effort for IP Verification.

REFERENCES

1. Chao Liang.Zhou Fang.C.-Z.Chen,"Method for analog-mixed signal design verification and model calibration Chao Liang ", China Semiconductor Technology International Conference Year: 2015.
2. C. Liang, "Mixed-Signal Verification Methods for Multi-Power Mixed-Signal System-on-Chip (SoC) Design", IEEE 10th Int. Conf. on ASIC (ASICON, Oct.28-31, Shenzhen, China), 2013.

3. CS/CoE1541: Intro. to Computer Architecture, Sangyeun Cho "Computer Science Department,University of Pittsburgh.
4. Lingling Chai .Zheng Xie . Xin'an Wang, "A verification methodology for reusable test cases and coverage based on system Verilog" IEEE International Conference on Electron Devices and Solid-State Circuits 2014.

AUTHORS PROFIL

Subhranshu Shekhar Padhee is pursuing bvvbvn M.Tech Degree in VLSI Design stream a t Thapar Institute of Engineering and echnology,P Technology,Patiala and working as an intern in STmicroelectronics,Greater-Noida in TDP team(Technology Designing Platform) . He has done projects on Functional Verification of Analog and Mixed Signal IPs. The author has completed his B.Tech in Electronics and Communications from Biju Patnaik University of Technology Odisha. Area of interest of the author is Low power, Digital IC design . Currently he is doing his master thesis under guidance of his mentor and co-author Dr Anil Arora in Functional Verification Of Analog and Mixed signal IPs.

Dr.Anil Arora is an Assistant Professor at Thapar Institute of Engineering and Technology,Patiala.He is currently working toward his research in the field of Micro-Electro-Mechanical Systems (MEMS) Design and fabrication.