FPGA Based Coin Recognition System

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Abstract*: Coins are most widely used in regular day to day existence at different places like in banks, markets, general stores, weight machines, vending machines, and hundis in temples. People used to count the coins manually before the arrival of coin recognizing and counting systems. It takes a lot of time and may lead to errors. So, it is necessary to develop automatic coin recognition and counting systems. These systems are already available in other countries. Unlike other countries, it is difficult to detect coins in India due to variability in the coin features for same denomination. In this paper, an FPGA (Field Programmable Gate Array) based coin processing is done along with recognition and counting. OV7670 camera is interfaced with Basys 3 FPGA. A HDL code is developed for interfacing camera. The advantage of FPGA is that it provides high processing performance, flexibility and low development cost. Due to reconfigurable feature of FPGA, high resolution cameras like 2MP, 5MP can be interfaced to detect the objects with high resolution.

***Index Terms*: Coin, FPGA, Image processing, Verilog HDL.**

I. INTRODUCTION

Different denominations of Indian coins currently existing are ₹ 1, ₹ 2, ₹ 5, and ₹ 10. Humans have the capability to detect and identify different coins irrespective of their shape, orientation and size. But humans cannot count huge amount of coins manually which takes a lot of time and also many errors. So, there is a need to design a system which will automate this process. There are different systems available for the recognition of coins like Mechanical Systems, Electromagnetic Systems and Image processing Systems [1].

In mechanical systems, recognition of coins is done on the basis of physical parameters like radius, weight, thickness, etc. But this type of systems cannot differentiate between original and fake coins as only physical properties are considered. Also it cannot detect different materials of coins. So, this system is efficient.

In electromagnetic systems, coins are differentiated based on the different materials used. Here the coins are allowed to pass through an oscillating coil at certain frequency range so that different materials provide different changes in their amplitudes and frequencies. Along with these changes, parameters like radius, weight, thickness, etc are also used to differentiate the coins. So, this method is better than mechanical system.

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In image processing systems, the image of the coin is taken and different algorithms are applied on it to detect the unique features of the coins that are required for the recognition. Image processing is the best method to recognize coins. There are also methods to recognize coin based on the character on it [2]. Generally MATLAB is the tool used for the image processing. But MATLAB needs a dedicated computer for the simulation. This problem can be solved by using the hardware design which is portable. Hardware design can be implemented using various technologies like Application Specific Integrated Circuits (ASIC), Digital Signal Processor (DSP), Application Specific Standard Products (ASSP) and Field Programmable Gate Arrays (FPGA). Out of these technologies, FPGAs is the best solution as they offer better performance, less time consuming, reconfigurable, flexibility and low development costs.

II. RELATED WORK

Suchika malik, Parveen Bajaj, Mukhwinder Kaur [3] proposed a method which uses unequally spaced Fourier Transform algorithm to detect the presence of coin and neural network, rotation invariance is used for the recognition of coins. The performance of the method is measured based on the parameters like signal to noise ratio, mean square error. There is a need to improve the accuracy and speed of the system.

Keyur D. Joshi, Vedang D. Chauhan, and Brian W. Surgenor [4] proposed a method to classify and count the currency coins with high speed and accuracy using Machine Level Inspection (MVI). A camera based system is used for the on-line classification of moving coins. As the coins are moving on the conveyor, speed of the target i.e. number of coins per min is calculated. Next the presence of coin is detected and recognized. Current system counts only 30 coins per min with the efficiency of 89%. It can be further improved to count 1000 coins per min with the efficiency of 99.9%. Rathod Prahaladsinh Kanubha, Y.J.Parmar [5] proposed an easy method to recognize the coin and separate based on the features of the image. In this paper, the RGB image is converted to black & white image and area of each region is identified and recognized. Recognition time is very low but it recognizes particular coins only and fake coins are also detected which gives wrong result. Accuracy can be further improved to detect more number of coins.

Dhanabal.R, Sarat kumar Sahoo, Bharathi V [6] proposed a method for detection and counting of coins using FPGA. To avoid the difficulty of using MATLAB, FPGA based detection is implemented here. Initially the image pixel values are stored in the block memory of FPGA. Then image enhancement techniques like manipulating brightness, operating threshold, contrast stretching are applied for the detection of circles and counting the number of circles. This is done by using the hardware description language, verilog. Later the result is verified using MATLAB for correctness. The parameters like power, cost, voltage and storage is compared for different FPGA boards. Sonali A Mahajan, Chitra M. Gaikwad [7] detected the face value of the Indian coins by comparing with the predefined data set. Two sides of the coin image is captured and image is compared with the data set based on the radius of the coin. Rotation invariance technique is applied to detect the rotated coins. This method is easy, faster and provides good accuracy. It will not detect the fake coin. Zhao Wenge, He Huiming [8] interfaced the hardware and software system. A FPGA based image processing system which includes acquiring the image, storing the image, processing and real-time display. In this system there three main steps involved, conversion, mapping, Layout and routing. By FPGA design flow we can achieve high speed, low power consumption and efficient circuits. Ching-His Lu, Hong-yang Hsu, Lei Wang [9] proposed a method by enhancing the contrast of the image which is achieved by Histogram Equalization. Proposed a new method, AIVHE (Adaptively Increasing the value of Histogram) where original Probability Density Function (PDF) divided into upper and lower blocks so it can automatically adjust the contrast enhancement to enhance image quality. This function is simple and easy to implement on hardware. Duanjinghong, Deng Yaling, Liang Kun [10] presented image processing system on DSP uses image processing unit and FPGA uses image sampling logic unit. For hardware configuration CCD camera is used to capturing the data and DSP board is used for processing those captured images. Image data is divided into frames and stored in 4:2:2 format order. These systems have capability of high speed processing and flexibility for implementing all real time applications. Janarbek Matai, Ali Irturk and Ryan Kastner [11] presented a real time system for face recognition on a Virtex-5 FPGA by taking video input from camera. Viola-Jones algorithm is used for face detection and Eigenface algorithm for face recognition. The system runs at 45 frames per second on FPGA.

Vanderlei Bonato, Eduardo Marques, and George A. Constantinides [12] proposed parallel hardware architecture for the detection of features in an image using the scale invariant feature algorithm. It takes the input from the CMOS image sensor and output is obtained from the FPGA.

Alareqi Mohammed, Elgouri Rachid, Hlou Laamari [13] and Neha.P.Raut1, Prof.A.V.Gokhale2 [14] presented the concept of using Xilinx System Generator for hardware software co-simulation in the image processing applications.

R. Harinarayan, R. Pannerselvam, M. Mubarak Ali, and D. Kumar Tripathi [15] presented the FPGA based edge detection for Sobel and Prewitt operators.

III. METHODOLOGY

In this paper, recognition of coins is done for two types of input images. In the first type, image coefficients are stored in the block memory of FPGA using MATLAB and other is image captured from camera.

The pre defined image of the coin is directly given as input in general image recognition. The simulations are done in MATLAB, Xilinx Vivado and also on FPGA using ChipScope Pro logic analyzer.

Two approaches are used for the recognition of coins in MATLAB. One method is area based and the other method is correlation.

1. Area based recognition

Most of the coins have different physical parameters like radius, area, shape, etc. By taking this advantage, area of the coins in the image is calculated and recognized.

Steps followed in matlab are

- Read an RGB coin image.
- Convert that coin image to gray image.
- Convert gray scale image to binary image by setting a threshold value.
- Use image filling to reduce the noise so that we get circular regions in the places of coin.
- Find area, centroid of each circular region in the binary image.
- Based on the area of coins, recognize them.

2. Unique feature based recognition

Each coin consists of a unique feature, those features are identified and stored as the data set. When a coin is given as input, it is compared with the images in the data set using correlation.

Steps followed are

- Read the RGB coin image.
- Convert that coin image to gray image.
- Read images from the data set one by one and compared it with the input image using correlation.

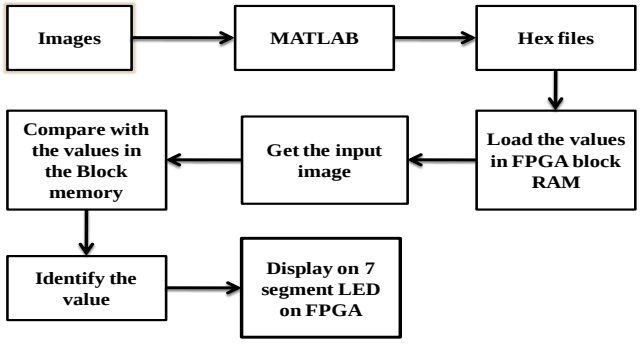

Fig. 1 Block Diagram for FPGA Implementation

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The block diagram for this type of recognition is shown in the fig. 1. MATLAB tool is used to convert the coin images into their coefficients. These coefficients generated are loaded in the block memory of FPGA. When the input image is given, the coefficients of the input image are compared with the coefficients of the images in the block memory and if the value matches then the corresponding coin value is displayed on 7-segment LED on FPGA.

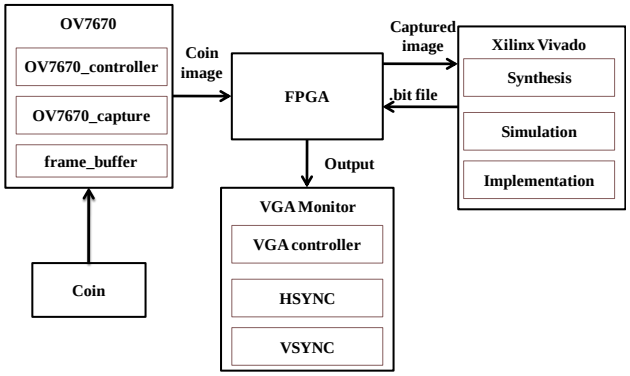

Fig. 2 Block Diagram of Camera based Recognition

In the previous methods, the image is converted to hex file using MATLAB and those files are given as input to the Xilinx. In this method, the image is captured from OV7670 camera as shown in fig. 2. The data from the camera to FPGA is observed using ChipScope pro logic analyzer. The unique hex data values obtained for the each coin are stored in the block memory of FPGA. When the coin is placed in front of camera and, real-time hex values are obtained. If those values matches with the stored data in block memory of FPGA then based on the resulting currency value, LEDs are made to glow on FPGA.

IV. FPGA

It consists of configurable logic blocks and programmable interconnects so that it can be used for different applications based on the given specification. There are different types of FPGA development boards available like Basys, Nexys, Zedboard, etc. In this paper Basys 3 board is used.

Basys 3 is a ready-to-use development platform which is based on the Artix-7 FPGA from Xilinx. Basys 3 FPGA utilizes Xilinx Vivado FPGA Design Tools which is not possible with Basys 2.

In Basys 3 board, there are about 33,280 Logic Cells in 5200 slices, Block RAM is of 1,800 Kbits, DSP Slices of 90 and internal clock is 450 MHz+.

Table I Features of Basys 3

Pmod Connectors	3
Switches	16
Buttons	5
User LED	16
7-Seg Display	4-Digit
VGA	12-bit
USB	HID (KB/Mouse/Mass Storage) Electrical Power
Logic Level	3.3v
Physical	Width 2.8 in Length 4.8 in

V. OV7670

It is a small size, single chip and low voltage CMOS based image sensor which can be used in FPGA, Arduino, ARM, DSP, etc. This module requires 3.3V power and external clock source to power up. It uses SCCB (Serial Camera Control Bus) for the processing. The resolution of camera module is 640×480 VGA, pixel size is 3.6µm x 3.6µm and the output format is 8 bit i.e. 4:2:2 RGB data.

VI. RESULTS & DISCUSSION

Fig. 3 to fig. 7 represents the recognition of coin in MATLAB. Variation in area for different coins is taken as a parameter to recognize coins in fig. 3 and in fig. 4 to fig. 7, coins are differentiated on the basis of unique feature present in each coin.

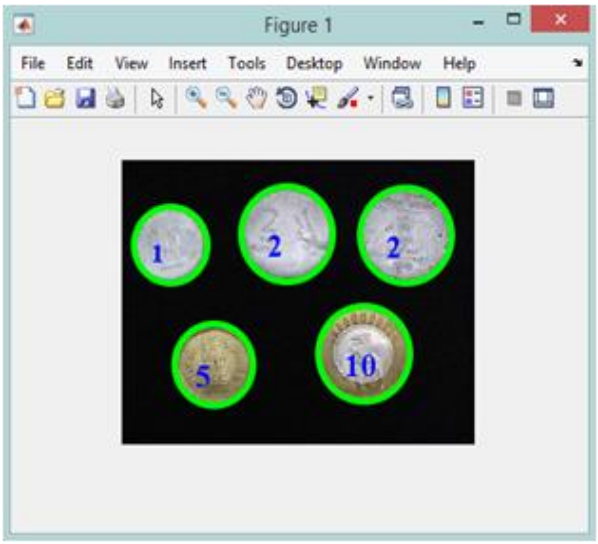

Fig. 3 Area Based Recognition

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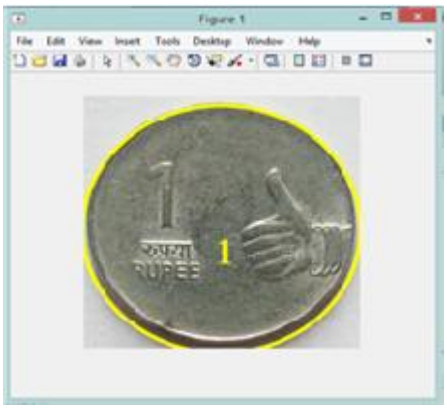

Fig. 4 One Rupee Coin Recognition

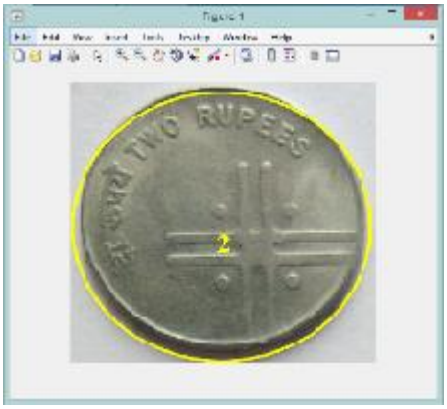

Fig. 5 Two Rupee Coin Recognition

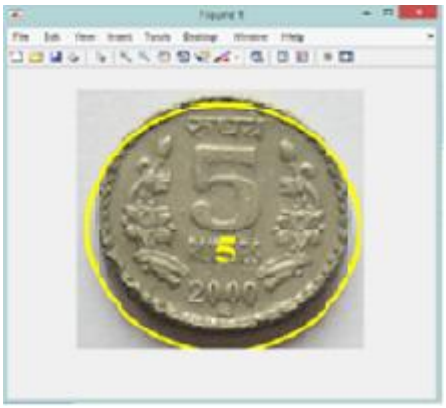

Fig. 6 Five Rupee Coin Recognition

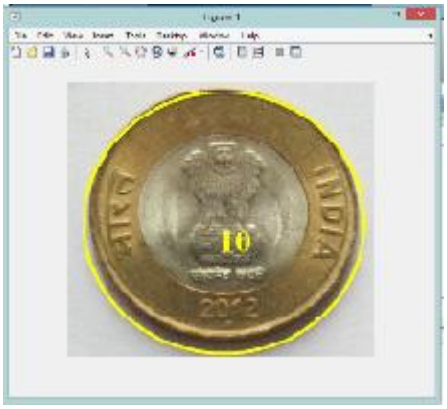

Fig. 7 Ten Rupee Coin Recognition

Fig. 8 to 10 represents the recognition of coin which are obtained by comparing the each pixel values of the input image i.e. the image which is located in the center is compared with the images that are located in the corners of the image. If it matches then the result is shown on the 7-segment LED on FPGA board.

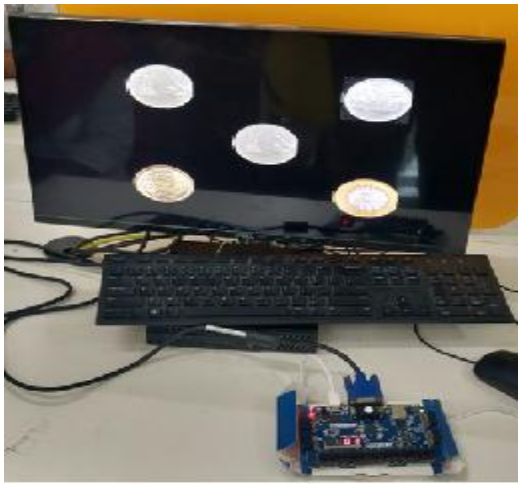

Fig. 8 One Rupee Coin Recognition on FPGA

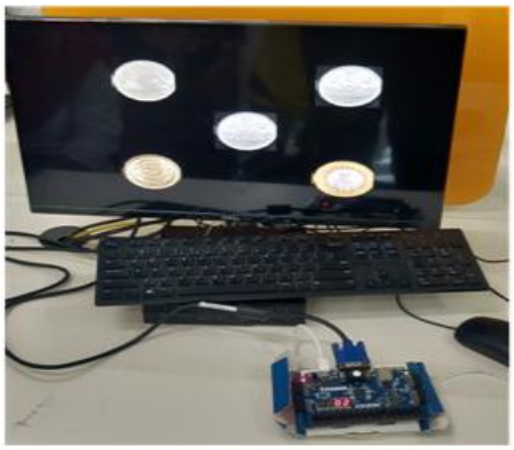

Fig. 9 Two Rupee Coin Recognition on FPGA

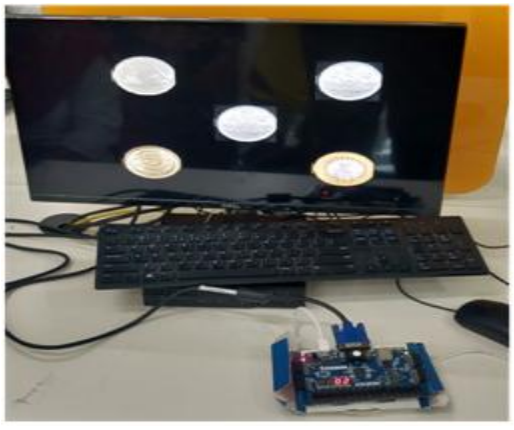

Fig. 10 Ten Rupee Coin Recognition on FPGA

The image is obtained here by interfacing Basys 3 board to the camera OV7670. Fig. 11 shows the interfacing of Basys 3 board to the OV7670 camera. When the coin is place in front of camera, image will be displayed on the monitor is shown in figures 12 to 14.

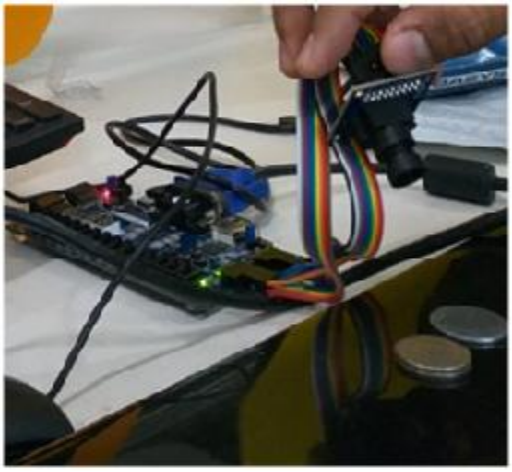

Fig. 11 Interfacing OV7670 with Basys3

Fig. 12 Two Rupee Coin Processed by Basys3

Fig. 13 Five Rupee Coin Processed by Basys3

Fig. 14 Ten rupee Coin Processed by Basys 3

Fig. 15 indicates the simulation in the ChipScope pro obtained after placing the coin in front of camera as shown in the fig. 16, one LED became on after placing one rupee coin in front of it. The information about the utilization of FPGA is shown in table II. The RTL schematic is shown in fig. 17.

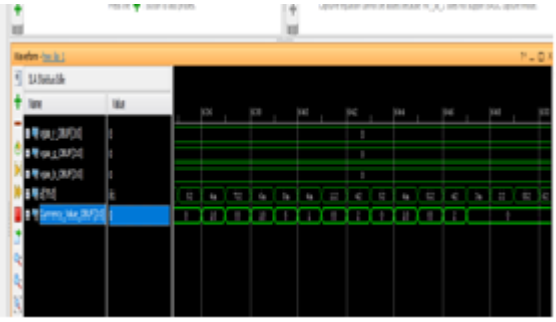

Fig. 15 ChipScope Pro Simulation after Placing Coins

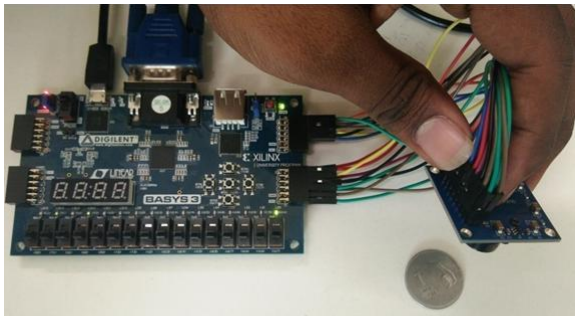

Fig. 16 One Rupee Coin Recognition in Real-time

Table II Device Utilization Summary

Utilization | Post-Synthesis | Post-Implementation

Graph | Table

Resource	Utilization	Available	Utilization...
LUT	1437	20800	6.91
LUTRAM	117	9600	1.22
FF	2071	41600	4.98
BRAM	28	50	56.00
IO	39	106	36.79
BUFG	5	32	15.63
MMCM	1	5	20.00

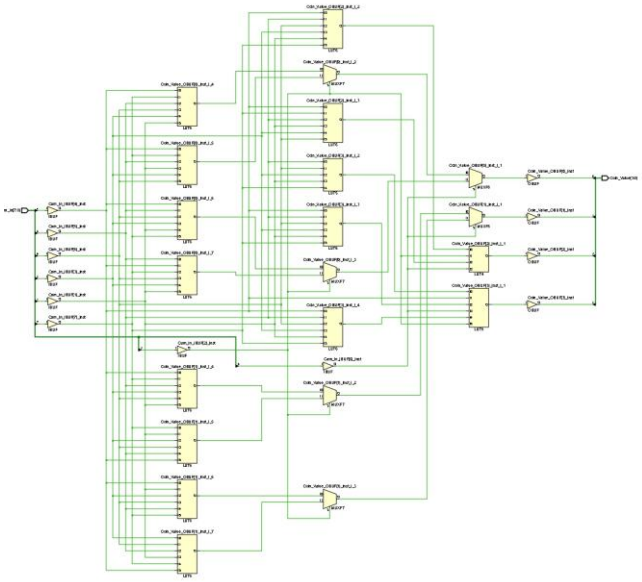

Fig. 17 RTL Schematic

VII. CONCLUSION

The hardware based coin recognition system is proposed and implemented on FPGA using verilog HDL. Software simulations are done in MATLAB tool. In real time, coin is recognised by interfacing OV7670 camera with Basys 3 FPGA board and real-time hex values of the coin which is captured from camera are obtained using ChipScope Pro logic analyzer. When the coin is placed in front of camera and if the resulted pixel values matches with the stored data in block memory of FPGA then outputs are displayed on LEDs. The disadvantage with the static mode is that the block memory of the Basys 3 board is low, only some images can be stored and identified. When camera is interfaced, variations in light intensity, position, distance of the camera may lead to errors. Further research can be done to improve the speed and accuracy of the system by interfacing high resolution cameras, using high end FPGAs and also using deep learning.

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