Design and Implementation of Reduced DC-link Capacitance using Voltage Compensation Technique for a Solar PV Module

K.Usha, S.Manasa, R.Priyadharshini

Abstract*: *The bulkiness of the DC link capacitor is a very critical matter of concern, in the solar power harnessing circuit. An alternative method to reduce this bulk capacitor is necessary to reduce the overall cost of the system and the ripple content in the circuit, without affecting the overall efficiency of the system. In this paper, a methodology is proposed in which a voltage compensator is integrated with the DC bus line to accomplish the reduction in the DC link capacitance for a solar PV module.

Index Terms*: *DC Link Capacitor, Voltage Compensator, Capacitor Reduction.

I. INTRODUCTION

In the past few decades, the conventional energy sources are facing the major problem of incremental depletion. The renewable resources are used in the recent years due to its several advantages like high sustainability, long lasting, less maintenance, etc. Photovoltaic which is a rapidly growing and increasingly utilized renewable resource is used as an input source to the system. Maximum Power Point Tracking (MPPT) algorithm is employed to maximize the efficiency of the PV module [1]. A typical power conversion system consists of two power converters. The first converter is used to convert the variable input dc voltage from the PV panel to fixed dc voltage. The second converter circuit acts as an inverter to convert the fixed dc voltage to ac voltage which is supplied to the load. In between these two stages DC-link capacitor is used to reduce the power fluctuations between the synthesized power and load demand .The harmonics get filtered and voltage variation in the DC link are reduced. The presence of higher order harmonics may also damage the operation of MPPT controller adversely affecting the maximum power delivered to the grid. Electrolytic capacitors are generally utilized for this purpose due to its high energy storing capability at reasonable cost. However, the electrolytic capacitors are bulky and less reliable which results in large Total Harmonic Distortion (THD) of the input source current [2]. Thus, efforts have been taken to reduce the size of the electrolytic capacitor by introducing a series voltage compensation technique which improves the system stability and controlled voltage regulation is achieved. The requirement of an additional switch to eliminate the ripple current is absent. However, a diode bridge converter scheme cannot be accomplished as they suffer switching losses. A relationship in the operating frequencies between the first stage and the second stage is obtained in [3]. An active component connected in parallel to the DC link to compensate for the ripple is adopted by [4]-[6]. In [4], the ripple conduction circuit is implemented by a full-bridge topology. Here the disadvantages are the high inductor current stress and the high switching frequency requirement which makes the ripple conduction circuit difficult to be applied in practice. In [5], a current injection method by a half-bridge structure is used. A bidirectional converter that employs buck and boost action in a full-bridge topology applied when the load demands a DC current proposed in [6]. In all the above solutions, the active and passive elements of the circuit are exposed to high voltages in the circuit causing di-electric stress during switching action. The presence of fluctuations between the power from the panel and the grid , is suppressed by the inclusion of an additional port consisting of active elements that absorb the power difference as proposed in [7]. In [8], the ripple cancellation or reduction takes place in the DC link by connecting an inductor in addition with the capacitor. It is presumed that the capacitance is of infinite value and the ratio of the inductance in a transformer isolated circuit being 1:1. The drawback of this configuration is the large size of the inductive elements that add to the bulkiness of the circuit.

II. SYSTEM METHODOLOGY

Figure 1 illustrates the typical structure power harnessing circuit for PV standalone applications, motor drives, and grid connected power harnessing circuit. The two power stages in the system are the converters and the inverter circuit. The solar PV output which is in a partially DC form is converted into a fixed DC output. The boost converters are predominantly used in this stage as the grid voltages are normally greater in magnitude than the harnessed power voltage. The DC voltage is then fed to the inverter at the second power stage. The DC-link capacitors are connected between the two power converters. The link capacitor absorbs the momentary power deviations from the load to the MPPT circuit.

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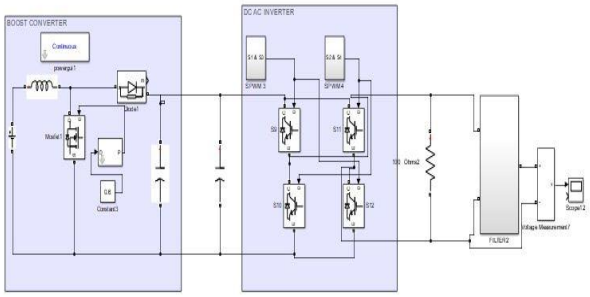

Figure 1: Block diagram of the two stage power converter system

The link capacitors help in filtering the harmonics, and provide sufficient energy during the hold-up time of the entire system. The system operates such that the energy supplied by the solar panel is completely sufficient to supply to the load. In this condition, the energy from the panel is fed to the filter capacitor that filters out the ripples from the source. Inverter will convert the obtained dc from the capacitor to ac that feeds the load.The MPPT algorithm is used to obtain the maximum power from the panel. The pulses required by the converter and the inverters are given by the driver circuits. The driver circuits are controlled by the signals from the ARDUINO UNO microcontroller. The microcontroller monitors the feedback signals, and appropriately gives pulse signals to the MOSFETS in the driver circuit. The outputs of the ARDUINO are 3.3 volts and 5 volts respectively.

III. DESIGN

Figure 2 shows the system which consists of two power conversion stages with series compensation. The voltage compensator generates an AC voltage that counteracts the ripple voltage on the output of the boost converter. Thus, the input of the inverter is a DC voltage equal to the average value of the voltage V_{dc} across the DC-link capacitor C_{dc}. The DC-link voltage V_{dc} and the input voltage of the voltage compensator V_a are sensed.

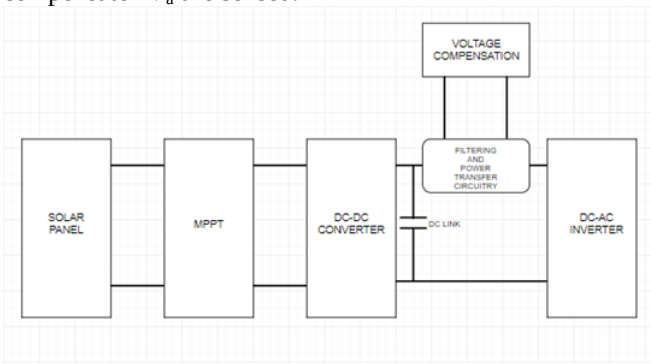

Figure 2: Block diagram of the voltage series compensator network for a solar PV module

The Thyristor controlled voltage source is connected in series with the DC link capacitance. A compensator generates a voltage corresponding to the ripple present at the output side of the first stage of the converter. The main principle is to connect a voltage source that gets added to the converter output stage before feeding into the inverter, controlled by a PI controller depending on the voltage fluctuation in DC Link side. Since the high frequency voltage ripples could be filtered out using a filter circuit, only the low frequency voltage ripple degrade the MPPT operation. The addition of a compensator reduces the ripples being processed by the link capacitance , implying the reduction in the required minimum value of DC link capacitance. The triggering circuit represented in Figure 3, extracts the ripple from the boost converter circuit. The obtained ripple is stabilized with a PI controller. The PWM circuit is used to switch the Thyristor circuits in sequence with the ripple detected. The replacement of lower values of capacitance from electrolytic capacitors is possible with the reduction of high frequency oscillations at the output stage of the converter level. The quality of current at the inverter to grid integration is reduced due to fluctuating current at the input end, so that suitable control techniques must be adopted to reduce such an effect.

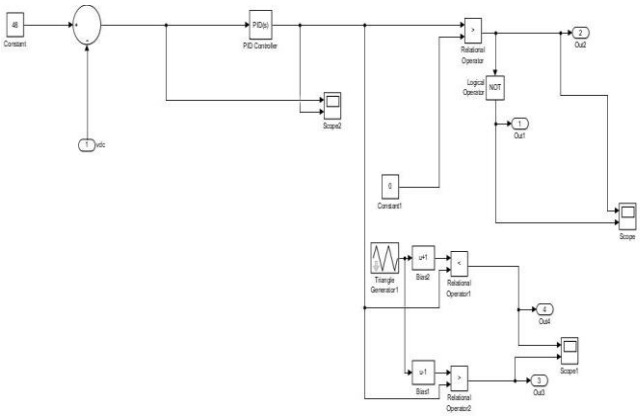

Figure 3: Triggering circuit that extracts the ripple from the boost converter circuit.

The solar panel produces the necessary power to the load. The solar power produces the output power of 100 W, with the maximum operating voltage V_{mp} corresponds to16.9 V and the maximum current I_{mp} of 5.91 A. The open circuit voltage of the solar panel V_{oc} is 21.2 V and the short circuit current I_{sc} is 6.33 A. The assumed output voltage of the panel V_{out} is 20 V. The output from the solar panel is given to the variable DC converter. The maximum output from the panel is obtained using the perturb and observe (P&O) algorithm. The input given to the converter Vin is 20V, acts in the boost mode to provide an output upto 60 V. The output voltage of the converter is

$$V_{out} = \frac{1}{1-d} V_{in} \quad (1)$$

Where d = the duty cycle of the input pulse given to the MOSFETS. From equation (1), the duty cycle of the pulses fed to the converter is, d = 0.6, for optimal operation to reduce the switching losses.

The inductance used in converter is

$$L = \frac{(1-d)^2 \Delta R}{2f} \quad (2)$$

The determined value of the inductor is 960µH.

The value of capacitance used in the boost converter is

$$C_{min} = \frac{d\, V_o}{V_r\, R\, f} \quad (3)$$

The minimum value of capacitance used is $1.2\,\mu F$ The maximum allowable ripple for the boosted DC voltage remains in the range of 2.5-5% for maximum efficiency. In order to achieve the increased operational efficiency, a voltage compensation source is connected in series with the capacitor.

The DC link capacitance associated with the intermediate stage between converter and inverter is C $= \frac{I\,t}{\Delta V}$ (4)

Fixing the voltage ripple to the minimal value, the required DC link capacitance is $100\mu F$. After boosting the input voltage in DC converter to 60V, the current through the link capacitance corresponds to 1A. The link capacitance feeds the inverter. The single-phase inverter with the Pulse Width Modulator supplies with the signals for the MOSFETS to enhance conduction.

The pulse width modulator of sine wave frequency, f_m= 50 Hz and the corresponding triangular wave frequency, f_{tr} = 500 Hz. The modulating index of the inverter is

$M_f = \frac{f_{tr}}{f_m}$ (5)

The modulating index used to drive the inverter is 12.The voltage compensation is connected in series to the bulk capacitor branch. The DC ripples operated by the capacitor decreases in the magnitude and effectively reduces the DC bus Capacitance given by

$C_{dc} = \frac{m_a{}^2 I_D}{\omega_1\, 2\, |\Delta V|}$ (6)

Where I_D is the dc component of Current flowing through the output side of the dc-link capacitor/module bus line and ω_1 frequency of Current flowing through the input side of the dc-link capacitor/module bus line [9]. The compensator produces the equivalent sine wave, with respect to the ripple in the DC link. The compensation provides the external voltage to cancel off the low frequency ripples and decreases the rapid voltage fluctuation. Hence, the voltage fed into the inverter contains steady state voltage and the power transfer in the system is increased. With the value of modulating index of the compensator equal to 9, the value of the DC link capacitance is $40\mu F$.

IV. SIMULATION RESULTS

Without Compensation circuit, the boost converter output is increased to 60V which contains ripple of 16.8V, peak to peak with a link capacitance of 40 μF. Figure 4 shows the solar PV module with the compensator connected in series. The ripple is reduced to 2.2V, (p-p) with the inclusion of the compensator circuit. The voltage compensator generates a 12V (p-p) value as illustrated in Figure 5. The decrease in the ripple in the link capacitance for an output of 60V with and without compensation is shown in Figure 6. The ripple is efficiently removed without the use of any active component. The inverted output is fed to the grid as illustrated in Figure 7.

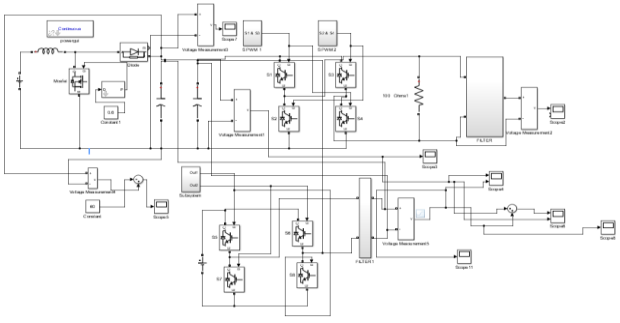

Figure 4: Circuit with the series voltage compensator.

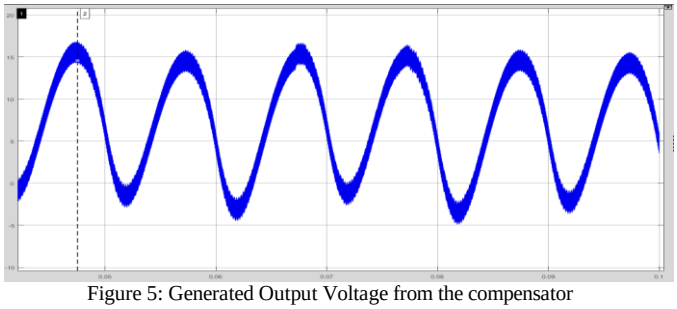

Figure 5: Generated Output Voltage from the compensator

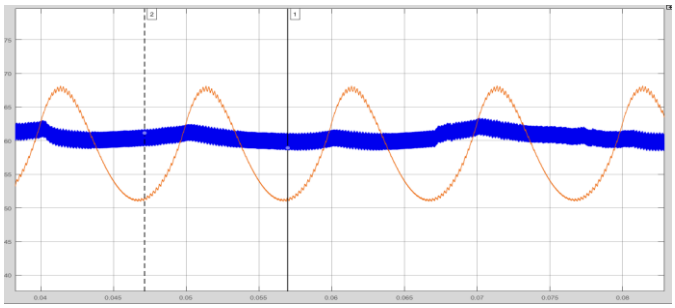

Figure 6: Comparison of Ripple in Output Voltage of Compensated and Uncompensated Circuit

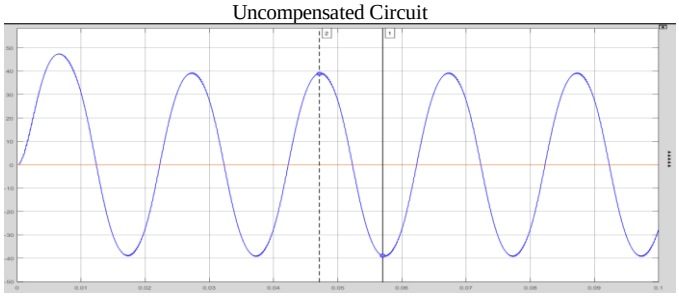

Figure 7: Inverter voltage fed to the grid.

V. HARDWARE IMPLEMENTATION

The prototype model of the simulated circuit with the compensator circuit is shown in Figure 8.The boost converter with series compensator circuit boosts the input voltage of 20V to an output voltage of voltage to 52 V. The solar panel output is emulated using a transformer from a fixed AC source and is rectified before supplying to the boost converter. The DC link capacitance of 47 µF is connected between the converter and the inverter stage. The ripple in the boosted voltage is with a magnitude of 2.9 V. The compensator feedback is compared with the momentary DC link capacitance voltage ripple and is programmed using Arduino ATMEGA. The boosted voltage is fed into the inverter circuit with a compensator connected in series with the DC link.Thus, the input voltage of the inverter is the addition of the voltage source and the voltage in the DC link capacitance. The inverter output AC is used for the power applications and its accuracy depends on the type of filter used in the circuit model.

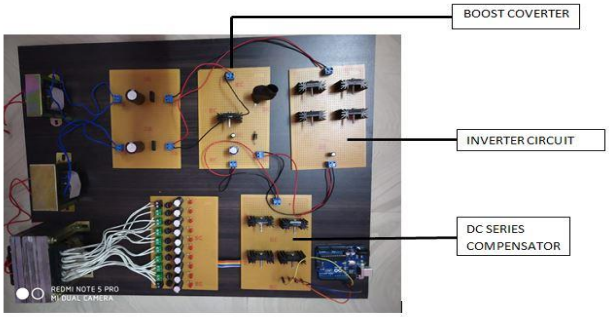

Figure 8. Experimental setup of the prototype circuit model

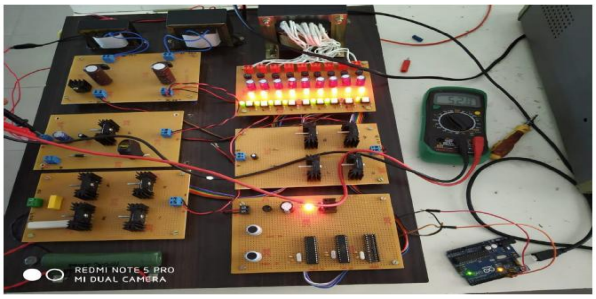

Figure 9. Compensated Output Voltage of the DC boost converter

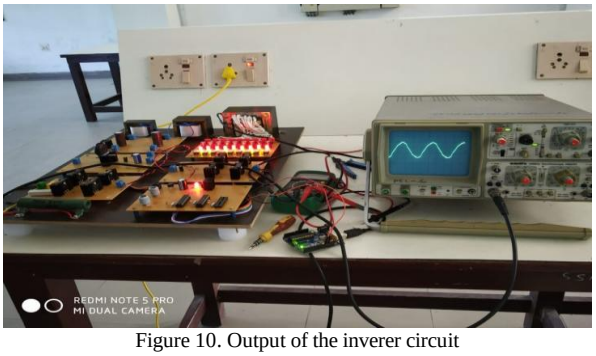

Figure 10. Output of the inverer circuit

The integration of voltage compensator decreases the ripple content from the 100 W solar PV panel is decreased from about 16.8 V to 2.2V. The Electrolytic capacitance of length 48 mm and diameter 18 mm (for 100μF) can easily be replaced with an electrolytic capacitance of 16mm diameter and 34mm length(for 40μF). A reduction of 19.04% of length in the capacitance and a 11% reduction in the diameter is observed. Though the electrolytic capacitor is cheaper, the high ESR and ESL values lead to increased losses and decrease in the lifetime of the capacitor. Hence, an alternative such as the ceramic capacitance of dimensions 0402(0.4mm x 0.2mm) or 0603(0.6mm x 0.3mm) and of value 10μF can also be used which produces better efficiency and performance.

VI. CONCLUSION

The reduction in the ripple current corresponds to the reduction of the value of the capacitance for a prototype circuit model with series compensator circuit. The reduction in the value of the capacitance allows the replacement of the commonly used electrolytic capacitors which has inferior characteristics like High ESR, limited lifetime, leakage currents, etc. with power film or ceramic capacitors which has better characteristics comparatively. The analysis is carried on the prototype experimental circuit setup which can be extended to higher voltage level where the proportional increase in reduction of the bulk DC capacitance is observed with increase in voltage level.

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