Design of PLL with VCO of 40MHz-1 4GHz Ultra low phase noise-120dBc/Hz very low RMS Jitter<180aS

N. Leela Krishna Sai, M. Parthasarathy, RayamSumanth, R. Saktivel

Abstract: ***This paper presents the design of Phase Locked Loop(PLL) with Voltage Controlled Oscillator(VCO) of 40Mhz—1.4GHz, ultra-low phase noise -120dBc/Hz, very low Root Mean Squared(RMS) Jitter <180aS by using 180-nm CMOS technology through Cadence Virtuoso Environment. In this paper, comparison between VCO designed with PMOS load ring VCO and Current starved VCO is shown. PMOS load ring VCO has an average power dissipation of 29.31 uW and with an oscillating frequency of 820 MHz. While Current Starved VCO has an average power dissipation of 20uW and with oscillating frequency of 1.17GHz. Phase Frequency divider(PFD) is made of resettable D–flipflops which uses a different structure rather than the conventional one with lower transistor count. PFD along with charge pump is used to reduce finite phase errors. Asynchronous frequency divider circuit is used with new structure of D-flipflop in which area and power dissipation reduces by 41.66% and 58.4%. The total average power dissipation and RMS Jitter of PLL with PMOS load ring VCO designed is 13.68 mW and 1.87as respectively and PLL with current starved VCO is 8.68mW and 31.24zs respectively. By varying control voltage of VCO from 0.4V to 1.6V, the tuning range from 28.2MHz-1.66GHz is attained.***

Index Terms: Current starved VCO, Frequency divider, Phase locked loop (PLL), Root Mean Square(RMS) Jitter, Voltage Controlled Oscillator (VCO).

I. INTRODUCTION

A. Background

A man's life constitutes a routine that he often sticks on to. The routines may not be the same always but each routine is synchronized with the previous versions of it and is sometimes better than them. It can be said to be an iterative process where some feedback lets him know and locks the phase of the routine undergoing with a looping structure. Such observations gave life to a similar system long back named as Phase Lock Loop (PLL). Used almost in all day-age applications, but raises the infamous question: is it necessary and why? After answering, a question arises again: is it to our requirement? Even though the system is doing above and beyond the necessary, in order to testify the general conceptions and for better performance, a system is eventually in place to fit around. "What major issues concern a design engineer?", the answer might probably lead back to three main concepts, Power, Area and Performance. Moving in depth, the common linkage to all the analog and digital components and circuits leads us to an important segment called the phase lock loop. It can be said that, on the whole, a phase lock loop is simply a system that controls the input reference signal given from the system and generates the output signal with the required phase with some relation to the input signal. It could be keeping the input and output signals in phase or out of phase even with some phase difference as desired.The approach to obtain the necessary specifications can be capsuled as: Generate a plan, implement the plan, pre-assume the plan does not work, and fix the plan via maintaining the pre-assumed not advisable outcome. It can be apprehended that the operation of PLL can be taken as a parallel to the approach discussed. Impelling further, the approach of a PLL can be bridged as: give an input signal, try to develop a lag-free free running signal at the output, expect the signal to behave odd, and feed the output back to the input to detect any changes and lock the phase for the output signal. 1673 was the year when the PLL phenomenon was observed between the automatic synchronizations of different coupled pendulums. This phenomenon was later developed into various fields and now it has become a very significant part while using clock in any circuit. A PLL is made up of blocks like a phase frequency detector, a loop filter, a charge pump, and a voltage control oscillator.

The techniques and methods employed in constructing the PLL is explained in section II, the method of analysis in section III, results obtained in section IV, discussion of those results in section V, Conclusion in section VI, future scope in section VII.

B. Objectives

- To design a PLL with very low RMS Jitter <180aS.
- PLL with an ultra-low phase noise- 120dBc/Hz.

II. TECHNIQUES AND METHODS EMPLOYED

Basically, in a PLL first block will be Phase frequency Detector. In that basic building block will be a D-flipflop with reset. Choosing the design of D-Flipflop will have great influence on area, power dissipation and propagation delay. Conventional D-flipflop is built by using 24 transistors.

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D-flipflop used here shown in the upcoming sections is having only 14 transistors which has a reduction of 41% in transistor count, so there is drastic improvement in area, speed and power [1]. So in PFD, two D-flipflops are used. So the transistor count is reduced to 28 from 48.Frequency divider block [2,3] is used in the feedback path of PLL. This divider block is designed using mentioned D-flipflop structure. Frequency divided by 2 network is used here. For the frequency divider by 8 circuit variation ofmentioned parameters are as follows in Table. 1:

Table. 1 Parameters of Frequency Divider circuit

Parameter	Frequency divider with conventional design	Frequency divider with proposed design	Reduction (%)
No. of transistors	72	42	41.66
Propagation delay(speed)	500uS	10uS	98.00
Power dissipation (Power)	216.94uW	90.24uW	58.40

One Q output of the D-Flip flop produces the fast output signal and the otheroutput d-flip flop produces the slow signal output. If a frequency of input signalDFF 1 is high and the frequency of DFF2 is low then there produces the highfrequency signal as output and if the frequency of DFF1 is low and frequency ofDFF2 is high then the DFF2 frequency state will be maintained. The first risingedge of DFF1 frequency will be maintained until the other goes for a rising edge.In literal terms, one produces positive current source and the other producesnegative current source. In general terms, phase detector has two input signals, one isfrom the reference signal and the other from the voltage controlled oscillator and itproduces the output signal is proportional to the phase difference of these twosignals. Lock range of PLL is that the frequency range at which the changein the input frequency. Phase noise is the ratio of noise in the offsetfrequency to the output frequency node.

If two input signals having the same frequency, but first signal leads the second one, then first output representing the first input continues to generates pulses which widths are proportional to the difference in the delay of two input signals. If also the frequency of first signal is more than the second one, increasing pulse widths are generated which will be shown in the upcoming sections.

Basically VCO is an electronic oscillator whose oscillation frequency is controlled by input voltage. VCO section is designed with one of the mentioned methods which is PMOS load ring VCO[4] of five inverter stages. It is basically behaving as two terminal device diode in lieu of P-typeMOSFET as the Drain and Gate terminals are shorted. Since for the N-MOSFET and P-MOSFET their respective source terminals are connected to Ground and VDD along with bulk, Body bias effect will not be considered. In the configuration of diode connected load, P-MOSFET provides resistance which acts as a resistor giving an advantage over manufacturing high cost resistance. Here PMOS load ring VCO has low power [4] dissipation of 29.31 uW.

Current starved VCO [5] is one type of VCO working on the basis of ring oscillator in addition with one CMOS which will be working as current source for the inverter. Normally ring oscillator comprises of delay stages in which output is feedback to the input of first delay stage. No. of delay stages for a ring oscillator to work is ODD number of delay stages. Here 5 inverter stages [6] are used. For a current starved VCO too, working principle is similar. From the schematic view of current starved VCO, middle MOSFETS M28, M21 act as inverter stage, whereas MOSFETS M30, M19 behaving as current sources. The work of those MOSFETS is to limit the current to its respective inverters, by which we can say that inverter is starved for current and hence the name. The drain currents of the MOSFETs M34, M40 will be same and they are set by input voltage. The current of those MOSFETS are mirrored in each of the current source stages (eventually to inverter stages). In the circuit upper P-MOSFETS are connected to the MOSFET M28 and so on, and all low N-MOSFETS are connected to the source voltage.

Performance analysis [7] is done for calculating phase noise and RMS jitter which are discussed in upcoming sections.

III. METHOD OF ANALYSIS

Phase and frequency detector block has two inputs. One is reference signal and other is feedback signal. Parameters of the Phase-Frequency Detector are tabulated in Table. 2. It detects the phase difference of the two inputs and this output is given as input to the charge pump circuit. This charge pump circuit integrates [4,8] the output current of charge pump into a suitable electro motive force signal which is given as input to the low pass filter that integrates the output current of charge pump into control voltage which is used to control VCO block that controls the frequency of oscillations. This current is copied to next stage through current mirror circuit. Output current is proportionate to input voltage.

The parameters of charge pump and PLL are tabulated in Table. 3. Performance analysis of PMOS load ring VCO is measured by performing analysis such as PSS, Phase noise analysis, average power and RMS jitter and calculated parameters have been covered in Table. 4. The frequency of oscillations is given by

$$f = \frac{1}{2*t*n} \quad (1)$$

Where ‘t’ represents the time-delay for a single inverter and ‘n’ represents number of inverters in the inverter chain.

For current starved VCO, by varying control voltage, its output oscillating frequency is measured. Control voltage is varied from 0.4V to 2V and its corresponding frequencies are tabulated in table.5. Graphical representation of control voltage vs frequency is shown in Fig. 6.

To obtain the frequency of oscillation equation:

$$Ctot = Cout + Cin \quad (2)$$

$$Ctot = Cox(WpLp + WnLn) + \frac{3}{2}Cox(WpLp + WnLn) \quad (3)$$

$$Ctot = \frac{5}{2}Cox(WpLp + WnLn) \quad (4)$$

$$Fosc = \frac{Id}{N*VDD*Ctot} \quad (5)$$

Where Id is drain current, N is total no. of inverter stages, Cox is oxide capacitance and Wp and Wn are width of PMOS and NMOS respectively and Lp and Ln are lengths of PMOS and NMOS respectively.

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Finally for total PLL circuit various parameters which are calculated from the outputs of PLL simulation and are tabulated in TABLE in V. We analyse the tuning range of the PLL circuit simulated via (t2-t1) where t2 is the time point where the cycle becomes stable and t1 is the time period at the same value of the voltage just one cycle behind. This gives us an estimate of our tuning range and to calculate it using the simulated waveform data and the offset frequency which is known to us using:

$$Tuning\ range = \frac{maximum\ frequency - minimum\ frequency}{offset\ frequency} \quad (6)$$

Locking range of PLL is defined at the tip where VCO output, frequency divider output and input are met at the same point from where the cycle behaves in sync with the next consecutive cycle. Lock range is also called as Track range. Basically it can be said as range of frequencies over which Phase Locked Loop system output follows the input frequency.Capture range is defined as the range of frequency which attains the phase lock.

IV. RESULTS

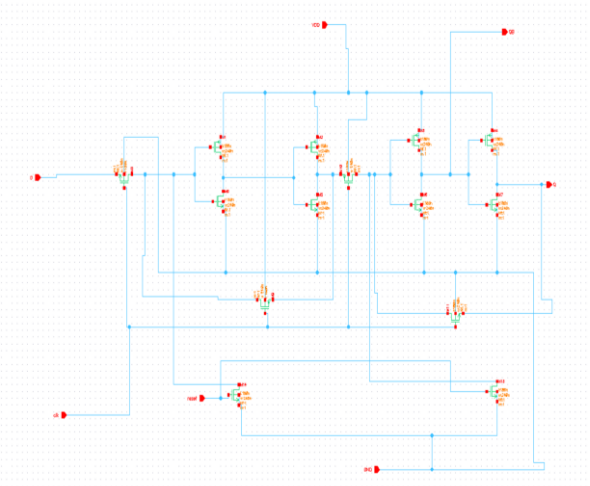

Fig. 1 Schematic New structured D-Flipflop

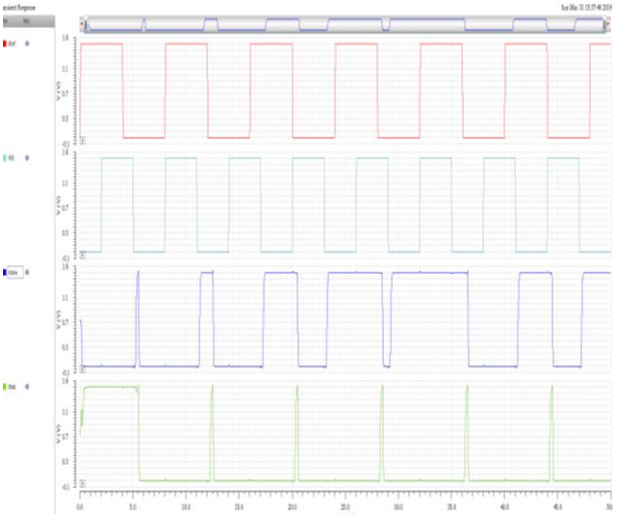

Fig. 2 Output of PFD

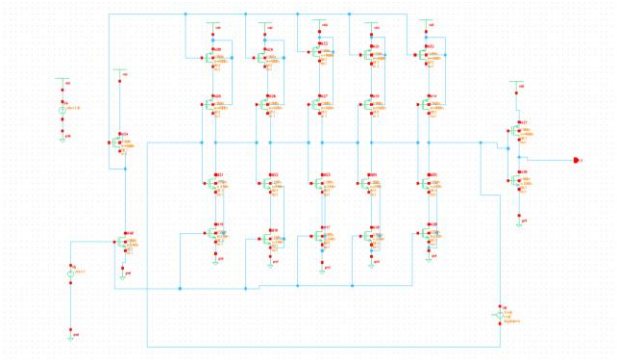

Fig. 3 Schematic of CSRVCO

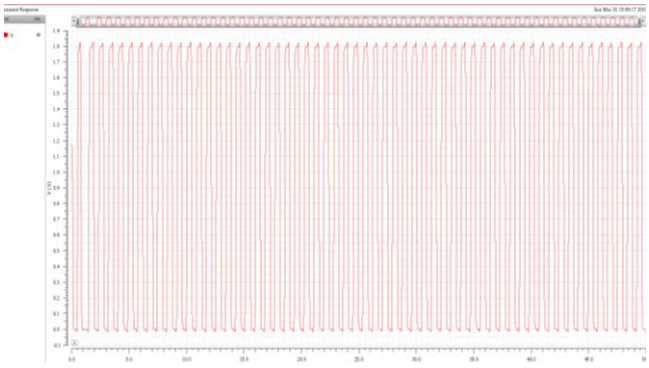

Fig. 4 Output of CSRVCO

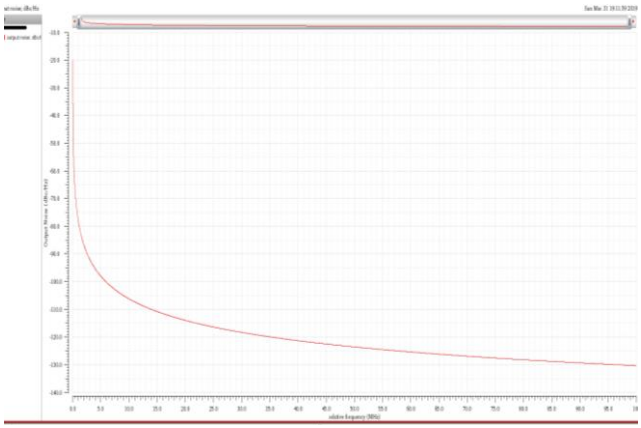

Fig. 5 Phase noise analysis of CSRVCO

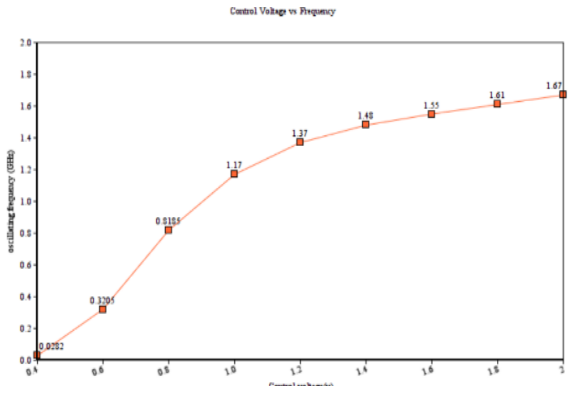

Fig. 6 Control voltage vs output frequency of CSRVCO

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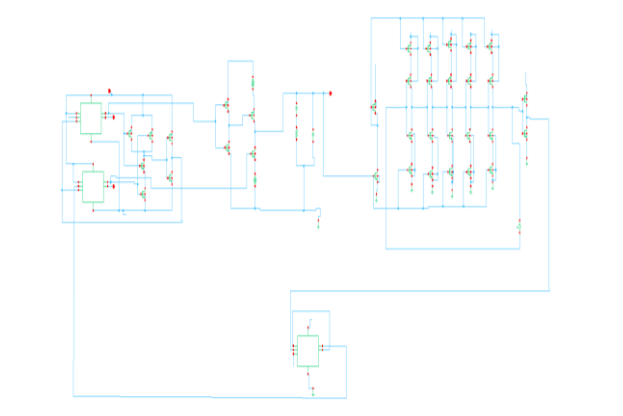

Fig. 7 Schematic of PLL with CSRVCO

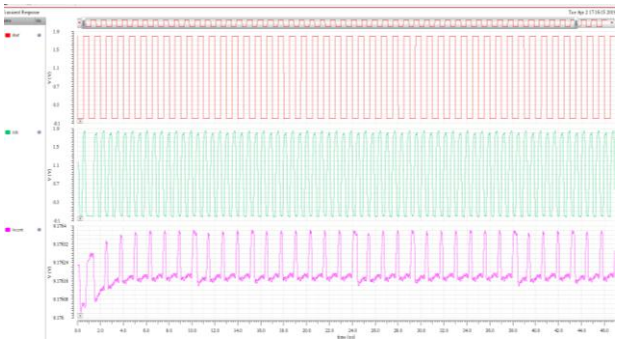

Fig. 8 PLL output with frequency divided output and control voltage

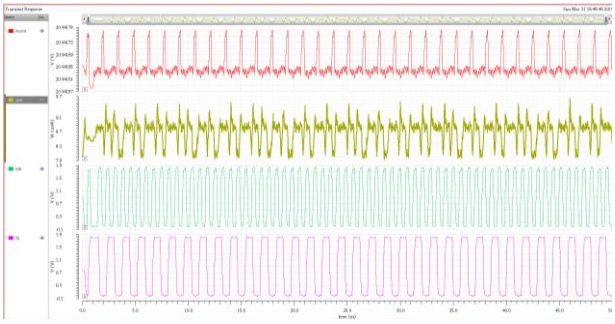

Fig. 9 PLL output with average power

Fig. 10 Output of PLL locks with input

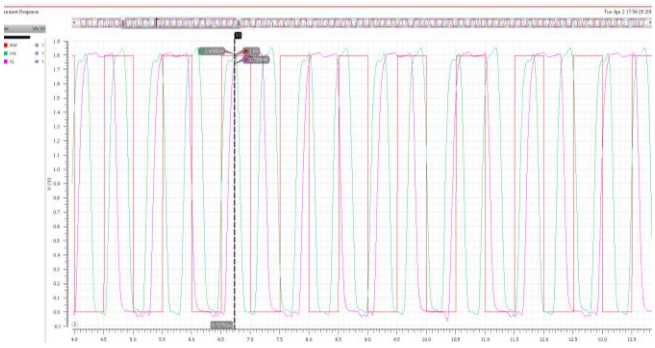

Fig. 11 Locking range of PLL

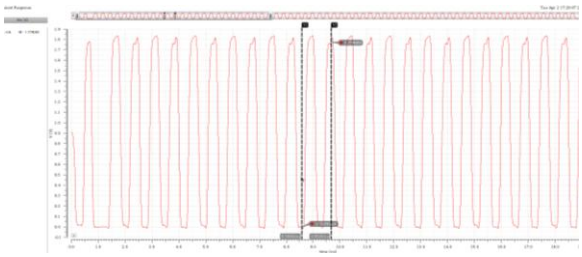

Fig. 12 Tuning range of PLL

V. DISCUSSION AND INTERPRETATION OF RESULTS

The above section contains the results of the PLL simulated. Fig.1 shows the schematic of a D-Flipflop that is implemented using less number of transistors so that propagation delay and power consumption is less. We design the PFD block and frequency divider block with help of the same D-Flipflop and overall power consumption and propagation delay will be less which helps in designing the very low power consumption PLL.

PFD block gives us two signals as output depicted in Fig.2. Which we denoted as FAST and SLOW where FAST gives the phase difference when the input leads the feedback frequency and SLOW gives the output when input lags the feedback frequency. These pulses can be next given to a charge pump where certain operations occurs as discussed above. In the Fig.2 frequency of the first signal is lower than the second signal and therefore gradually increasing pulse widths are generated from second output of the phase detectorFig.3 shows the schematic of the VCO which is current starved Voltage Controlled Oscillator. As mentioned in previous sections, inverters are being starved for the current by upper PMOSFETS.Fig.4 shows output generated by Voltage Controlled Oscillator. Furthermore, the VCO generates the oscillations which further runs the next blocks and is also the output. We then perform phase noise analysis.Fig.5 represents such phase noise analysis plotted and calculated average phase noise of the given values in the graph. This is the phase noise of our PLL.Fig.6 represents the graph which shows the linear variation of oscillating frequency with the gradual increase in the control voltage. Here, input control voltage is increased gradually from 0.4V to 2.0V. By that oscillating frequency is increased from 0.0282MHz to 1.67GHz.

Fig.7 denotes the schematic of the entire PLL circuit where the operations described above take place. We can observe the output at the VCO output pin and input is the reference clock to the frequency divider circuit. Here frequency divider by 2 circuit is used which exactly divides the output frequency of VCO that is given as input to the frequency divider by 2. This frequency divided output is feedback to the second input of Phase Frequency Detector block.
Fig.8 shows the output of CSRVCO PLL along with frequency divider output and control voltage.
Fig.9 shows the output of PLL with CSRVCO along with control voltage, frequency divided output and average power.
Fig.10 shows the output of PLL has the phase locked oscillations of the wave where there is a mismatch at the beginning of the circuit and then locks itself with the input and produces a fairly proper output.
Fig.11 shows the locking range of PLL system as per defined in the previous section.
Fig.12 shows the determining the tuning frequency.
We then calculate various parameters from the output of the PLL from which Fig.8. is shown having the calculation of tuning range for the circuit. We then calculate locking range and also RMS Jitter of the entire circuit. The results of each block can be noticed in the tables below:
Table.2 tells us about the phase-frequency detector with its parameters.
Similarly, we can see that Table.3 constitutes the charge pump as well as the LPF parameters and the values like capacitors, resistors etcetera.
The following Table.4 corresponds to PMOS load ring VCO and its parameters and, Table.5 consists of the current starved VCO parameters.
Table.6 shows the variation of the oscillating frequency with the variation with the control voltage of CSRVCO.
Table. 7 sums up the parameters of PLL system with PMOS load ring VCO.
Table.8 comprises of the parameters of the PLL system with current starved voltage controlled oscillator.
All the parameters listed are obtained from simulation done in Cadence Virtuoso Environment. By all these parameters, we can come to the conclusion that which configuration will be more efficient.

Table. 2 Phase Frequency Detector

Parameter	***Value***
AspectRatio(W/L)	1.33
Technology	UMC180
Average Power	331uW
V_{DD}	1.5V

Table. 3 Charge pump, Low pass filter parameters

Parameter	***Value***
C1	15 pF
C2	1.5 pF
R	1K
Technology	UMC180
V-control	2.84 V

Table. 4 PMOS load Ring VCO parameters

Parameter	***Value***
Power Supply	1.8
No. of Inverter stages	5
Technology	UMC180
Frequency	810 MHz
Average Power	29.31 uW

Table. 5 Current starved VCO parameters

Parameter	***Value***
Power Supply	1.8
No. of Inverter stages	5
Technology	UMC180
Frequency	1.17GHz
Average Power	20uW

Table. 6 Control Voltage vs Frequency of CSRVCO

Control Voltage	***Frequency (GHz)***
0.4	0.0282
0.6	0.3205
0.8	0.8185
1.0	1.17
1.2	1.37
1.4	1.48
1.6	1.55

Table. 7 PMOS load ring VCO findings along with other parameters

Parameter	***Value***
f_{VCO}	820 MHz
Power of PLL	13.68mW
f_{Div}	410 MHz
Technology	UMC180
Power Supply	1.8V
Phase noise	-95.42 dBc/Hz
V-control	2.84 V
Tuning Range	1.21
Offset Frequency	1 GHz
Locking Range	4.27ns onwards

Table. 8 Current Starved VCO findings along with other parameters

Parameter	*Value*
f_{VCO}	1.37GHz
Power of PLL	8.68mW
f_{Div}	685.6MHz
Technology	UMC180
Power Supply	1.8V
Phase noise	-120dBc/Hz
V-control	9.1 V
Tuning Range	1.229
Offset Frequency	1 GHz
Locking Range	6.72ns onwards

By comparing the two PLL systems with the determined parameters, current starved VCO produces the better results when compared to PMOS load ring VCO in many parameters such as power consumption, range of frequency generated, RMS jitter, phase noise etcetera. More over the CSRVCO gives additional advantages such as maintaining a constant amplitude level and furthermore it is also shown that frequency of oscillation is inversely proportional to the supply voltage and hence consumes less power.

VI. CONCLUSION

Everyone needs a legitimate solution, yes? But seldom piles out otherwise. May be this time. The prospects turn out good here as this is played back, to realise a triumph. Achieved as we speak in a series of feedback loops. Part of the feedback is the output. By performing the simulation of the circuit, we could take a moment in noting that the phase noise obtained for the circuit with PMOS load ring VCO is -95.42 dBc/Hz and also the RMS Jitter of the entire PLL circuit can be predominantly noted as 1.8as. For the PLL system with current starved VCO, obtained phase noise is -120dBc/Hz and RMS jitter of total PLL system is 31.27zs. To wrap up things around, the PLL is never a diversion of any sorts but a factual solution.

VII. FUTURE PLANS

This design operates under low power conditions. The present VCO uses a single stage current starved VCO where as it can be done for a current starved VCO [8] with two stages: the first stage being operational transconductance amplifier which produces a constant biasing current at the output and the second stage being N-Inverter stage [9] controlled by the output bias current of the OTA so that we reduce some voltage noise at the input and can obtain even better power consumption. More over by changing the output resistance of the current starved VCO, frequency of oscillations can be varied accordingly [10].

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