Energy Recovery Circuit of Soft Switching Fullbridge Converter using Optimization Techniques

Ranadheer Reddy, S.Manikandan

Abstract: ***This paper is used panel applications for DC-DC converter and full bridge energy recovery circuits of new shift phase converter. Auxiliary resonant network is consisting of main switches and it is used converter for soft switching techniques. Output and input loads are includes condition in operation process. The transformer loss reduction and it is contributed to the soft switching process. Important bridge components are used to uncoupled design in efficient way. Zero-current switching process is operating auxiliary switches with resonant network. The operation modes are analyzed and key designs are analyzed then verify circuits of DC/DC converter. On -polluting and cost free energy are important source to enhance converter then transfer hard and soft switches process. Advanced techniques are used to enhance converters and used switch, diode, capacitor and inductor in SARC (simple auxiliary resonant circuit).ZVS (zero voltage switch), ZCS (zero current switching) are used to operate circuit with main switches .PI controller is use an algorithm of cat swarm optimization.***

Keywords: ZVS, ZCS, IGBTs, ERC, SARC, EMI, CSO.

I. INTRODUCTION

The power converters are utilized by the switching devices and it is includes parasitic capacitances. The collector, emitter, drain, source are provide switching converter. High powers with speed applications are consist of MOSFETs and IGBTs. It is contain high capacitance of various characteristics process. Tail current is used by IGBTs; it is improve loss of turn off. The problems are relieved using snubber and it is contain capacitive of parallel in externally. Hard switching operations are turn on and it consists of large capacitance .EMI noise and switching loss dissipation is occurring in the time [1].In high frequency, converters and inverter switches are used soft switching technologies for solve a different type of problems. High power applications are utilized topology of PWM full-bridge DC-DC converters and used soft switching schemes. Soft switching techniques are implementing in the easy way and it is configure to the full-bridge topology then control MOSFET driving pulse sequence process. The operation of Zero voltage switching is used switching devices then it is includes power efficiency converters. It is perform switching actions with high frequency range. Transformers are designed and used magnetic filters then utilized switching frequency in fixed manner.

The transformer of leakage inductance is utilized by converter and contains additional inductor series.

The level of load current and resonant inductance is affecting the soft switching range. In the time of load current increase effective reduction of duty cycle is affect by inductances, it is a large process. High transformer ratios are reducing stress of diode voltage. The frequency of converter is consisting of limitation and reduces duty. The secondary rectifier diodes are consisting of high inductor and capacitance junctions. The main path soft switching circulates used resonant inductor and contain conduction losses utilized operational modes. Output load is transferred by the resonant power then increase current and load it. Circuit loss is used to increase circulate current and load current. The application includes high and low input voltage load current, it is present resonant conduction loss. It is used loss factor of circuit [2].

PDP applications are contain ERC (energy recovery circuits) for instead of soft switching technologies. Different type of capacitive loads is charge or discharge using ERC.A full-bridge DC/DC converter and AC converter comparison used PDP display and includes ERC driver. The following figure is explaining it. A body capacitance of main switch is containing load capacitance converters. The sustain mode is describe MOSFET junction; it includes characters of electrical capacitive process. Energy is recover power using ERC. Soft switching process is used DC/DC converter for capacitance charge and discharge process. The power stage design operation is utilized by ERC and it is processed based on the extra resonant circuit. The operation of soft switching is contain heavy efficiency and used low energy then it is contribute a size of process.ERC topologies are re generating temporary transformer and analyze it. The experimental results are verified by design example guidelines and it is operate with 50 kHz then used prototype of converter with 1kw.

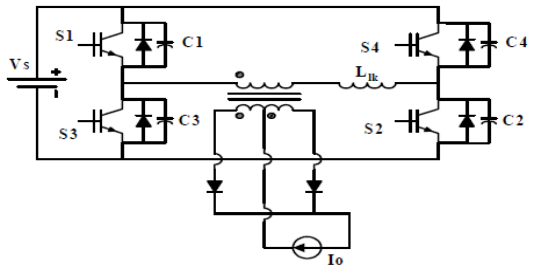

Fig 1. DC/DC converter with conventional phase shift full-bridge

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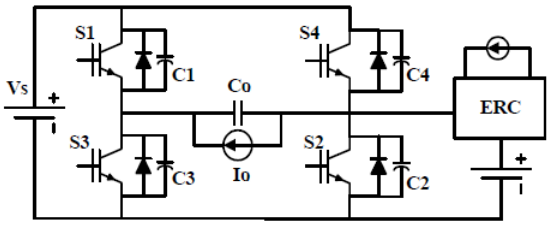

Fig 2. Energy recovery circuit of PDP sustain driver

II. OPERATION PROCESS

The transformer is regenerated then used ERC and circuit converter of ZVS additional circuit. The phase –shift converter provide lagging leg switches and it is connect with auxiliary circuits. An inductor current is described soft switching voltage and used auxiliary circuits. The rectifier diodes of secondary process and resonant inductor of primary process are used current load and junction capacitance it is based on the initial current process. Energy of inductor current is used soft switching and it is depend on the design of load current conditions. Network of auxiliary resonant consist of different load and it is supply resonant energy. Main circuit is used resonant inductor then it is includes energy source with externally. The conditions of Input and output voltage are achieved based on the soft switching techniques. The primary side conduction loss are reduced with circulating energy and used auxiliary network externally, it is includes energy –recovery operations. Resonance inductor with small leakage is increase with effective duty ratio [3].

The soft switching conditions are containing range of input voltage and load variation. In the primary side reduce conduction losses. The secondary transformer is providing procedure of design in the easy way. The selection of inductor optimal resonance is used diodes.

$$T_{delay} = C_{sw}\frac{V_S}{I_{Llk}},$$

$$L_{lk}\cdot {I_{Llk0}}^2 \geq C_{sw}\cdot {V_S}^2 \qquad \text{----------(1)}$$

Here,

$$I_{Llk} = I_{load} / N$$

$$I_{Llk0} = I_{Llk} - \Delta I_{Llk}, \quad \Delta I_{Llk} = \frac{V_S}{\sqrt{\frac{L_{lk}}{C_{eq}}}} \qquad \text{---------- (2)}$$

Here,

C_{sw} is describe the capacitance of switch junction
V_s is describe voltage of input
L_{lk} is describe leakage inductance
N is describing as secondary turn ratio.

III. RELATED WORK PROCESS

The power conditioning system of DC-DC converter is efficient process, it is presented by the soft switching boost converter. The approach of soft switching is used to decrease switching losses .The high voltage current is contain resonant switch converter and utilize low charge battery .PWM is includes loss of switching process and used battery charger. PV system efficiency process is decrease boost converter in the time of turn on or turns off. A simple auxiliary resonant circuit (SARC) is implemented by the boost converter of soft switching techniques. Exchanging techniques are reduced the voltage and used HFtransformer.ZVS and ZCS proposed converter are improve execution and used topology then analyze productivity and transfer converter. DC-DC converter is used MOSFET transfer frameworks. The switching converter of ZVS and ZCS are used diodes with converter switching process. Couple capacitor and inductor is used DC converter with high effective ways. Dynamic switches are consisting of zero voltage converters and use PWM [4].

IV. ANALYSIS OF OPERATION

DC current source are analyzed output filter then assume it. The switches are choose with junction capacitance and it is includes operating modes. The proposed converter is containing conduction paths. During switching cycle operation modes are used proposed converter it is explained in the below figure.

MODE 0[~t_0]:

The diode body, S1, S3 is ON in this process.

MODE 1[t0~t1]:

In this process used t0, Sa2, S1, S3 switches and it is referred as ON stages and remaining switches are OFF stages. The current is flow using leakage inductor. The current is increased in linear way and it is increase resonance inductor then it is reach into inductor current leakage .The voltage transformer (T auxiliary) is regenerated source and contain various voltage.Da1 source are recovered a transformer of regenerate current process[5].

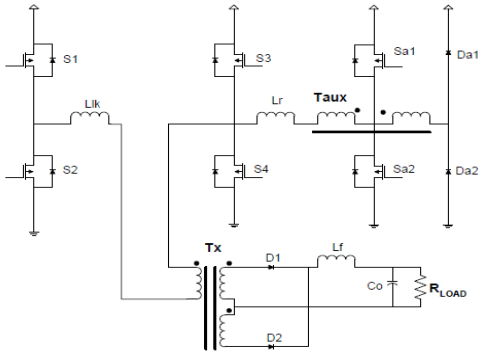

Fig 3. Circuit of full bridge converter

$$I_{Lr}(t) = \frac{V_s - aV_s}{L_r}(t - t_0) \quad where \quad 0 < a < 0.5$$

$$I_{Llr}(t_1) = I_{Llk}(t_1) = I_{Llk0} \qquad t_0 < t < t_1$$

---------- (3)

MODE 2[t1~t2]

This process used t1, it is includes S1, Sa2 switches, it is described as the ON stage then other switches are OFF stages. The S3 is conducting current of anti-parallel diodes; it is contain recovery time in reverse way. At the same time increase resonant current in linearly.

$$I_{Lr}(t) = I_{Llk0} + \frac{V_s - \alpha V_s}{L_r}(t - t_1)$$

----------(4)

Here,

$$I_{Lr}(t_2) = I_{Lr0} \qquad t_1 < t < t_2$$

---------- (5)

$$t_2 - t_1 = t$$ (Reverse recovery of body diode)

---------- (6)

Da1 is used for the recovered transformer then regenerate current process.

MODE 3[t2~t3]

The process stage is used t2.S3 body diode is turnoff in natural ways, and it is includes S1,Sa2 .These are defined as ON stage remaining process are described as OFF stages.S3 and S4 parasitic capacitances are used to begin resonant inductor.S4 is described as reduced to zero voltage. In the primary side Taux design ratio is calculated as twice compare to the secondary winding process.

$$i_{Llk}(t) = -\frac{Z}{L_{lk}\varpi}(I_{Llk0} - I_{Lr0})(1 - \cos\varpi t)$$

$$+\frac{1}{\varpi}\cdot\frac{(\alpha-1)}{L_{lk}+L_r}V_S \sin\varpi t - \frac{(\alpha-1)V_S}{L_{lk}+L_r}t + I_{Llk0}$$

$$i_{Lr}(t) = (I_{Llk0} - I_{Lr0})\cdot\frac{L_{lk}}{L_{lk}+L_r}(1-\cos\varpi t)$$

$$-\frac{1}{\varpi L_r}\cdot\frac{L_{lk}}{L_{lk}+L_r}(\alpha-1)V_S \sin\varpi t + \frac{(1-\alpha)V_S}{L_{lk}+L_r}t + I_{Lr0}$$

$$v_c(t) = (I_{Llk0} - I_{Lr0})Z\sin\varpi t$$

$$+\frac{L_{lk}}{L_{lk}+L_r}(\alpha-1)\cdot V_S\cdot(1-\cos\varpi t) + V_S$$

---------- (7)

Here,

$$Z = \sqrt{\frac{L_{eq}}{C_{eq}}}, L_{eq} = L_{lk} // L_r, C_{eq} = C_{s3} // C_{s4}, \omega = 1/\sqrt{L_{eq}C_{eq}}$$

$$v_c(t_3) = 0,\ i_{Llk}(t_3) = I_{Llk1},\ i_{Lr}(t_3) = I_{Lr1}.$$

---------- (8)

Da1 is recovering a source and it is regenerate transformer using current at the same time of process.

MODE 4[t3~t4]

This process is used t3 and S4 of body diode is on naturally and it is consist of ZVS turn on process. The current is linearly decreased and it is completed resonance in simultaneous way [15].

$$v_C(t) = 0$$

$$i_{Llk}(t) = I_{Llk1} + \frac{V_S}{L_{lk}}(t - t_3) \qquad i_{Llk}(t_4) = I_{Llk2} = \frac{1}{N}I_0$$

$$i_{Lr}(t) = I_{Lr1} + \frac{-\alpha V_S}{L_r}(t - t_3) \qquad i_{Lr}(t_4) = I_{Lr2}$$

----------(9)

Da1 source are recovered transformer and it is regenerate current in the same time.

MODE5 [t4~t5]

This process is used t4 and includes a resonant current of zero value.Sa2 body diode is off naturally then Sa2 is contain ZCS turn off process. Load current is providing by S1 and S4.

$$v_C(t) = 0$$

$$i_{Llk}(t) = \frac{1}{N}I_0$$

$$i_{Lr}(t) = I_{Lr2} + \frac{-\alpha V_S}{L_r}(t - t_4) \qquad i_{Lr}(t_5) = 0$$

----------(10)

MODE6 [t5~t6]

This process is used t5 for relaxation and recovery of the energy part. The load current is provided by the S1 and S4.

$$v_C(t) = 0 \qquad i_{Llk}(t) = \frac{1}{N}I_0 \qquad i_{Lr}(t) = 0$$

-------- (11)

MODE 7[t6~t7]:

The process is used t6 and S1 is off stage. The S1 and S2 parasitic capacitances are charge in the linear way and it is begin to current load process.

$$v'_C(t) = -\frac{1}{C_{eq}}\cdot\frac{1}{N}I_0(t - t_6) + V_S$$

$$i_{Llk}(t) = \frac{1}{N}I_0 \quad , \qquad i_{Lr}(t) = 0$$

$$v'_C(t_7) = 0$$

---------- (12)

MODE 8[t7~t8]:

The process is used t7 and S2 body diodes are turn on in naturally if S2 switch is reduced to zero in the time of voltage process.S2 switch is contain ZVS and it is turn on.S2and S4 are provide circulation of current with leakage inductor[6].

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$$v'_C(t)=0$$

$$i_{Llk}(t)=\frac{1}{N}I_0 \Rightarrow I'_{Llk} \quad , \quad i_{Lr}(t)=0$$

---------- (13)

MODE9 [t8~t9]:

This process is used t8 and contains S4 switch turn off stage.S3 and S4 parasitic capacitances are begin resonant with leakage inductor. The energy is high and it is describe as current load and S4 switch voltage is proportional to the energy of inductor [14].

$$v_C(t)=I'_{Llk}Z_1\sin\varpi_1(t-t_8)$$

---------- (14)

Here,

$$Z_1=\sqrt{\frac{L_{lk}}{C_{eq}}} \quad , \quad \varpi_1=\frac{1}{\sqrt{C_{eq}\cdot L_{lk}}}$$

---------- (15)

$$i_{Llk}(t)=I'_{Llk}\cos\varpi_1(t-t_8) \qquad i_{Lr}(t)=0$$

------- (16)

Mode 9 process in end stage,

$$v_C(t_9)=V_S \; and \; i_{Llk}(t_9)=I'_{Llk0}$$

----------(17)

It is assumed as follow,

$$I'_{Llk}Z_1 > V_S$$

---------- (18)

MODE10 [t9~t10]:

This process is used t9 and includes S3 body diode then it is turn on. The S2 and S3 body diode are containing source then it recovered with leakage inductance and it is used freewheeling current process. Linear way is maintained for decrease a current process.

$$v_c(t_9)=V_S=v_C(t_{10})$$

$$i_{Llk}(t)=\frac{-V_S}{L_{lk}}(t-t_9)=I'_{Llk0} \, , \qquad i_{Llk}(t_{10})=0$$

$$i_{Lr}(t)=0$$

----------(19)

MODE 11[t10~t11]

This process is used t10 .In the time of recovery reverse time produce S3 current of anti-parallel diode process. Linear way the leakage current is decreased.

$$i_{Llk}(t)=\frac{-V_S}{L_{lk}}(t-t_{10}) \quad , \quad i_{Lr}(t)=0$$

$$v_C(t_{10})=v_C(t_{11})=V_S, \; i_{Llk}(t_{11})=-I'_{Llk1}$$

---------- (20)

MODE 12[t11~t12]:

This process is used t11 .The S3 body diode is turn off naturally.S4 parasitic capacitances input voltages are begin resonant of leakage inductor. The resonance is used S4 switch and it is decrease to zero voltage [13].

$$v_c(t)=-I'_{Llk1}Z_1\sin\varpi_1(t-t_{11})-V_S(1-\cos\varpi_1(t-t_{11}))+V_S$$

$$i_{Llk}(t)=-I'_{Llk1}\cos\varpi_1(t-t_{11})-\frac{V_S}{Z_1}\sin\varpi_1(t-t_{11})$$

$$v_c(t_{12})=0, \; i_{Llk}(t_{12})=-I'_{Llk2}$$

----------(21)

MODE13 [t12~t13]

This process is used t11.The S4 body diode is turn on naturally and used S4 switch then turn off ZVS. The S2 and S4 body diode is consisting of circulation current with leakage inductor then it is complete resonance process [7].

$$v_c(t)=0$$

$$i_{Llk}(t)=-I'_{Llk2}-I_{Llk0}$$

---------- (22)

MODE14 [t13~t0]:

This process is used t13 and includes Sa1 switch then turn on. MODE 0 is repeating the operation mode process.

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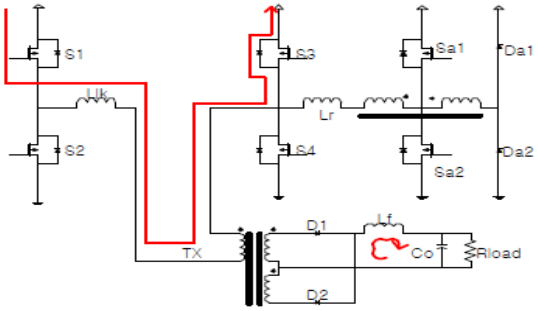
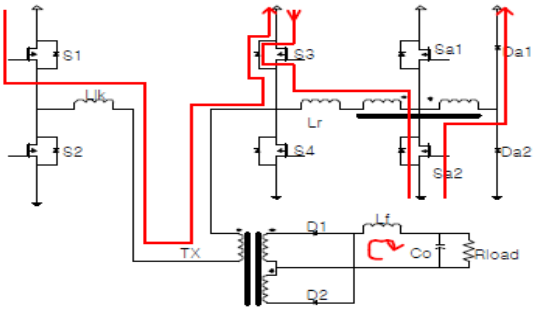
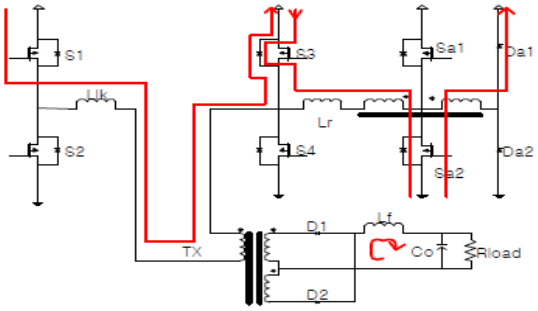


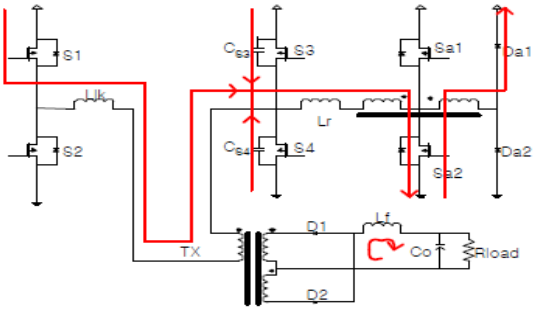
MODE 0



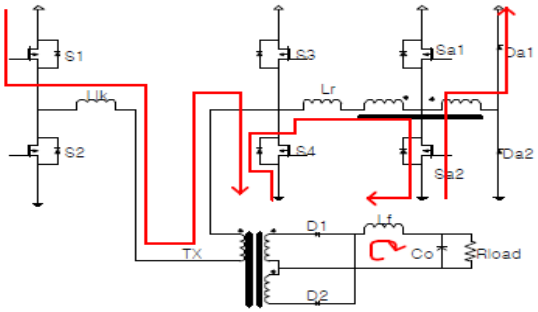
MODE 1



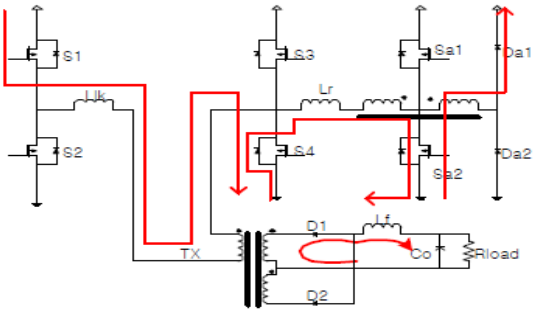
MODE 2



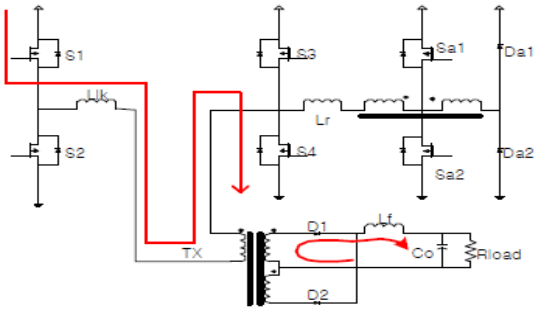
MODE 3



MODE 4



MODE 5



MODE 6

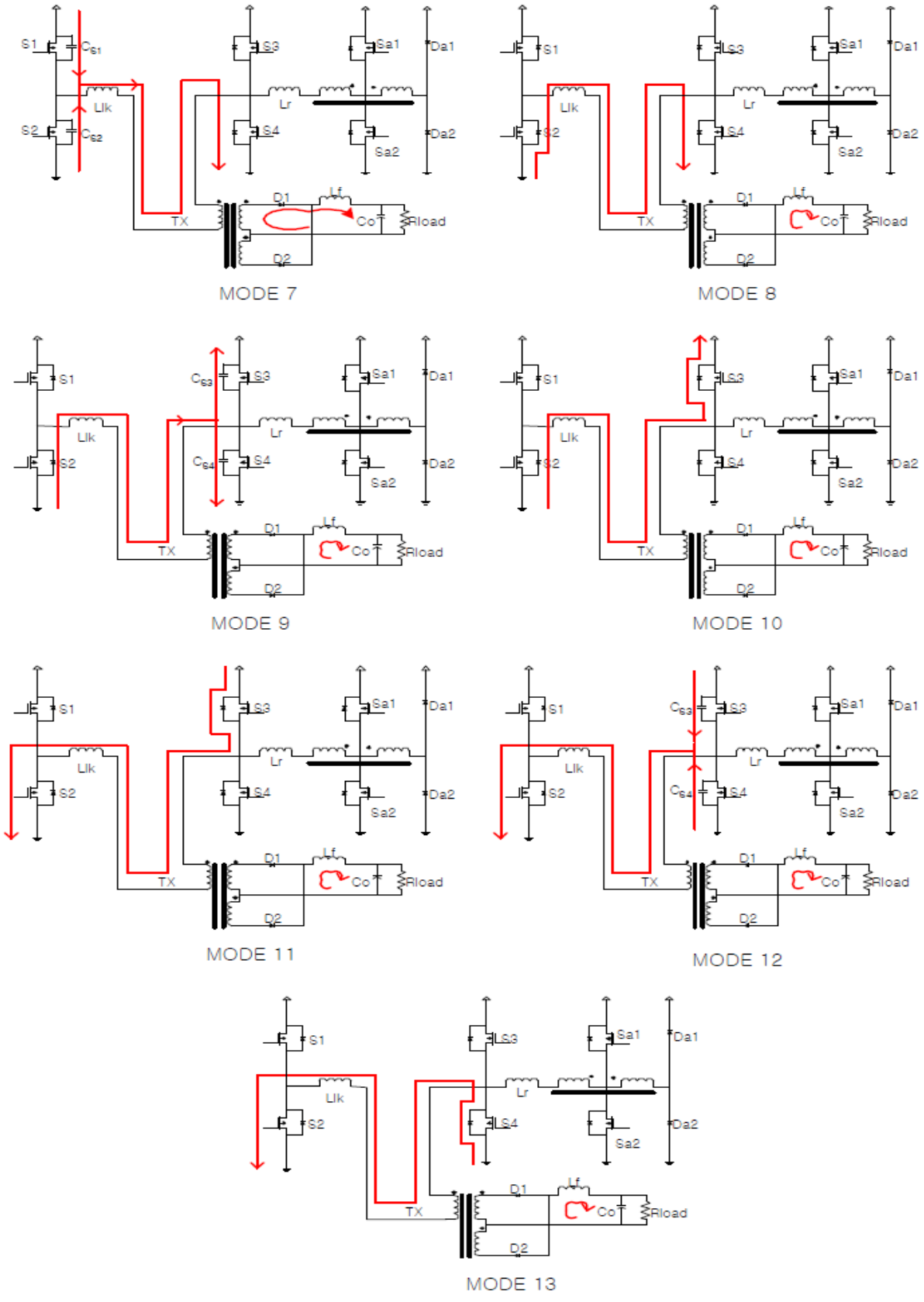


Fig . 4 proposed converter operating modes and conduction path

V. BOOST CONVERTER OF HARDWARE

Switching and soft switching process

DC-DC boost converter is consisting of input and output voltage process. DC-DC converter is includes switches, diodes, capacitors and inductors. The capacitor is utilized by the MOSFET and it is used enhanced converters. Voltage and current converter is containing devices of exchange converters.

An auxiliary resonant circuit is defined as the boost converter circuit of traditional way. The auxiliary resonant circuit is consisting of inductor, capacitor, and switch and diode process. The voltage is reduced by use of ZVS (Zero voltage switching) and ZVS (zero current switching) process. The full capacitor of voltage switch is includes ZVS. Electromagnetic interface (EMI) is reduced normally using full circuit process [8].

CSO Algorithm process

Cat Swarm Optimization is one of the algorithm processes, it is develop and optimize PI controller process. The switching loss is decreased then increase boost converter soft switching process. R-Load and RL –Load are used for switching performance.CSO is described high electricity of resting circumstances. The power is calculated using modes [9].

VI. RESULTS AND EXPERIMENTS

Design process is consisting of soft switching with resonant capacitance. Junction capacitance is providing drain and source of MOSFET. The soft switching energy circuits are need capacitances. The resonant inductance is consist of full-bridge and resonant auxiliary networks. Inductance of resonant is used RMS current and contains zero switching time. Reverse recovery process are used auxiliary diodes in the time of current turn –off. The loss of conduction and time of conduction is designed then trade off it. The conduction loss is decreases and used additional inductor devices. The conduction loss and frequency of switching process is containing duty ratio with high inductance.

Design the transformer and regenerative optimal condition resonance. The half soft switching is described low turn ratio calculation. The auxiliary switches are used inductor current with leakage, resonant inductance, and voltage of input and current load process [10].

The auxiliary resonant network is utilized reverse recovery time and it is affected by the lagging leg switches of body diodes. In ERC resonant inductor is used injection of current in the base of reverse time. The designing of optimal circuit is used time with converter hardware of validate experiments. It is define input voltage and it is specify prototype of hardware process. The range is calculated as 100~500 voltage and includes high duty cycle of Dmax=0.8.The output power of DC is described as the 500W-2kW.The frequency of switching is defined as the 60 kHz. The Tx and N ratio calculation is given below.

$$N \geq V_{in,\min} \cdot D_{eff} / V_0 \qquad \text{--------- (23)}$$

Here,

$$D_{eff} = D_{\max} - f_{sw} \cdot T_{soft}$$

$$T_{soft} = 4\pi / \omega_1 + (t11 - t9) \qquad \text{----------(24)}$$

The full-bridge converter design results are explained in the following tables.

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Table 1. Hardware implementation of devices

	Parameter / Part number	A remarks
Transformer	PQ4040, 2 pieces Input-parallel, output-series	Primary turns: 36 Secondary turns: 13
DC blocking Cap.	4.7 uF (63V)	
Leak. Inductance	25 uH	Extra inductor (10 uH) added
Output Cap.	44 uF (250V)	
Output Inductance	260 uH (40A)	MPP core
Main Switch	2SK2837 (600V, 20A)	MOSFET 4
Rect. Diode	FML34S (400V, 20A)	Ultra fast diode, 4 pieces
Snubber Cap.	0.33 uF (200V)	
Snubber Res.	22 kΩ (2W)	
Snubber Diode	UF5404	Ultra fast diode, single
Reso. Inductor	5 uH	MPP core
Reso. Aux. Switch	IGBT (600V, 10A)	2 pieces
Reso. Aux. Diode	MUR860 (600V, 8A)	Ultra fast diode, single
Regen. Transformer	PQ2020	Primary turns: 7 Secondary turns: 24

The circuit diagram and set of hardware are described. The full-bridge converter is consisting of conventional phase and it is compare to the voltage of switching process and current transformer. In the freewheeling mode of current is used for phase shift converter. The energy source of circulate process is used phase-shift converter of conventional process. The ERC load conditions are contain legging leg soft switching process. The body diode of anti parallel is utilized reverse recovery of current injection process. The switch S2 is used the soft switching technologies and develop the operating condition converter then it is includes low load inputs and heavy load process [11]. The loss of conduction is decreases current circulating process. The different load input range results are used in the process converter. The converters are support R-Load and RL load and it is contain solid conditions with R-stack process. The voltage is given by RL-stack and it is support converters. Strong circumstance is containing extra time process. The converters are developed with R-Stack process [12].

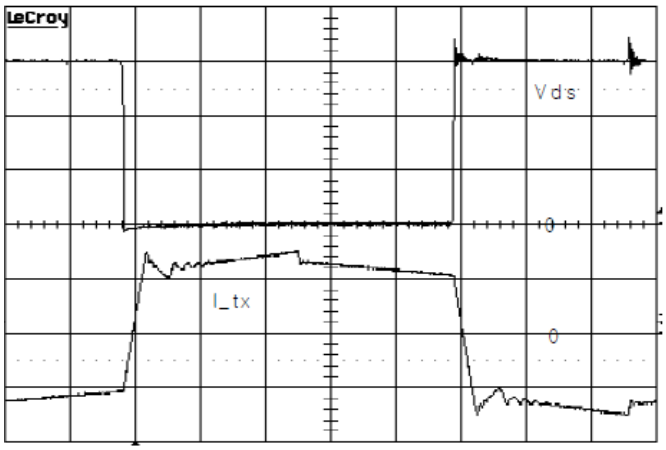

Fig . 5 Conventional converter of S4 primary current transformer

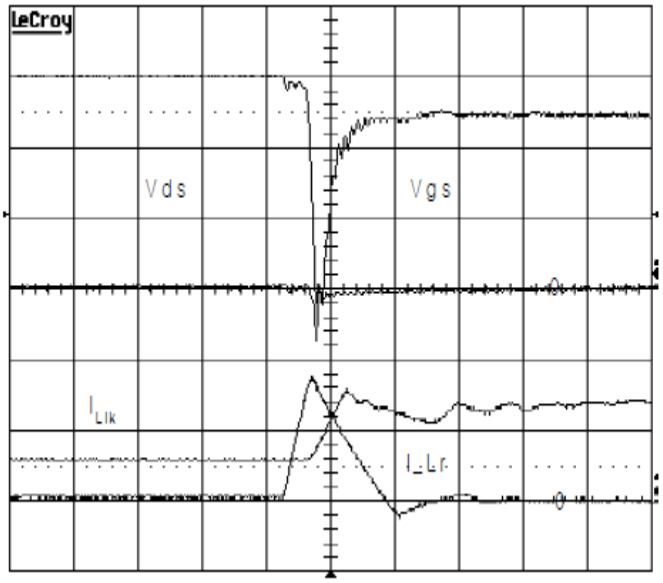

Fig . 6 proposed converter of inductor current .Vds, Vgs of S4 switching process

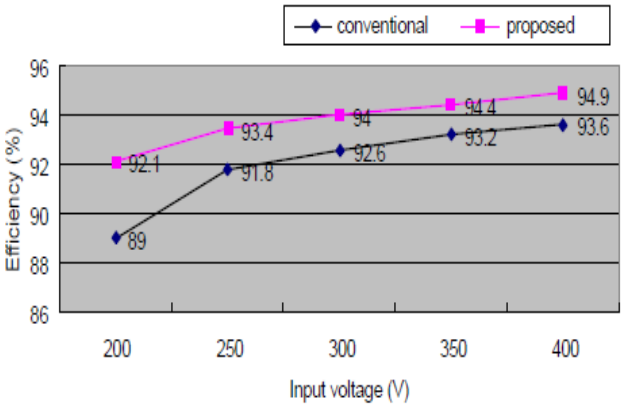

Fig . 7(a) output power of input variations

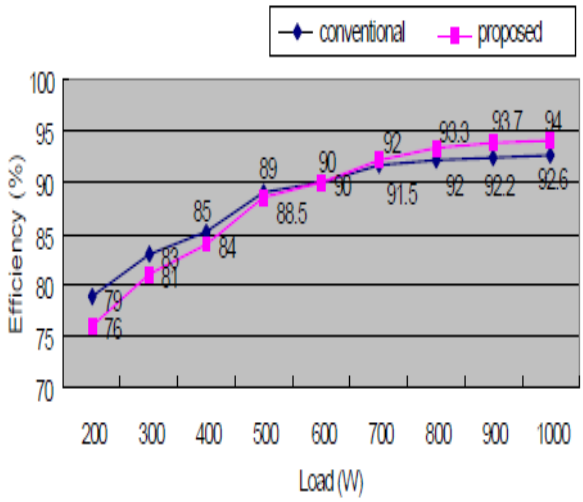

Fig . 7(b) Input voltage of variation of load

Fig . 7 The proposed conventional converter comparison process

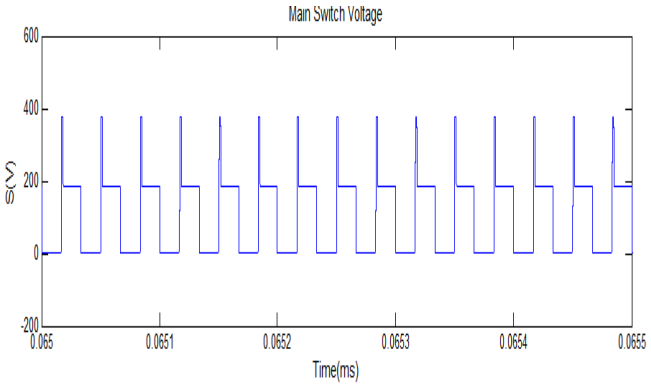

Fig . 8 Main switch of current

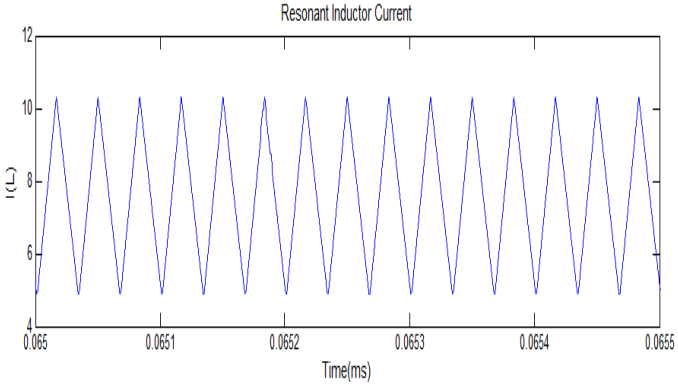

Fig . 9 Converter current of resonant inductor

VII . CONCLUSION

The circulation of primary current is decrease conduction losses and decrease phase shift converter of conventional process. The soft switching operations are supported for additional resonant network. It is includes variation of load with input voltage process. The transformer is regenerate and used device switching then it is connect to side of lagging leg. In the time of load is high and input is low power efficiency is calculated as heavy in the proposed converter process. The design operations are analyzed and verified efficiency of power. The full load process is defined high efficiency power. The recovery of energy circuit is used phase-shift converters of conventional process. Additional resonant network is includes topology of power conversion methods. Simple auxiliary resonant circuit (SARC) is used R-load and RL-stack. The zero voltage switching (ZVS) and zero current switching (ZVC)are used to operate circuits of main switch process.CSO algorithm is used PI controller then boost converter soft switching results are produced by the R-load and RL-load .It is decrease loss of the boost converter soft switching process. The boost converter of hard switching process is used CSO (cat swarm optimization) algorithm process.

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