Design and Analysis of CMOS Schmitt Trigger

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Abstract: ***This paper entitles the implementation of a complementary MOS Schmitt trigger using CMOS 130nm in. Complementary MOS Schmitt trigger is analyzed with the conventional Schmitt trigger in terms of power, slew rate and hysteresis at various technologies and temperatures. The two operating points*** V_{th+} ***and*** $V_{th-\ are}$ ***evaluated with respect to the supply voltages at different technologies and temperature.***

I. INTRODUCTION

In [1], the Schmitt trigger has an inverter-like voltage transfer characteristics, but with two different logic threshold voltages for increasing and for increasing and for decreasing input signals. With this unique property, the circuit can be utilized for the detection of low-to-high and high-to low switching events in noisy environments. In this the W/L ratio is also varied as in Fig.1.

In [2], Schmitt triggers are specially constructed bistable circuits that exhibit hysteresis, therefore input high and low voltages are depend up on the output state of the device. This property is useful in signal shaping applications. In addition, Schmitt trigger display exceptional noise rejection capability because the sum of the noise margins may exceed the supply voltage.

In a Schmitt trigger, positive feedback and greater-than-unity loop gain are required, as with any bistable circuits. The achievement of hysteresis also requires that there be a switching element that introduces a state –dependent voltage between the input and ground. The noise rejection afforded by hysteresis is especially important if a signal is to be applied to a count-up or count-down circuit. This can be understood by considering what happen when a noisy, slowly varying signal is applied to both a conventional inverter and a Schmitt trigger.

The Schmitt trigger correctly interprets the waveform as a single high-to-low transition, whereas the non-hysteresis inverter misinterprets the input waveform. Clearly, this difference is important if the result is to be used by a counter.

In addition to their ability to reject noise, Schmitt triggers are valued for their ability to sharpen slowly varying waveforms in the absence of noise. This is especially true in the case of CMOS, for which slowly varying wave-forms give rise to increased short circuit conduction and the associated dissipation.

In [4] This paper explores the sub threshold operation of the ST and provides complete analytical expressions for its design. In this the voltage transfer characteristic of the ST is analysed and the origin of the hysteresis is explained.

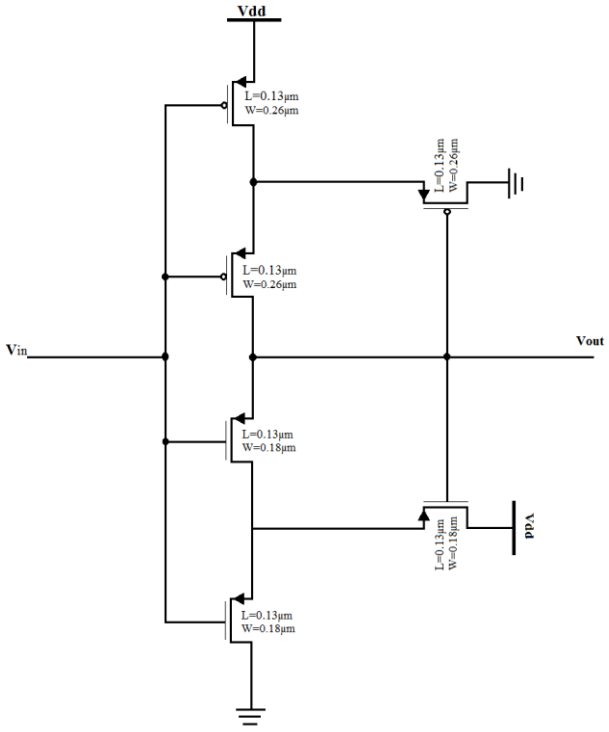

Fig.1 W/L ratio of CMOS Schmitt trigger

II. PROPOSED TECHNIQUE

As shown in Fig.2. the two-fold transistor inverter is utilized because the transistor (N1 and P1) have some higher

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edge voltage than N0 and P0 because of impact and because of which the yield changes to high from low or low from high when after the ON state of N1 or P0 separately.

Presently after expansion of two additional transistors P2 and N2 the circuit is able to give hysteresis. At the point when zero information voltage is connected at the info, both N0 and N1 are in OFF condition while P0 and P1 are in ON condition and yield is at high rationale level. At the point when the information scopes to limit voltage of N0 transistor then N0 will be on, while N1 stays OFF and this time yield will be high N2 will be on, while N1 stays OFF and as of now yield will be high N2 will be on so N0 endeavor to pull down the hub somewhere in the range of N0 and N1 while N2 attempt to destroys up this hub to voltages. At low voltages, the cross coupled inverter pair quality is of noteworthy stress during the advancement and read action, to improve the dauntlessness of data read (0 and 1), Schmitt trigger game plan is used. In this structure, ST increases or lessens the trading edge of an inverter depending upon the course (PMOS and NMOS) of the yield change. This alteration is cultivated with the help of course of action transistor analysis procedure with diminished transistor mean action.

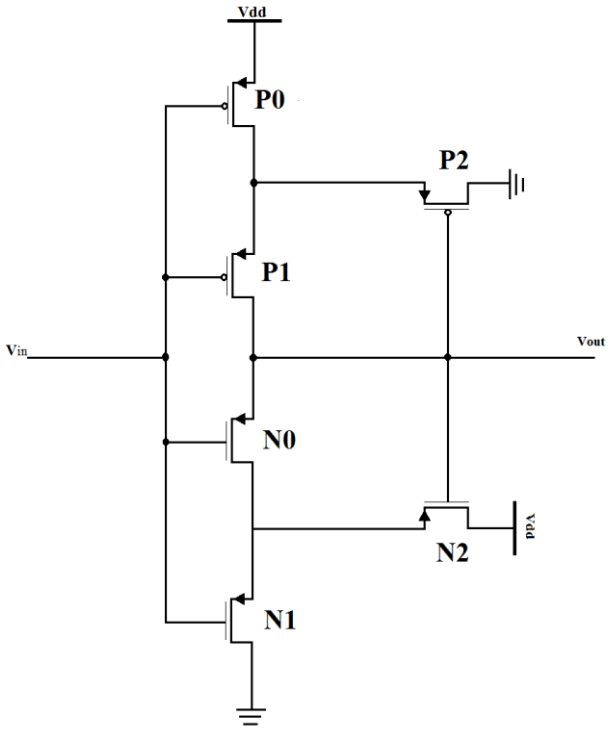

Fig. 2 Schematic of CMOS ST

III. MATHEMATICAL ANALYSIS

In [1], we start our analysis assuming that input voltage is increasing from 0 to V_{DD} .

$$i)\ At\ V_{in} = 0\ V:$$

P0 and P1 are turned on, then

$$V_x = V_y = V_{DD} = 1.2\ V$$

N0 and N1 are turned off. P2 is off; N2 is on and operates in saturation region. Calculating the threshold voltage of N2 with 2 $\emptyset_F$ = -0.6 V,

$$V_z = V_{DD} - V_{T,6} = 0.85\ V$$

$$ii)\ At\ V_{in} = V_{T\,0,n} = 0.24\ V:$$

N1 turns on, N0 is still off.

$$V_x = 1.2\ V$$

$$iii)\ At\ V_{in} = 0.5\ V$$

Assume N0 is off, while both N1 and N2 operate in saturation region.

$$\frac{1}{2}k'\left(\frac{W}{L}\right)_{P0}\left(V_{in} - V_{T0,n}\right)^2 = \frac{1}{2}k'\left(\frac{W}{L}\right)_{N2}\left(V_{DD} - V_z - V_{T,N2}\right)^2$$

Solving this we get

$$V_z = 0.7\ V$$

As per assumption N0 is indeed turned off:

$$V_{G\,S,4} = 0.2 - 0.7 = -0.5 < V_{T\,0,n} = 0.3$$

$$iv)\ At\ V_{in} = 0.85\ V:$$

V_z Continues to decrease. Assuming N1 in linear region and N2 in saturation

$$\frac{1}{2}k'\left(\frac{W}{L}\right)_{N1}\left[2\left(V_{in} - V_{T0,n}\right)V_z - {V_z}^2\right] = \frac{1}{2}k'\left(\frac{W}{L}\right)_{N1}\left(V_{DD} - V_z - V_{T,N2}\right)^2$$

$$V_z = 0.2\ V$$

Gate to source voltage of N0

$$V_{G\,S,4} = 0.85 - 0.2 = 0.65 > V_{T\,0,n} = 0.3$$

We conclude that upper threshold voltage $V_{th}{}^+$ is approximately equal to 0.85V

Now by considering a negative input sweep, i.e.: assuming the input voltage from V_{DD} to 0.

$$i)\ V_{in} = 1.2V:$$

N0 and N1 are on, so that the output voltage V_x = 0V. The PMOS transistors P0 and P1 are off, and P2 is in saturation, thus,

$$\frac{1}{2}k'\left(\frac{W}{L}\right)_{p2}\left(0 - V_y - V_{T,p2}\right)^2 = 0$$

$$V_y = -V_{T,p2} = -\left[V_{T0,p} - 0.4\left(\sqrt{0.6 + V_{DD} - V_y} - \sqrt{0.6}\right)\right]$$

$$V_y = 0.25V$$

$$ii)\ At\ V_{in} = 1.0V:$$

P0 is at the edge of turning on, P1 is off, and P2 is in saturation. The output voltage is still un-changed.

$$iii)\ At\ V_{in} = 0.8V:$$

P0 is on and in saturation region. P2 is also in saturation, thus,

$$\frac{1}{2}k'\left(\frac{W}{L}\right)_{p0}\left(V_{in} - V_{DD} - V_{T0,p}\right)^2 = \frac{1}{2}k'\left(\frac{W}{L}\right)_{p2}\left(0 - V_y - V_{T,p2}\right)^2$$

$$V_{in} = 0.5V$$

Now we determine the gate-to-source voltage of P1 as

$$V_{G\,S,2} = 0.8 - 0.5 = 0.3 > V_{T0,p} = -0.3$$

This indicates that P1 is still turned off at this point.

$$iv)At\ V_{in} = 0.35V:$$

If P1 is still off, P0 is in the linear region, and P2 is in the saturation region:

$$\frac{1}{2}k'\left(\frac{W}{L}\right)_{p0}\left(2\left(V_{in} - V_{DD} - V_{T0,p}\right)\left(V_y - V_{DD}\right) - \left(V_y - V_{DD}\right)^2\right) = \frac{1}{2}k'\left(\frac{W}{L}\right)_{p2}\left(0 - V_y - V_{T,3}\right)^2$$

$$V_y = 0.65V$$

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At this point the PMOS transistor P1 is already turned on. Consequently, the output voltage is being pulled up to $V_{DD.}$ and concludes that the lower logic threshold voltage V_{th}^{-} is approximately equal to 0.35V.
In theoretical analysis, V_{th}^{+}=0.85V and V_{th}^{-}=0.35V and as per the practical analysis, V_{th}^{+}=0.907V and V_{th}^{-}=0.129 at an operating frequency of 500MHz and a supply voltage of 1.2V.

The Table1 describes complementary MOS Schmitt trigger operation is performed with W/L ratios of PMOS & NMOS transistors at different voltages with respect to their technologies.

Table . 1 WL ratios of CMOS Schmitt trigger at different technologies

	Technology	130nm	90nm	60nm	32nm	22nm
	Supply Voltage	1.2V	1V	0.8V	0.6V	0.5V
NMOS	Length (µm)	0.13	0.09	0.06	0.032	0.022
	Width (µm)	0.18	0.1	0.075	0.045	0.035
PMOS	Length (µm)	0.13	0.09	0.06	0.032	0.022
	Width (µm)	0.26	0.18	0.12	0.064	0.5

IV. RESULT AND ANALYSIS

The Table2 describes complementary MOS Schmitt trigger operation with different operating point's v_{th+} & v_{th-} at various temperatures with respect to their technologies.

Table. 2 Vth+ and Vth- values of CMOS Schmitt trigger operated using different technologies.

	Range	130nm	90nm	60nm	32nm	22nm
V_{th+} (mV)	0° C	790	665	540	460	415
	10° C	795	670	540	460	420
	27° C	800	665	535	455	425
	36° C	800	670	535	455	425
	50° C	795	670	535	460	430
	60° C	790	665	540	455	430
V_{th-} (mV)	0° C	315	330	260	130	150
	10° C	325	340	255	130	145
	27° C	335	335	265	135	150
	36° C	345	330	260	140	150
	50° C	340	330	265	140	160
	60° C	340	325	260	145	150

In [4], it's demonstrated that the hypothetical least offer voltage expected to get hysteresis is

$$2\ln(2+\sqrt{5})\ kT/q = 75mV$$

at room temperature theoretically. And done this practically at a frequency of 500MHz a hysteresis of 77.8mV is obtained practically which is approximately equal to the theoretical value of 75mV. The Table3 describes complementary MOS Schmitt trigger operation in terms of power at different temperatures with respect to their technologies.

Table. 3 Power dissipation of CMOS Schmitt trigger with respect to temperature and technologies

		POWER (µW)				
	Technology	130nm	90nm	60nm	32nm	22nm
Temperature	0° C	3.2132	1.7377	0.5944	0.0422	0.0222
	10° C	3.1338	1.6883	0.5809	0.0424	0.0216
	27° C	3.1139	1.5715	0.5464	0.0396	0.0208
	36° C	3.0483	1.5261	0.5321	0.0396	0.0205
	50° C	3.0934	1.4720	0.5247	0.0386	0.0204
	60° C	2.8978	1.4148	0.5017	0.0380	0.0202

The output waveforms of complementary MOS Schmitt trigger is in fig3 considering a sinusoidal signal as an input signal with an operating frequency of 500MHz, DC Offset =0V, Supply voltage V_{DD}=1.2V

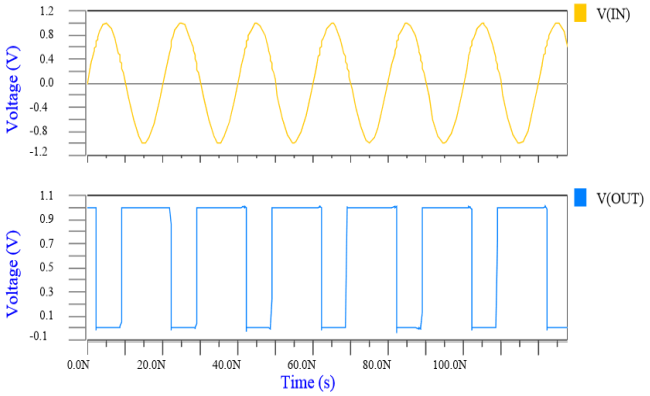

Fig. 3 Output Waveforms

From the above fig3, it is observed a square wave output is obtained with unequal time periods i.e. T_{ON} != T_{OFF} that results in an asymmetrical square wave. It is also observed that T_{ON} period is large compared with T_{OFF} period.

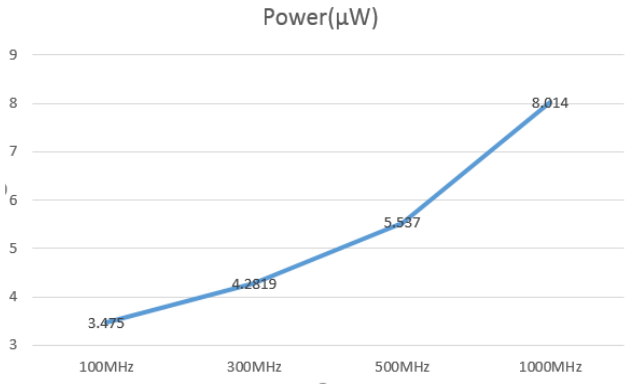

Fig. 4 Power (µW) Vs. Frequency (MHz)

A comparison of power with frequency is in Fig4, From the fig4, it is observed that the power increases with increase in frequency. The above graph describes power variation with frequency from 100MHz to 1000MHz. The minimum power is observed at frequency of 100MHz and maximum power is observed at 1000MHz respectively.

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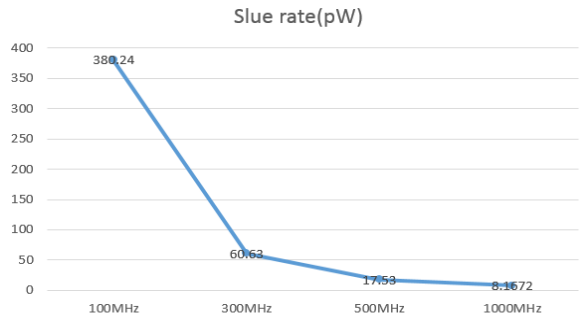

Fig. 5 Slew Rate (ps) Vs. Frequency (MHz)

A comparison of slew rate with frequency is in Fig5, from the fig5, it is observed that the slew rate decreases with increase in frequency. The above graph describes slew rate variation with frequency from 100MHz to 1000MHz. The maximum slew rate is observed at frequency of 100MHz and minimum slew rate is observed at 1000MHz respectively.

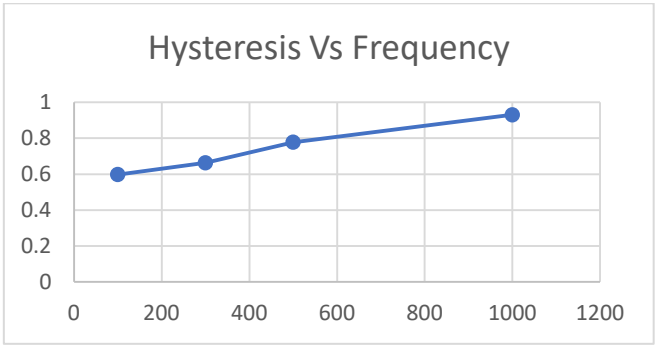

Fig. 6 Hysteresis (mV) Vs. Frequency (MHz)

A comparison of hysteresis with frequency is in Fig6, from the fig6, it is observed that the hysteresis increases with increase in frequency. The above graph describes hysteresis variation with frequency from 100MHz to 1000MHz. The minimum hysteresis is observed at frequency of 100MHz and maximum hysteresis is observed at 1000MHz respectively. In this context, hysteresis at 500MHz is considered for designing complementary MOS Schmitt trigger.

V. CONCLUSION

The paper concludes that a Complementary MOS Schmitt trigger is a power efficient device for the use of many portable applications and is advantageous over conventional Schmitt trigger in power by 50%. Complementary MOS Schmitt trigger presents perfect voltage swings for both logic 0 and logic 1 at 500MHz frequency. It also concludes that the average power dissipation decreases with increase in temperature and advancements in technology respectively. Average power dissipation increases and slew rate decreases with increase in frequency. The hysteresis obtained at 500MHz is approximately equal to theoretical hysteresis=77.8mV.

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