Performance Comparison of Dynamic Bias Comparators

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Abstract: ***This paper encloses the performance comparison of dynamic bias based double-tail latch and Elzakker's comparators using HEP 1 by MENTOR GRAPHICS in 130nm CMOS process. Power, delay & PDP of these comparators are compared with & without using dynamic bias that results in significant improvement of these parameters Performance comparison of these parameters utilize 500MHz frequency. Dynamic bias comparators may scale back the common energy consumption when compared to the prior comparators.***

Keywords: ***Dynamic bias, double-tail latch comparator, Successive Approximation Register (SAR), Elzakker comparator, Analog-to-digital converter (ADC).***

I. INTRODUCTION

The STRONGARM latch with its alternatives can vastly use as comparators for their long last feedback needed for fast selections, static power consumption, and full swing outputs, they suffer from very high needed voltage headroom that yield is difficult to sort them in very low voltage low-sub-micron technologies. An inclusion, due to less isolation between regeneration latch and differential input stage, the latch will suffer from very high kickback noise at the inputs, a common mode dependent offset that may be deal with especially for data converters. The double-tail latch structure bestowed in quenched these problems by dividing the preamplifier from the latching operation, whereas at the constant time low voltage headroom demand and allows the operation at lower supply voltages.

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Double-tail latch comparator is dynamical from the years for more applications for ADCs.

In double-tail latch comparator aims for successive approximation register ADC as in the Figure.1, the pre-amplifier is hard-switched into robust inversion. The extra degree of freedom will be provided for each tail transistor one for the latch stage and other for the pre-amplifier. It provides the individual management to the regeneration time for the latch stage and for the common-mode current for the pre-amplifier

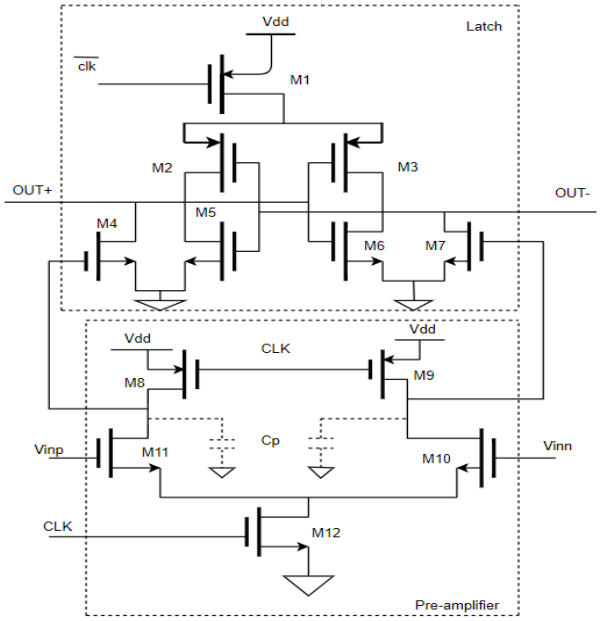

Fig. 1 Double-tail latch comparator

It will be yield at high operation but also produce relatively very high input referred sound levels that are filtered to the capacitances Cp at the pre-amplifiers output nodes in Fig1. It will consist almost 75% of the energy consumption comparators. The energy- per- comparison is provided for a given signal to noise ratio then determined by the value of these C_P's. the SAR ADCs aims for very-less power wireless sensor nodes with high resolution. The energy needed by the pre amplifier can be reduced by the use of bi directional amplifier. In this a detailed analysis of the latch type comparator with a dynamic bias-based pre-amplifier is discussed.

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II. PRIORART

The operation of double-tail latch comparator is in Fig1.

1. RESET PHASE: When CLK=0, the M8 and M9 transistors pre-charge the AI+ and AI- nodes to V_{DD}, that makes transistors M4 and M7 to discharge their output nodes to GND.
2. COMPARISON PHASE: When CLK = V_{DD}, M12and M1 turn ON, M11 and M8 turn OFF and voltages at nodes AI+ & AI- starts to drop. During the RESET PHASE, these nodes have to be charged from the GND to V_{DD}, which leads to high power dissipation.

The STRONGARM latch topology finds wide usage as way electronic equipment, a comparator, or simply a powerful latch with high sensitivity. The term "STRONGARM" commemorates the use of this circuit in Digital instrumentality Corporation's sturdy ARM silicon chip but the basic structure was originally introduced by Toshiba's Kobayashi. STRONGARM latch has some reasons they are:

a. Static power is zero,
b. Provides rail-to-rail swing,
c. Input- offset is obtained only from one differential pair.

In this, we have a tendency to analyze the circuit and its properties. Due to technology, there is the requirement of large voltage.

For use in SAR ADCs, Elzakker introduced an efficient comparator as in Fig3. In this, the preamplifier stage is identical but the output is fed back to the PMOS transistors that are present within the latch. In COMPARISON PHASE, when CLK =0 the AI+ and AI− nodes are at V_{DD} and PMOS transistors are OFF, which is ensured that once the output of the common mode voltage of the preamplifier decreases below the threshold voltage of the transistors, then the latch stage starts conducting. A sufficient differential voltage at its inputs to perform the operation of regeneration when the latch stage turns "ON".

Double-tail latch is dynamic from the past few years for the simplest energy consumption ADC's. The double-tail latch-design is like minded for low-voltage operations, mainly in applications such as sense amplifiers for on-chip digital communication that operates close to V_{DD}. It suffers from the poor management of energy dissipation for a given SNR which is because that the regenerative latch as well as the preamplifier stage begins operating at the identical time. The differential voltage at the pre amplifier output is close to zero at the beginning of the comparator operation.

III. PROPOSED ART

In dynamic bias, it is proposed and used recently to decrease energy charge steering current mode logic in double-tail latch comparator and a uniform charge is needed at each node for comparator operation.

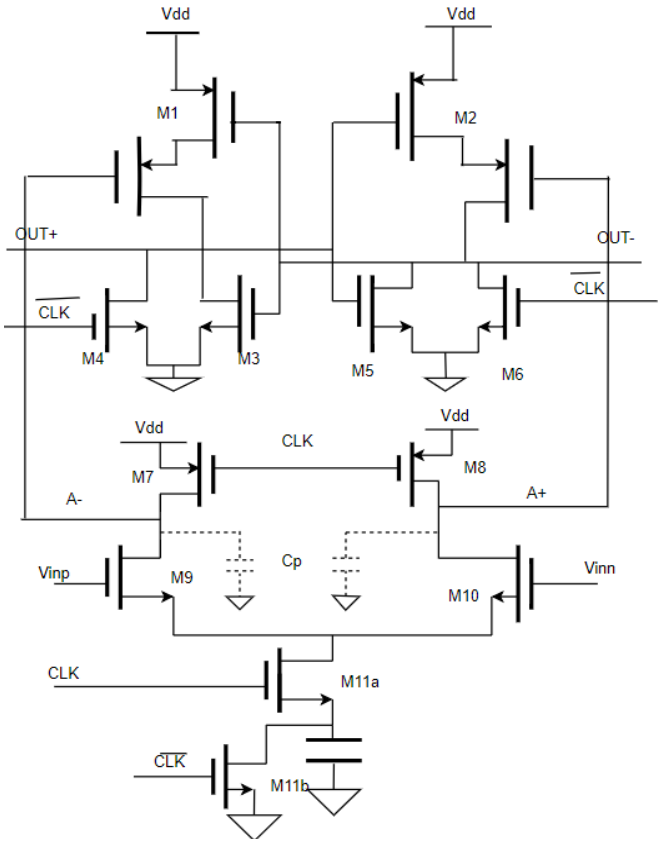

Fig. 2 Dynamic Bias Elzakker's Comparator

The dynamic bias technique could be a comparatively simple method to scale back the amount of discharge on the preamplifier output energy bias. The dynamic bias comparator is employed to make minimized energy applications in electronic communication & restoring circuits like clock-data recovery.

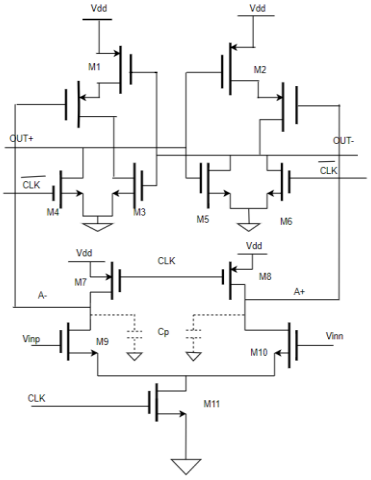

Fig. 3 Elzakker's Comparator

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In this, dynamic biasing is applied to a double-tail latch comparator to enhance the performance. The switched-current tail transistor M11 in Figure3 is replaced by a tail capacitor and a switch tail transistor M11a in Figure2. The dynamic bias comparator is in Figure2.

RESET PHASE: If CLK= 0, the M7 & M8 transistors pre-charge the AI+ and AI− drain nodes to V_{DD}, transistors M4 and M5 are used to RESET the latch and the C_{TAIL} is discharged to GND through M11b.

COMPARISON PHASE: If CLK = V_{DD}, M11b, M8, M7, M4 and M5 which are used as reset transistors are turned OFF. The M11atransistor turns ON and the capacitances on the AI+ and AI- nodes start discharging. From the discharge of the capacitances, common mode current results in a tail current, I_{TAIL} that charges the capacitor C_{TAIL}. During the COMPARISON phase, as the voltage V_{CAP} increases, it decreases V_{GS} and that results in providing a dynamic bias to the differential pair. Both transistors M9 or M10 turns OFF and the voltage at drain of that transistor saturates. Another transistor will continue to discharge to its Cp until the second quenching point is reached i.e., V_S = max ($V_{INP} - V_T$, $V_{INN} - V_T$).When compared to the double-tail latch with the dynamic bias, both the nodes in the double-tail latch are completely discharged

Figure 4 represents double-tail dynamic comparator which consumes less energy consumption when compared to Double-tail comparator. In the double-tail dynamic comparator, there will be two input controlling transistors, M11 and M10 and there is also two transitional stage transistors M4 and M7 as shown in the figure 4 and it works in the both RESET phase and TRANSITION.

IV. COMPARATIVEANALYSIS

Power Delay Product is the product of power (averaged over a switching event) times the input–output delay.

PDP=2*(Average Power) *Delay

Value of 2 defines for both low to high and high to low transitions. The average power and delay are calculated for different types of comparators in Table 1. These are calculated at ΔV_{IN}=0.1, f=500MHz, V_{DD}=5V and at 27 degrees Celsius.

Table 1 . Comparison of different types of comparators with Power and Delay at ΔV_{IN}=0.1V.

Type of Comparator	Average Power(µW)	Delay (ps)	PDP (aJ)
Double-tail	100.662	202.434	20377.41
Elzakker	78.897	99.289	7833.604
Dynamic bias	31.126	99.208	3087.948
Double-tail dynamic bias	88.897	51.286	4556.504

The values of power delay product are plotted for different types of comparators as in figure 5. Double tail comparator has the highest power delay product and the dynamic bias comparator has the lowest power delay product.

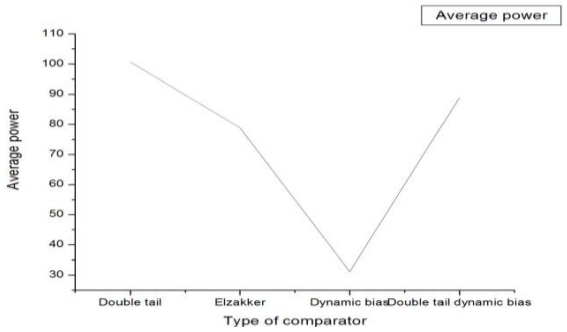

Fig . 6 Plot of average power with different types of comparators

The average power and delay are calculated for different types of comparators in Table 2. These are calculated at ΔV_{IN}=0, f=500MHz, V_{DD}=5V and at 27 degrees Celsius.

Table 2. Comparison of different types of comparators with Power and Delay at $\Delta V\Delta V_{IN}$ =0V.

Type (Comparators)	Average Power(µW)	Delay (ps)	PDP (aJ)
Double- tail	223.452	100.67	22494.912
Dynamic bias	100.765	69.081	6954.38
Double-tail Dynamic	78.564	89.654	7043.576

The values of power delay product are plotted for different types of comparators as in figure 7. Double-tail comparator has the highest power delay product and the dynamic bias comparator has the lowest power delay product.

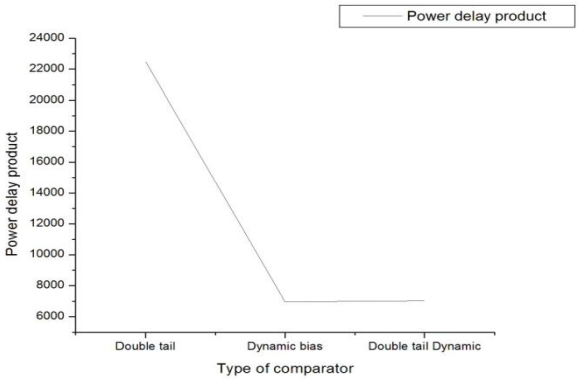

Fig . 7 Plot of power delay product with different types of comparators.

The values of average power are plotted for different types of comparators as in figure 8. Double-tail comparator has the highest average power and the dynamic bias comparator has the lowest average power.

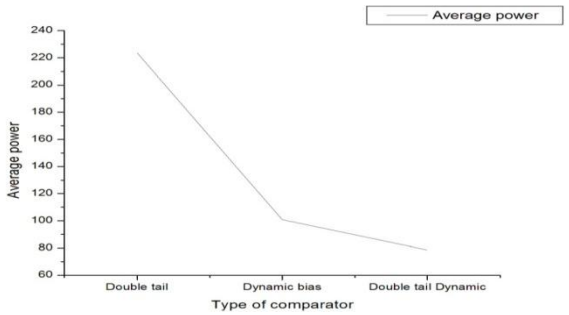

Fig . 8 Plot of average power with different types of comparators.

Here the average power and delay are calculated for double-tail comparator in Table 3. These are calculated at different types of temperatures and at ΔV_{IN}=0.1V, V_{DD}=1.2V, V_{CM}=1.2V, V_{INP}=1.3V, V_{INN}=1.1V, f=500MHz.

Table 3. Variation of Power delay product (PDP) with temperature of Double-tail Comparator at ΔV_{IN}=0.1V.

Temperature (Degrees)	Power (µW)	Delay (ps)	PDP (aJ)
0	179.35	18.649	3344.69
5	219.97	19.957	4389.94
15	221.01	19.958	4410.91
27	223.47	19.786	4421.57
36	233.89	20.398	4770.88
50	234.48	20.434	4791.36
60	236.56	28.270	6687.55

Here the average power and delay are calculated for double-tail comparator in Table 4. These are calculated at different types of temperatures and at ΔV_{IN}=0V, V_{DD}=1.2V, V_{CM}=1.2V, V_{INP}=1.2V,V_{INN}=1.2V, f=500MHz.

Table 4. Variation of Power delay product (PDP) with temperature of Double-tail Comparator at ΔV_{IN}=0V.

Temperature (Degrees)	Power (µW)	Delay (ps)	PDP (aJ)
0	98.595	201.080	19825.48
5	98.456	201.880	19876.297
15	99.240	203.405	20185.91
27	100.662	204.434	20578.735
36	101.114	206.392	20869.12
50	102.196	206.491	21102.55
60	102.662	207.912	21344.66

The average power and delay are calculated for Elzakker comparator in Table 5. These are calculated at different types of temperatures and ΔV_{IN}=0.1V, V_{DD} =1.2V, V_{CM} =1.2V, V_{INP}=1.3V, V_{INN}=1.1V, f=500MHz.

Table 5. Variation of Power delay product (PDP) with temperature of Elzakker's Comparator at ΔV_{IN}=0.1V.

Temp (Degrees)	Power (µW)	Delay (ps)	PDP (aJ)
0	31.737	99.324	3152.24
5	31.612	99.400	3142.23
15	31.375	99.686	3127.64
27	31.900	99.289	3167.319
36	33.635	100.163	3368.98
50	33.952	102.223	3470.67
60	34.433	102.472	3528.41

The average power and delay are calculated for Dynamic Bias comparator in Table 6. These are calculated at different types of temperatures and ΔV_{IN}=0.1V, V_{DD}=1.2V, V_{CM} =1.2V, V_{INP}=1.3V, VI_{NN}=1V, f=500MHz.

Table 6 .Variation of Power delay product (PDP) with temperature of Dynamic Bias Comparator at ΔV_{IN}=0.1V.

Temp (Degrees)	Power (µW)	Delay (ps)	PDP (aJ)
0	174.50	100.84	17596.58
5	180.56	100.89	18216.69
15	188.81	101.84	19228.41
27	188.40	104.85	19753.74
36	189.39	104.83	19853.75
50	190.38	105.83	20147.91
60	190.32	107.83	20511.42

The average power and delay are calculated for Dynamic Bias comparator in Table 7. These are calculated at different types of temperatures and ΔV_{IN}=0V, V_{DD}=1.2V, V_{CM} =1.2V, V_{INP}=1.2V V_{INN}=1.2V, f=500MHz.

Table 7 .Variation of Power delay product (PDP) with temperature of Dynamic Bias Comparator at ΔV_{IN}=0V.

Temp (Degrees)	Power (µW)	Delay (ps)	PDP (aJ)
0	18.071	100.174	1810.24
5	19.003	100.187	1903.85
15	19.003	101.371	1926.35
27	20.107	101.081	2032.43
36	24.861	101.184	2515.53
50	25.359	102.247	2592.88
60	25.968	102.824	2670.13

The average power and delay are calculated for Double-tail Dynamic Bias comparator in Table 8. These are calculated at different types of temperatures and ΔV_{IN}=0.1V, V_{DD}=1.2V, V_{CM} =1.2V, V_{INP}=1.3V, V_{INN}=1.2V, f=500MHz.

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Table 8 .Variation of Power delay product (PDP) with temperature of Double-tail Dynamic comparator at ΔV_{IN}=0.1V.

p (Degrees)	Power (µW)	Delay (ps)	PDP (aJ)
0	40.591	98.848	4012.33
5	42.563	98.847	4207.22
15	42.815	99.845	4274.86
27	43.401	99.841	4333.19
36	44.403	100.83	4477.24
50	46.387	101.82	4723.35
60	46.228	102.83	4753.76

Here, the average power and delay are calculated for double-tail Dynamic comparator in Table 9. These are calculated at different types of temperatures and at ΔV_{IN}=0V,V_{DD}=1.2V, V_{CM}=1.2V,V_{INP}=1.2V,V_{INN}=1.2V,f=500MHz.

Table 9. Variation of Power delay product (PDP) with temperature of Double-tail Dynamic comparator at ΔV_{IN} =0V.

Temp (Degrees)	Power (µW)	Delay (ps)	PDP (aJ)
0	204.50	78.848	16124.41
5	205.50	79.847	16413.34
15	205.81	80.845	16638.709
27	206.40	80.841	16685.58
36	207.59	87.839	16972.59
50	208.50	82.835	17261.15

V. CONCLUSION

It is clear that the calculated comprehensive delay, average power & PDP for comparators with dynamic bias are more performance efficient than the comparators without dynamic bias. Also, Dynamic bias based double-tail comparator is less energy efficient than dynamic bias based Elzakker's comparators. A new modeled comparator with dynamic bias reduces the power consumption by 50% with prior comparators. That results in reduction of total energy consumption of the comparator and provides the better isolation than other comparators. Hence, these are used to design SAR ADC and sense amplifiers.

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