# Static Timing Analysis and Timing Violations of Sequential Circuits

**G.Siva Priya, K.Hari Kishore, Fazal Noorbasha**

*Abstract: Designing of sequential circuits needs timing analysis at each and every stage of design process (synthesis, floor planning, placement, routing, layout design...) and comprises of three main parts-Timing checks, Constraints and Libraries. Timing checks such as setup (Ts) and hold time (Th) violation check in sequential circuits plays an important role during timing verification. This paper describes about static timing analysis mainly about reg2reg setup and holds analysis and analyses a kind of detection and correction circuits for Ts and Th violations [1] by associating a digital circuit to them.*

*Index Terms: Timing parameters, static timing analysis, additional pessimism, on-chip variations*

## I. INTRODUCTION

Sequential circuits are the major ones playing role in digital world. Without sequential circuits, no automation comes into practice. For such circuits, flip flops are the major blocks in which clock plays a key role. The relation between clock and data can modify the whole circuit as reliable or unreliable. So the timing of data with respect to time should be precise and compatible or else the circuit enters into metastable state or gives corrupted results. While designing sequential circuits, we come across different stages like logic synthesis, floor planning, placement, clock tree synthesis, routing, and layout. At every stage, timing analysis is important. Synchronous sequential circuits need precise timing parameters and violations in these specifications causes the Chip to operate with reduced frequency or totally failure of chip. Timing parameters or Specifications are setup time, hold time, clock frequency (f), skew and some other parameters Many factors effects these parameters [2] such asprocess dependent factors-etching, oxidation power supply voltage fluctuations Aging Jitter.

## II. STATIC TIMING ANALYSIS

Static Timing Analysis (STA) mainly divided into three kinds like timing checks, constraints, libraries as shown in Fig. 2.1.

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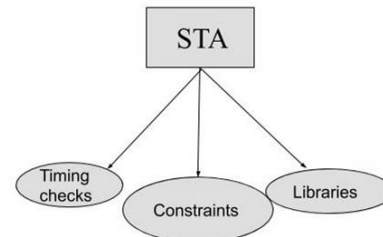


**Fig . 2.1 STA parts**

Constraints are design specifications like operating frequency whereas libraries are cells with delay models and are used to calculate delays of the cells.

### Timing Checks

For any chip before moving to fabrication stage static timing analysis is the mandatory one so that we can reduce. Timing violations. Initial level of checking/diagnosis for the chip is timing check and timing checks we do are setup time, hold time, recovery, removal, etc. Timing checks requires following terms:

i.   Timing path- valid critical path identification is important.
ii.  Arrival time
iii. Required time
iv.  Slack-min,max

*Timing path:* Path that reaches endpoint from start point where start point is of flip-flop clock pin/input port and end point is of flip-flop d pin/output ports as shown in Fig. 2.2.



**Fig . 2.2 Timing path definition**

*Arrival time (AT):* Time required reaching end point from start point and it is always calculated at end points.

*Required Time (RT):* Expected time for signal to arrive end point from start point. It defines the design needs like operating frequency.

*Slack:* Difference between arrival and required time.

Min slack/hold slack/min difference=AT-RT

Max Slack or Setup slack or max difference=RT-AT
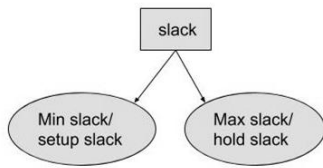
Types of slack is shown in Fig. 2.3



**Fig. 2.3 Types of slack**

From these two we have setup timing and hold timing analysis. We concern mainly about setup and hold static timing analysis. There are different types of setup and hold timing analysis. Based on the timing paths available, number of analysis varies. As shown in Fig. 2.4, we have maximum types of timing analysis.
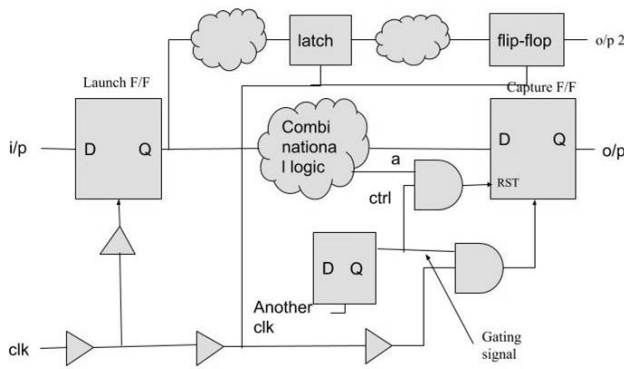


**Fig. 2.4 Sequential circuit to consider timing paths**

Types of setup/hold analysis:
1. reg2reg
2. in2reg
3. reg2out
4. in2out
5. clock gating
6. recovery/removal
7. data-to-data
8. latch(time borrowing/time given)
9. slew/transition-(data, clock)
10. load-(fan out, capacitance)
11. Clock timing-(skew, pulse width)

*Reg2reg analysis*: Timing path from launch flip-flop clock port to capture flip-flop d pin which includes two registers (flip-flops), so reg2reg.

*In2reg analysis*: path from input port to launch flip-flop d pin.

*Reg2out analysis*: path from capture flip-flop clock port to output port.

*In2out analysis*: path from input port to output port.

*Clock gating analysis*: path from another clock pin to AND gate output i.e., making the capture flip-flop as gated one by applying clock signal whenever the flip-flop is needed which reduces power consumption.

*Recovery/removal analysis*: path from another clock port to reset signal port of capture flip-flop.

*Data to data analysis*: paths from clock to a pin and another clock to control signal.

*Latch (time borrowing/time given) analysis*: In some of the sequential circuits, latches are available. If the time between clock and latch does not meet, then level of latch can be borrowed to clock period known as 'time borrowing'. If the time between latch and top flip-flop in the circuit doesn't meet, then time can be given to flip-flop from latch known as 'time given'.

*Slew/Transition analysis*: Data and clock slews are calculated as they have different signal transition timings(rise and fall times) because clock changes rapidly while data changes not often.

*Load analysis*: At each and every node ofcircuits, load values can be calculated. At loads, fan-out and capacitance values are calculated.

*Clock timing analysis*: A critical analysis of STA where skew and clock pulse width values are majorly important.

## III. DEMONSTRATION OF REG2REG SETUP/HOLD ANALYSIS WITH AN EXAMPLE

Out of all kinds of analysis, understanding of reg2reg analysis makes remaining analysis easy to understand. Now a circuit is considered and doing reg2reg setup/hold analysis [8].For this analysis, step by step process is followed.

**Step-1**: Consider a circuit as in Fig. 3.1 with known specifications like gate delays, wire delays, clock period, combinational path delay, clock-to-q delay, setup time, hold time, jitter uncertainty, required arrival time at final output port, initial signal arrival times of combinational circuit.
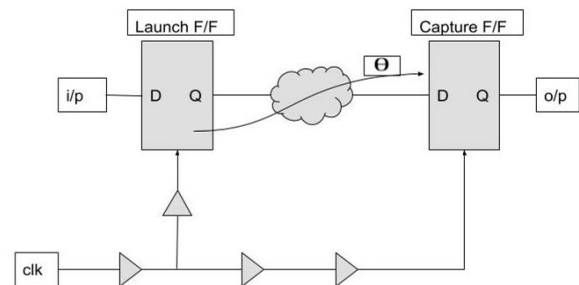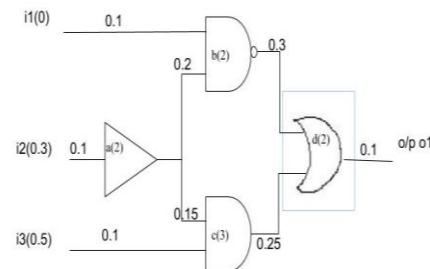


**Fig . 3.1 Sequential circuit**



**Fig. 3.2 Combinational circuit in the above sequential circuit**

Here i1(0), i2(0.3), i3(0.5) are input signals to combinational circuit and values inside them are signal arrival times from source i.e., flip-flop output, values inside gates indicate gate propagation delays and values above wires indicate wire delays, clock frequency considered here is 1GHz, so clock period=1 ns.

**Step-2**: Converting circuit into directed acyclic graph (DAG) known as timing graph where complete circuitry (all input ports, output ports, gates) is represented in nodes form as shown in Fig. 3.3
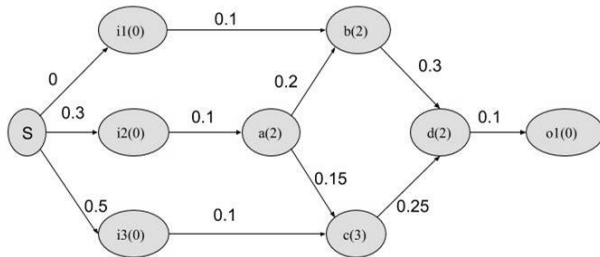


**Fig . 3.3  Timing graph**

**Step-3**: Calculation of actual arrival time (AAT)
AAT is calculated at every node by moving forward (launch flip-flop to capture flip-flop) in timing graph. It is done by adding up node delay(at which node we are calculating) and wire delay previous to that(where the signal is coming from) to previous node AAT. If a node has more than one receiving signal then worst/max/late values of all arrival times are considered as AAT.

**Step-4**: Calculation of required arrival time (RAT)
RAT is described as time at any node where we expect the latest transition in a single clock cycle; it is a requirement, specification. RAT is also calculated at every node by moving backward from capture flip-flop to launch flip-flop in timing graph. It is done by subtracting the previous node delay, wire delay from previous node RAT. If a node consists of two RATs then min/best/early value is considered.

**Step-5**: calculation of slack

Setup slack=RAT-AAT

Hold slack=AAT-RAT

Slack value should be positive or zero but should not be negative. If negative slack occurs then there is a violation, have to modify to get positive slack. At every node slack is calculated to identify which node is causing negative slack so that we can do changes to make slack value positive and this process of making positive slack is known as "Engineering Change Order"(ECO). The AAT,RAT and slack values from the timing graph is given in below table 1. Here the RAT at output port is taken as 7.55ns. All the values are considered in ns time units.

**Table 1.  Arrival times and Slack values at nodes**

| Node | AAT | RAT | Slack |
|---|---|---|---|
| S | 0 | -0.35 | -0.35 |
| i1(0) | 0 | 3.05 | 3.05 |
| i2(0) | 0.3 | -0.05 | -0.35 |
| i3(0) | 0.5 | 2.1 | 1.6 |
| a(2) | 2.4 | 2.05 | -0.35 |
| b(2) | 4.6 | 5.15 | 0.55 |
| c(3) | 5.55 | 5.2 | -0.35 |
| d(2) | 7.8 | 7.45 | -0.35 |
| o1(0) | 7.9 | 7.55 | -0.35 |

To get positive sla ck at some nodes we do path based analysis (PBA) instead of graph based analysis(GBA). GBA is nothing but the previous process we have done.In calculation of AAT if we consider min value instead of worst value then we may get positive slack, this is known as PBA.

**Step-6**: Convert pins to nodes and compute AAT, RAT and slack

For detailed and accurate timing analysis, we go for PBA. For this we make timing graph with pin node conventions. The points before gates and after gates, input, output ports are considered as pins and all these pins are converted to nodes and will make timing graph. Then computation of AAT, RAT and slack follows the same process as before.

**Step-7**: Setup and Hold analysis equation
The timing analysis equations are given for the circuit shown in Fig. 3.4
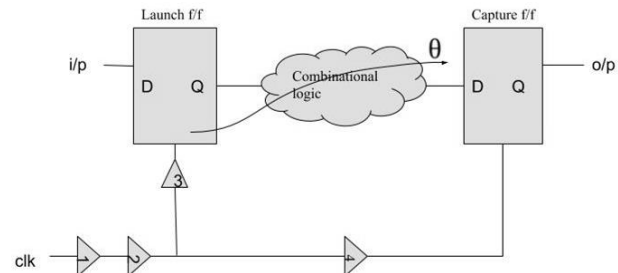


**Fig. 3.4 Circuit for setup analysis with single clock**

Setup analysis equation:
$$\theta + \Delta 1 < T + \Delta 2 - S - Su$$
Where θ =clk-to-q delay + combinational logic delay
Δ1=sum of launch F/F clock network buffer delays
=Delay of (1+2+3) buffers
T= Time period of clock
Δ2 =Sum of capture F/F clock network buffer delays
=Delays of (1+2+4) buffers
S=setup time
Su=setup uncertainty=Parameter used to model jitter.

Actual setup equation is $\theta < T$ showing that signal reaching from clock pin of launch F/F to capture F/F D pin which includes path of clock network, combinational logic, clock-to-q delay (internal delay of flip-flop) should arrive within a clock cycle. With inclusion of clock network buffers, we add those values on both sides (Δ1, Δ2). Signal should arrive within time period excluding setup time and jitter.

The left hand side equation refers to arrival time of data and right hand side refers to required time of data.

Hold analysis equation: $\theta + \Delta 1 > H + \Delta 2 + Hu$

Where H=hold time

Hu=Hold uncertainty of jitter

Equation describes that time needed to launch the data has limitation of θ >H i.e., time needed to reach the data from launch F/F clock pin to D pin of capture F/F should be at least greater than hold time.LHS side of equation refers to data arrival time and RHS side refers to data required time.

**Step-8**: Graphical to textual representation To have timing reports conversion of all the information in graphical form to textual form is needed. Textual representation of setup analysis is:

$$AT = \theta + \Delta 1$$
$$AT = \theta + b1/a + b1/y + b2/a + b2/y + b3/a + b3/y$$
$$= (0.9+0.013+0.043+0.021+0.051+0.032+0.055) \ ns$$
$$= 1.115ns$$

Where Δ1= sum of delays of buffers 1, 2, 3

$b1/a$=net delay (wire delay) of buffer 1

$b1/y$= cell delay of buffer 1

Similar indications for buffers 2 and 3.All the values above are considered values from a foundry for a circuit with known specifications for analysis purpose.

$$RT = T + \Delta 2 - S - Su$$
$$= T + b1/a + b1/y + b2/a + b2/y + b4/a + b4/y - S - Su$$
$$=(1+0.013+0.043+0.021+0.051+0.032+0.083-0.01\_0.09) \quad ns$$
$$=1.143ns$$

Slack=RT-AT=1.143-1.115=0.028ns

It shows a positive slack, so there is no setup violation. But this not the real scenario while dealing with fabricated chips. The delay values may vary depending upon on-chip variation (OCV) derates. This is due to etching and oxidation process of fabrication. For example consider OCV derates as +20%, -20%, the percentage varies from foundry to foundry and indicates that the delay values in clock network may get increased or decreased by 20%.For example a 100 ns delay value can range between 80 to 120 ns. So there will be 4ways of variation in clock network delays. Those variations are

   a) Increase of delay values in AT(Δ1 ) by 20%, increase of delay values in RT(Δ2 ) by 20%
   b) Increase of delay values in AT( Δ1 )by 20%, decrease of delay values in RT by 20%
   c) Decrease of delay values in AT( Δ1) by 20%, increase of delay values in RT( Δ2 ) by20%
   d) Decrease of delay values in AT(Δ1) by 20%, decrease of delay values in RT( Δ2 ) by20%.

Increase in delay value in clock network is termed as 'clock push-out' while decrease in delay value of clock network is termed as 'clock pull-in'. Now considering STA with OCV derates. Let us do the worst case analysis i.e., clock pull-in in RT (Δ2) so that violation arises and can eliminate it by the process of common path pessimism removal (CPPR). Δ2 values after clock pull-in which decreases delay values by 20% are

$$\Delta 2 = b1/a + b1/y + b2/a + b2/y + b4/a + b4/y$$

=0.0104+0.0344+0.0168+0.0408+0.0256+0.0664=0.01994ns
$$RT = T + \Delta 2 - S - Su$$
=(1+0.01994-0.01-0.09) ns=1.0994ns

Slack=RT-AT=1.0994-1.115=-0.0206ns

It shows negative slack which indicates setup violation. It arises because of OCV and to avoid timing violation we have to remove        additional pessimism (AP) introduced in it. In Δ1 andΔ2, we havecommon buffer delays b1 and b2.When we observe these delay values there exists different cell delay values due to OCV. In general a cell can't have two different delay values at a time. So we have to equalize it.

**Step-9**: AP removal

The difference between common path delays is termed as additional pessimism. This AP value may have get added in Δ1or lost in Δ2due to OCV. So let's add AP to   Δ2 to equalize common path delays. This addition or removal of AP to   Δ1 or Δ2 should be in such a way that $RT > AT$ to get positive slack.

$$AP = ((b1/a + b1/y + b2/a + b2/y) in\ \Delta 1) - ((b1/a + b1/y + b2/a + b2/y) in\ \Delta 2)$$
$$= 0.128\text{-}0.1024=0.0256ns$$

Addition of AP to Δ2=0.1024+0.0256=0.128ns equal to Δ1 common path delay.

RT=1.12ns

Slack=RT-AT=1.12-1.115=0.005ns= positive slack showing no violation.

Thus STA with OCV consideration before fabrication makes the chip gets fabricated without any violation. The same OCV theory and AP removal is applicable to hold analysis also. Now textual representation of hold analysis:

$$\theta + \Delta 1 > H + \Delta 2 + Hu$$
=>AT > RT
$$=> \theta + b1/a + b1/y + b2/a + b2/y + b3/a + b3/y > H + b1/a + b1/y + b2/a + b2/y + b4/a + b4/y + Hu$$
=>0.14+0.013+0.043+0.021+0.051+0.032+0.055 >
0.01+0.013+0.043+0.021+0.051+0.052+0.083+0.05
=>Slack=AT-RT=0.355-0.303=0.052ns=positive     slack
=>no    violation.

Here θ value is less compared to setup analysis because min delays are considered while computing hold analysis. Consider OCV for hold analysis and worst case for this analysis is both clock pull-in in AT and clock push-out in RT. Then Δ1and Δ2values after decrease in delay values by 20% in Δ1 and increase in delay values in Δ2 by 20%/ are:

Δ1=0.0104+0.0344+0.0168+0.0408+0.0256+0.044

Δ2=0.0156+0.0516+0.0252+0.0612+0.0384+0.0996

=>Slack=AT-RT= -.0396ns= negative    slack    indicating violation.

=>AP=0.1536-0.1024=0.0512ns

Subtracting AP in Δ2

=>RT=0.3516-0.0512=0.3004ns

=> Slack=AT-RT=0.312-0.3004=0.0116ns

It shows positive slack so that hold violation is removed after pessimism removal.

## IV. TIMING VIOLATIONS

Timing violations makes the chip entirely not to run in a proper mode of operation. From [1] detection and correction circuits for timing violations have been proposed based on timing equations analysis. To avoid violations many techniques have been proposed like adjustable delay buffers [3]-[6], time borrowing principle [7], etc. Details of detection and correction circuits are given in [1]. Mostly setup and hold time violations are seen and have to be avoided.

## V. DESIGNS, SIMULATED WAVEFORMS AND DISCUSSION

### Designs and Simulated Waveforms

Detection and correction circuits are designed in 90nm technology. Block diagram, designed circuits and waveforms are shown in following figures.
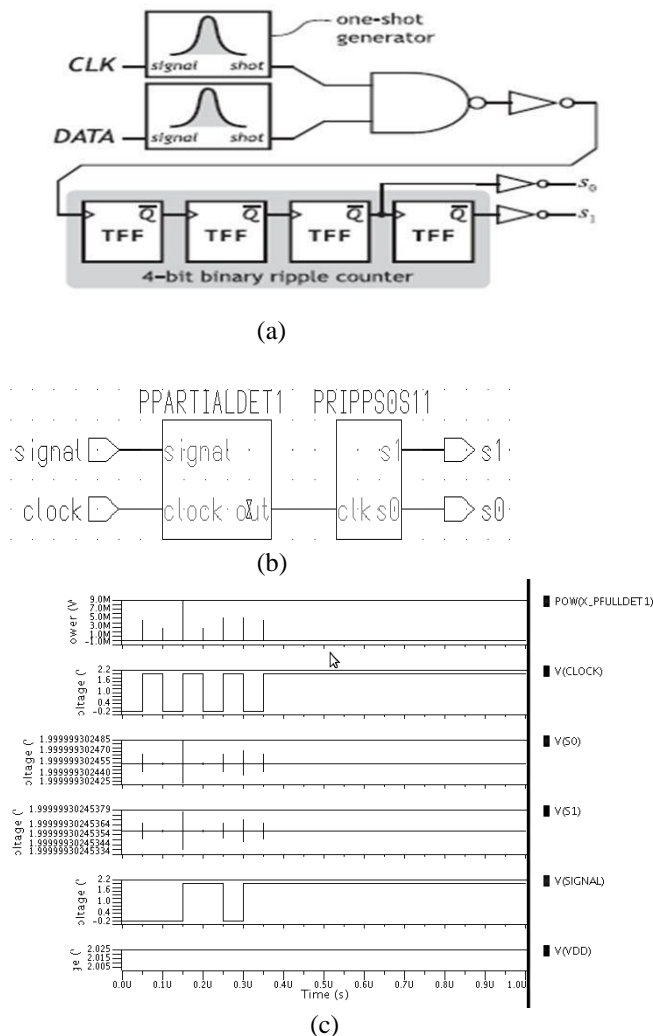


(a)



(b)



(c)

**Fig. 5.1(a), (b) and (c) represents circuit diagram, designed circuit and its simulated waveform of detection circuit**
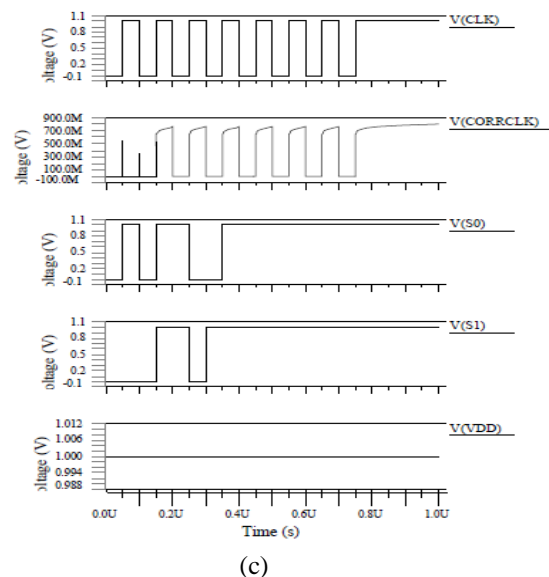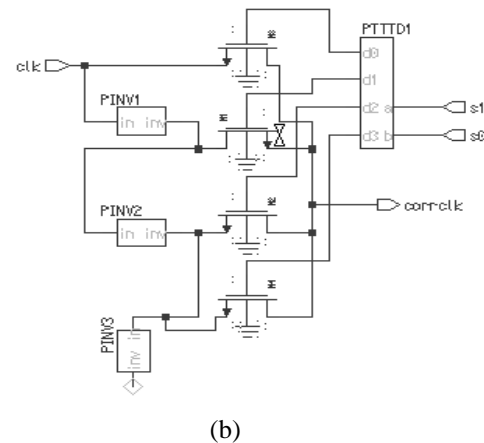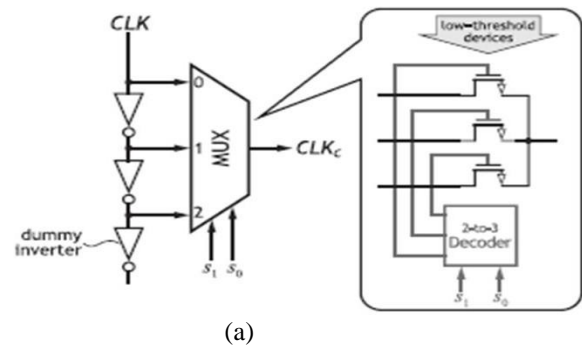


(a)



(b)



(c)

**Fig. 5.2 (a), (b) and (c) represents circuit diagram, designed circuit and simulated waveform of correction circuit**
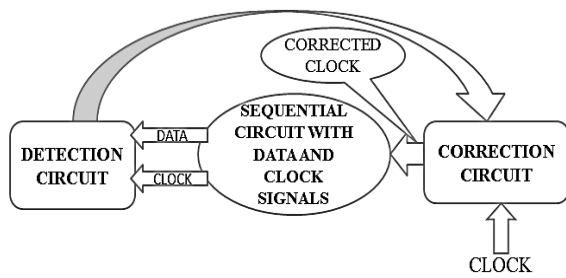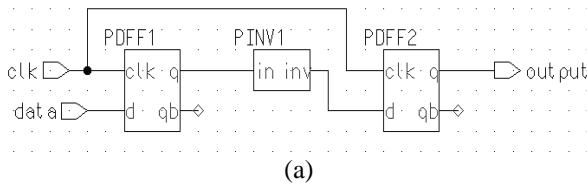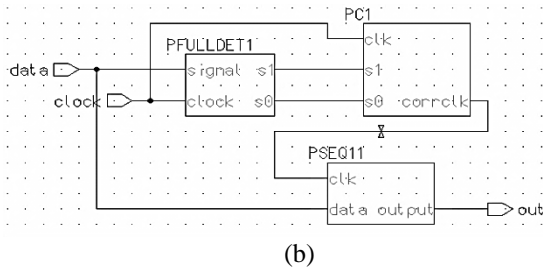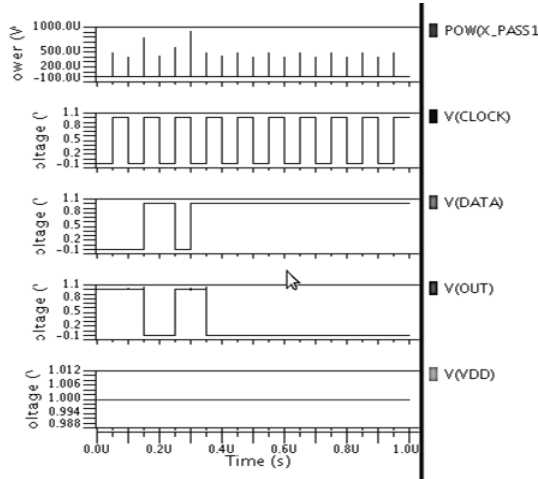
**Fig. 5.3 Block diagram of a Digital circuit associated with detection and correction circuits**
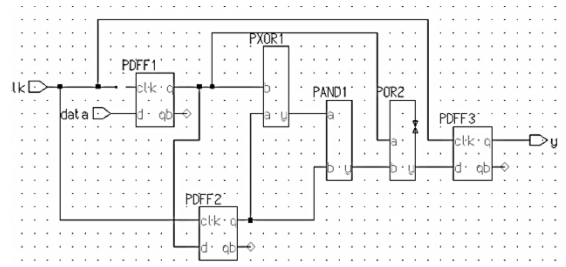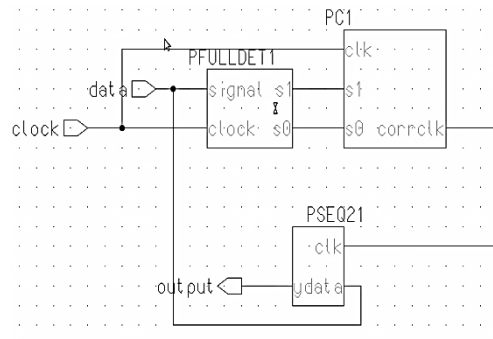


(a)



(a)



(b)



(b)



(c)

**Fig . 5.4 (a), (b) and (c) represents designs of sequential circuit, sequential circuit associated with detection and correction circuits and its waveform**
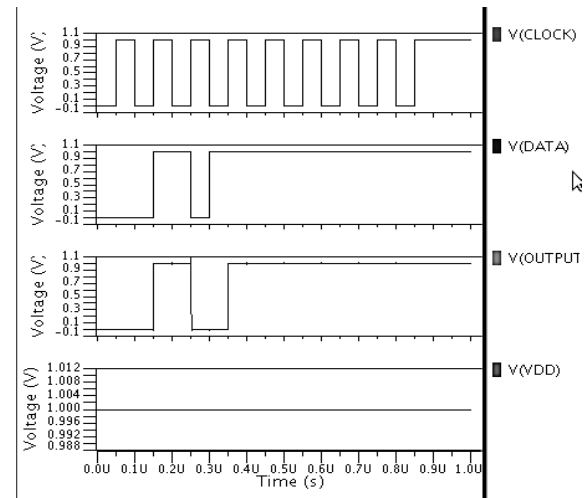


(c)

**Fig. 5.5 (a), (b) and (c) represents second sequential circuit, second sequential circuit associated with detection and correction circuits and its waveform respectively**

## VI. DISCUSSION

Detecting clock and data edges and comparing the edges and indicating it with control signals is done by detection circuit to detect violation. When there is a violation indication from detection circuit then the correction circuit modifies the clock by selecting one of the versions of clock signal so that violation gets avoided. In this paper some sequential circuits are inserted in between detection and

correction circuits to observe how the detection and correction circuits are performing. The circuit diagram, designed circuit and simulated waveform of detection circuit is shown in Fig. 5.1. The correction circuit diagram, designed circuit and simulated waveform of correction circuit are shown in Fig. 5.2. The two sequential circuits associated with detection and correction circuits are shown in figures 5.4 and 5.5 respectively. From above associated sequential circuits observation of detection and correction circuits is done. STA can be done using Open Timer software which is an open source high performance timing analysis tool, introduced by Tsung-Wei Huang [9].

## VII. CONCLUSION

In this paper reg2reg setup and hold analysis for an example circuit is described and circuits for detection and correction circuits are observed by associating sequential circuits to them. Before going to fabrication step, STA including OCV derates helps to avoid timing violations such as setup and hold time violations. Setup violation makes the chip operate under reduced frequency while hold violation makes the chip doesn't run at all. These violations make the circuit go into metastable stage.

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