Integrated Power and Clock Distribution Circuits in a Wired and Wireless Clock Network

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Abstract: Integrating power with clock distribution networks is necessary to reduce consumption of power in a system on chip(SoC). This paper presents a novel circuit which integrates power with a clock distribution network. A CMOS oscillator circuit has been designed to generate an integrated power clock signal to drive the combinational part of a circuit. A clock buffer circuit based on a schmitt trigger is developed to convert the integrated power and clock signal into a full swing signal for driving the sequential part of the circuit. The simulation results obtained for the circuit show power consumption of 2.5uW which is lesser as compared to Integrated Power and Clock Distribution circuits (IPCDN) and Globally Integrated clock and power distribution circuits. The overall power dissipation in the proposed circuit is 60.9% lower than IPCDN circuit. The frequency obtained is 5 GHz and a voltage swing of 415mV is obtained by the circuit. The proposed circuit uses only 10 transistors as compared to 18 transistors used in IPCDN circuit and helps reduce the area and the total power consumption. To send out the clock signal in a wireless manner a CMOS based On-Off Keying modulator circuit is connected to the clock buffer circuit.. This circuit converts the clock signal into a wireless signal which can then be transmitted.

Keywords: combinational, sequential, clock buffer, Differential power clock, distribution network, Low power, wireless clock.

I. INTRODUCTION

As power consumption in a integrated circuit (IC) reduces and performance increases, the complexity of the integrated circuit increases. With limited resources on-chip, design of global networks becomes very complex as these consume a major portion of available metal resources. Metal resources are majorly consumed by clock, ground and power lines in a IC. The circuits are usually designed independent of each other as each circuit exhibits characteristics which are different from each other resulting in heavy usage of on-chip resources as each circuit is connected to separate gates in an IC.

Prior research work on GIPAC[1] by Renatas Jakushokas and Eby G. Friedman in 2010 tried to merge power and clock signals globally. These merged signals were later separated from the GIPAC network into two separate signals by using passive filters. This technique of integrating power and clock signals worked as power and clock signals are fundamentally different signals. The clock signal has a high frequency component and the power signal is ideally DC, and so it is possible to separate these signals using high pass and low pass filters.

Research on IPCDN[10] by Seyed E. Esmaeili and Asim J. Al-Kahlili in 2013 tried to remove the complete CDN, both globally and locally, by integrating the power and clock distribution network.

A new investigation on hybrid wire-wireless clock distribution networks by Qian Ding, Benjamin J. Fletcher, and Terrence Mak proposes a new type of mixed wired and wireless Clock networks, which improves the performance of clock network on-chip by the use of embedded wireless clock transmitter and receiver. Here, On-Off-Keying (OOK) transceivers [11] are used for a simpler system, reduce the propagation delay and achieve significant power efficiency. A propagation delay which is around 57 times lower than a conventional H-tree. Is achieved in this system. A lower clock skew of 26.9ps (6.7% of a clock period at 2.5GHz) could be found in the proposed clock network.

II. LITERATURE SURVEY

The papers which have been published in this area have covered numerous aspects for reducing power consumption in circuits. Previous research work had focused on GIPAC[1] which tried to merge power and clock signals globally. These merged signals were later separated from the GIPAC[1] network into two separate signals by using passive filters This technique of integrating power and clock signals worked as power and clock signals are fundamentally different signals. The clock signal has a high frequency component and the power signal is ideally DC, and so it is possible to separate these signals using high pass and low pass filters

Another work investigates the feasibility of removing the entire CDN[10], globally and locally, by integrating power and clock networks. Usually, the CDN[3] contains two parts, and one of them is a clock grid driven by a global h-tree. If horizontal and vertical wires are implemented using a single metal layer each, then a clock network would need a minimum of four metal layers. If a similar number of metal layers are used for the global power network, then the entire clock and power network would use a minimum of six layers.

But if, IPCDN is used then the entire PDN and CDN distribution [2] both globally and locally, would use only four metal layers. Comparing this with usual resonant clock networks [8], where the clock signal has to achieve a full swing from 0 to V_{DD}, the signal generated in this case has a peak-to-peak voltage of 400 mV around Vdc,

In IPCDN[10], the generated signal is directly connected to the power line of sequential and combinational circuits,

and this removes the necessity of a local clock network[9] and also the need for low pass and high- pass filters. As, the voltage swing of the generated *signal* is 400 mV, it is quite low as compared to the conventional resonant clock networks. The only difference in IPCDN[10], is that a clock buffer is designed to convert the generated pwr_clk signal into a full swing clock signal so as to connect to the clock port of a sequential circuit.

A new exploration on hybrid wire-wireless clock distribution networks[11] by Qian Ding, Benjamin J. Fletcher, and Terrence Mak proposes a new type of mixed wired and wireless Clock networks, which improves the performance of clock networks on-chip by the use of embedded wireless clock transmitter and receiver. Here, On-Off-Keying (OOK) transceivers are used for a simpler system to reduce the propagation delay and achieve significant power efficiency. A propagation delay which is around 57 times lower than a conventional H-tree. is achieved in this system. A lower clock skew of 26.9ps (6.7% of a clock period at 2.5GHz) could be found in the proposed clock network.

III. METHODOLOGY

The methodology used in this paper is to use a CMOS oscillator circuit and a clock buffer based on a schmitt trigger circuit. The CMOS oscillator generates a sinusoidal signal, which is combined with a dc signal to generate a *pwr_clk* signal. The circuit in Fig 2 is an IPCDN circuit without using inverters and which can generate a power clock signal as shown in the simulation result in Fig 7. The circuit shown in Fig 1 is the transistor equivalent circuit of the CMOS oscillator. Which is the main circuit for generating the combined power clock signal. The generated signal can be used to drive the combinational part of a circuit. To drive the sequential block in a circuit , the power clock signal has to be converted into full swing clock signal. This is achieved by a clock buffer circuit which is a schmitt trigger circuit, converting the generated pwr_clk signal into a normal clock signal. To convert the obtained clock signal into a wireless one, a CMOS based on-off keying modulation circuit is connected to the designed clock buffer.
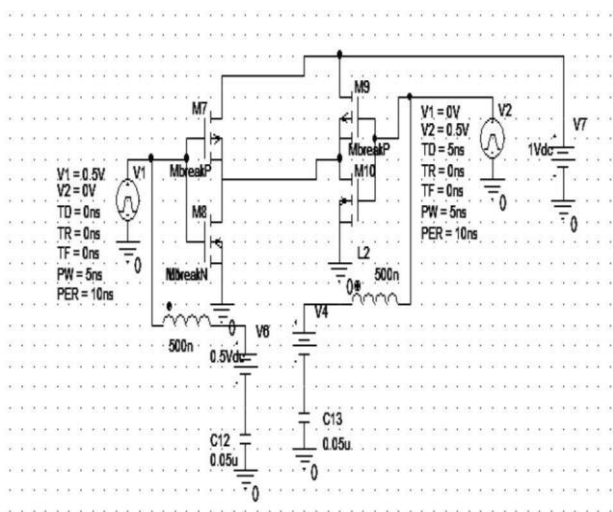

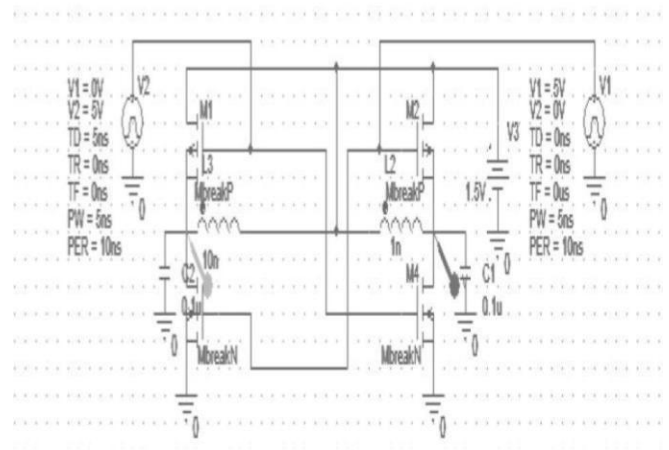**Fig. 1 Transistor based CMOS Oscillator (Proposed Circuit)**

Fig. 2 IPCDN Circuit without Inverters

IV. PROPOSED CIRCUIT

The proposed circuit is basically a CMOS oscillator which can generate a signal with a dc component and a sinusoidal swing. The proposed circuit generates a signal with a 415 mV swing, which can be used to drive a combinational circuit. Another circuit which is designed is used to convert the generated signal into a complete signal necessary to drive the sequential part of the circuit. The proposed circuit can be used to combine power and clock network signals and can be used to drive the digital part of a chip, as analog part of the circuit is vulnerable to fluctuations in power supply. The proposed circuit is as shown in Fig 1. The power consumed by the circuit is around 16.95nW. The *pwr_clk* signals generated are inverted versions of each other. The oscillation frequency generated is in the GHz range. The generated *pwr_clk* signal has amplitude of 415mV and a dc shift of 200mV and can be used to directly drive a combinational circuit, but to drive a sequential circuit, the generated signal has to be passed through a clock buffer to generate a full swing clock signal.

The generated clock signal is passed through a CMOS based On-Off Keying modulation circuit, which converts the wired signal into a wireless signal. This wireless signal can be transmitted as a wireless clock signal and can be used as a clock transmitter for globally synchronising wireless modules in a integrated circuit.
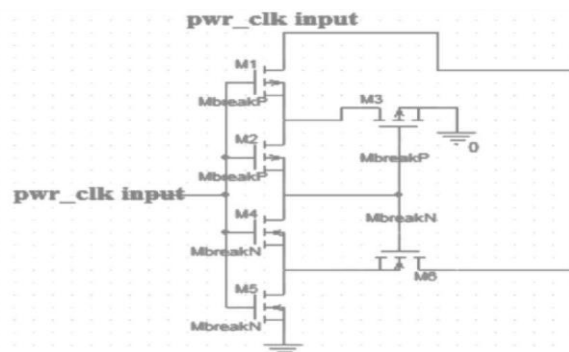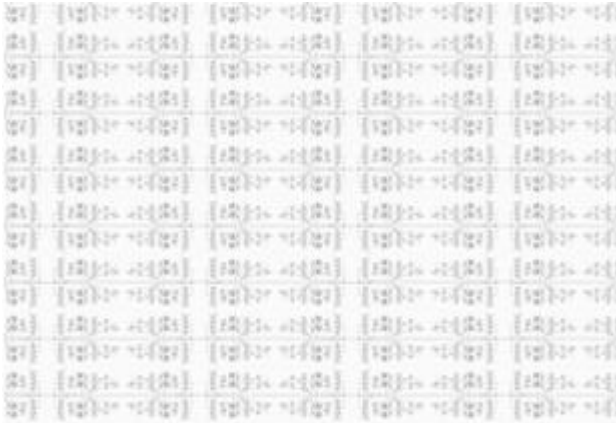

Fig. 3 Clock Buffer

Fig. 4 Clock buffer with CMOS based on-off keying modulation circuit

V. SIMULATION RESULTS

The results obtained have been simulated on SPICE CIS LITE version 17.2. Table 1 shows the comparison between proposed circuit with other methodologies for supply voltage Vdd(V) and voltage swing(mV). Fig 4 shows the circuit of a clock buffer with CMOS based on-off keying modulation circuit. Fig 5 shows a bar graph and a line graph. The line graph compares the power signal Vdd used in various methods with the proposed circuit. As shown in the line graph, the proposed circuit uses a supply voltage of 1V. The bar graph shown in Fig 5 compares the voltage swing of proposed circuit with other methodologies. As seen in the bar graph, the proposed circuit has a voltage swing of 415mV. Table 2 shows comparison of proposed circuit with other methods for power dissipation and transistor count. Fig 6 shows a bar graph which compares proposed circuit with IPCDN[10] for two different parameters, one is power dissipation and the other is the transistor count. It is evident from the graph that the proposed circuit has a lower transistor count and reduced power dissipation as compared to IPCDN[10].

The simulation output for CMOS Oscillator is shown in Fig 8, similarly the clock buffer simulation result is shown in Fig 9 and the simulation output for IPCDN without inverters is shown in Fig 10.

The simulation result for clock buffer with CMOS on-off keying modulation circuit is shown in Fig 11. Table 3 shows the comparison of power dissipation between proposed clock buffer circuit and proposed clock buffer with CMOS on-off keying modulation circuit. The bar graph shown in Fig 7 indicates the same.

Table. 1 Comparison of Voltage swing for various methods

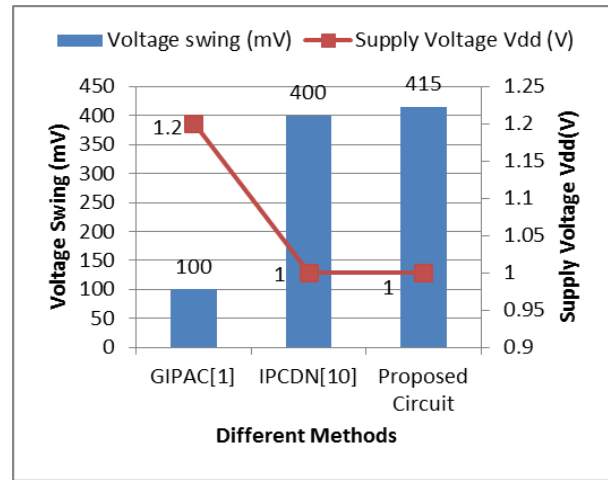| Sl.No	Methods	Voltage swing (mV)	Supply Voltage Vdd (V)
1	GIPAC[1]	100	1.2
2	IPCDN[10]	400	1
3	Proposed circuit	415	1

Fig. 5 Methods Vs Supply Voltage Vdd and Voltage Swing

Table. 2 Comparison for power dissipation and transistor count

Sl.No	Methods	Power dissipation in μW	No. of transistors
1	IPCDN[10]	6.4	18
2	Proposed circuit	2.5	10

Fig. 6 Comparison of power dissipation

Table. 3 Comparison of power dissipation for Clock buffer Vs Clock buffer with CMOS based on-off keying modulation circuit

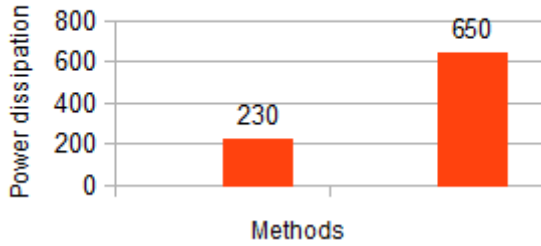| Sl.no	Methods	Power dissipation in nW
1	Proposed clock buffer	230
2	Proposed clock buffer with CMOS based on-off keying modulation circuit	650

Comparison of Power dissipation in nW

Fig. 7 Comparison of power dissipation between Proposed clock buffer Vs Proposed clock buffer with CMOS based on-off keying modulation circuit

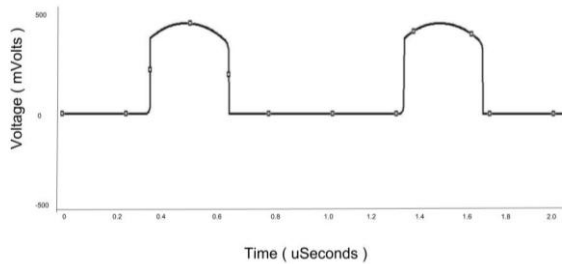**Fig. 8 Simulation result for CMOS oscillator**

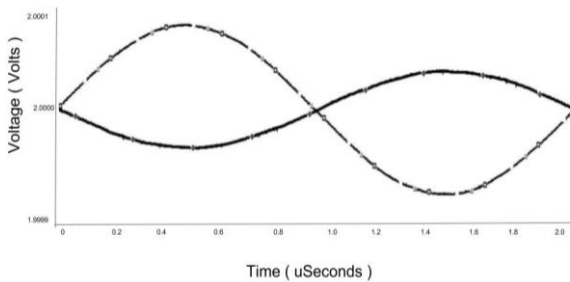**Fig. 9 Simulation result of clock buffer**

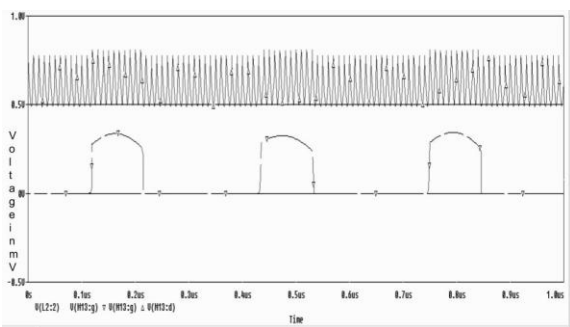**Fig. 10 Simulation result for IPCDN circuit without inverters**

Fig. 11 Simulation result for proposed clock buffer with CMOS based on-off keying modulation circuit

VI. CONCLUSION

The proposed circuit generates a combined power clock signal. Simulation results show that a signal with frequency of 5Ghz can be generated. The proposed circuit uses inductors which can increase the area, but using magnetic inductors can help reduce the overall area. The proposed circuit uses lesser area, due to the lower no of transistors used in the circuit. The voltage swing in the proposed circuit is 415 mV, which is slightly higher than IPCDN.

Comparing this circuit to IPCDN and GIPAC circuits clearly indicates that power supply Vdd used in this circuit is lower than used in GIPAC and is almost the same as in IPCDN. The overall circuit is smaller as compared to GIPAC and IPCDN. The clock buffer used in the proposed circuit also uses lesser area and lower number of transistors as compared to the clock buffer used in IPCDN. Due to the lower no of transistors being used, the proposed circuit occupies less area and there is a 60.9% reduction in total power dissipation as compared to IPCDN.

The CMOS based on-off keying modulation circuit added to the clock buffer is a way of converting the clock signal into a wireless signal which can then be transmitted globally across various modules. The frequency range of the wireless signal is 10Ghz. The power dissipation of the clock buffer with CMOS based on-off keying modulation circuit is higher, due to a more transistors being in the circuit. If the circuit can be optimised it can result in a lower power dissipation.

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