High Gain Low NF Stable Transformer Feedback Common Source LNA Design for 60 GHz Applications

Rajendra Chikkanagouda, Cyril Prasanna Raj P.

Abstract: ***This paper presents design of Transformer Feed-Back (TFB) Common Source (CS) Low Noise Amplifier (LNA)and implemented in 65 nm CMOS process parameters for operation at 60 GHz. The LNA is composed of four cascaded CS stages by utilizing gate-source TFB at the input side for input impedance matching to reduce the noise figure. The drain-source TFB is applied to the remaining stages for gain improvement, interstage and output matching. The designed LNA is simulated with Advanced Design System (ADS) and verified its functionality with respect to Noise Figure (NF), Gain, Linearity, Power dissipation and Stability. Simulated results of the proposed LNA show 23.91 dB of gain, 5.58 dB of NF and -7 dBm of IIP3 to accomplish linearity. The Figure of Merit (FoM) describes as a component of the linearity, gain and NF is 27 while drawing 15 mA from a 1.0 V supply.***

Keywords: 60 GHz, ADS, Transformer Feedback, Low Noise Amplifier, High Gain, Low NF

I. INTRODUCTION

Radio Frequency (RF) transceivers market demands communication links of higher data rate in the Industrial Scientific Medical (ISM) band at 60 GHz. RF systems operating in 60 GHz frequencies require receivers with a low Noise Figure (NF) and flat band response. The low NF, high gain, acceptable bandwidth, Figure of Merit (FoM), Stability and operation at low voltage are vital properties of LNAs that form the first subsystem in RF receiver. One of the design challenges in RF systems is selection of semiconductor technology. Microwave Integrated Circuits (MMICs) have been composed using III-V semiconductor technologies, such as Gallium Arsenide (GaAs) or Indium Phosphide [InP] reported in [1-3]. An expanding number of building blocks at 60 GHz and systems have been recently reported in SiGiBiCMOS [4-8] and CMOS technologies [9]. CMOS technology promises higher levels of integration, reduced cost, size and powerconsumption (P_{DC}). CMOS implementation also benefits from Moore's Law [9], and CMOS performance is enhancingat regular intervals, expanding its usefulness into mm-wave frequencies [19]. SiGe Heterojunction Bipolar Transistor (HBT) technology offers maximum cut-off frequency (f_T) [10]competitive with GaAs, although GaAs still offers better integration of passives and better power-handling capability. Considering the discussions reported in literature studies CMOS technology for LNA design is preferred. Millimeter-wave LNA's design in CMOS causes numerous challenges due to passive component losses and the Miller capacitance. The studies on design of LNA's using CMOS technology operating in the frequency range of 60 GHz are reported [12], [16-22], [25-28],[35]. A significant number of the earlier reported LNA's matching networks are designed with Transmission Lines (TL) which occupies moderatelymore chip area even at mm-wave band.In contrast, more area-efficient design approach can be achieved with the help of inductors (spiral). In this work design of 60 GHz LNA circuit using CMOS technology based on cascaded Common Source (CS) topology with Transformer Feed-Back (TFB) to achieve flat and broad response along with Gate-Source (G-S) and Drain-Source (D-S) circuitry for design of 4-stage CS LNA is presented. Area optimization of LNA circuitry is achieved by adopting TFB technique [9], [11], [14], [17]. Miller effect can be reduced using G-D capacitance neutralization [9], [18], [23]. Background theory, process technology and existing LNA designs are reported in section II. Designing a LNA for mm-wave applications and its simulation setup are presented in section III and section IV. Discussion on results is reported in section V. Section VI provides conclusion.

II. BACKGROUND THEORY

A. Process Technology

In this section a detailed discussion on different process technologies and various CMOS topologies for LNA design that have been considered as industry standard is reviewed. The performance of front-end units can be upgraded through Gallium-Nitride (GaN) [3] technology over the past GaAs semiconductors [2] due to its wider bandgap, greater electron mobility and good thermal conductivity which results better linearity, superior power density and low noise over a broader operating bandwidth [3].Silicon-Germanium (SiGe) technology may well start to interfere with mm-wave, however, since the transition (f_T) and maximum oscillation (f_{max}) frequencies of the most developed bipolar transistors exceed 200 GHz [4]. SiGe guarantees high levels of integration, which should lower cost and power dissipations.

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CMOS technology is exclusively responsive for its ability of integration with Intermediate Frequency (IF) and DSP functions (base-band) empowering trueSoC(Systems on Chip) [13].The Current-Voltage (I-V) characteristics become linear in sub-micron CMOS technology and hence there is an enhancement in the performance parameters such as NF, f_T, f_{max},g_m (transconductance). Be that as it may, the potential inclinations are joined by disadvantages, such as reduced breakdown voltages, subsequently decreased linearity and scaling of the metal back-end.

There are several important LNA topologies such as the Common Gate (CG), CS, Cascode, Current Reuse (CR) and Distributed amplifier topology. The cascode topology is preferred for its robustness to process variation, better isolation and high gain. It has better linearity when compared to CS and CG configurations. The minimal stability and marginally higher NF are the main disadvantages of cascode [3, 6]. The output admittance of the cascode topology is quite low in comparison to the Common-Emitter (CE) topology because it has a low capacitive component [7]. The single-stage design is inefficient in meeting the expected design trade-offs. In this design, cascaded version of CS is preferred to maximize gain and minimize NF. For LNA design, various feedback techniques such as Resistive FeedBack (RFB), Series-series FeedBack (SFB), Shunt-Series FeedBack (SSFB) and TFB are used. Generally Cascode and CS topologies without CG feedback, cannot accomplish simultaneous noise and impedance matching. At the input of the SFB LNA, the pad capacitance adds the additional resonant circuit at mm-wave frequencies. Input impedance matching and noise impedance over an extended bandwidth turns out to be more hazardous. SSFB simultaneously compensates the transistor pad capacitance and the input capacitance over a wider bandwidth [14]. Reactive feedback [11] decreases the NF, balances the gain, and sets the terminal impedances within the recommended bandwidth. Negative feedback is an alternative method to limit the terminal impedances, isolation, gain and NF. For wideband amplification, negative feedback has various advantages including gain stability over PVT variations, reduced distortion, minimum noise and impedance matching [11]. As losses are reasonably small in the transformer windings, the TFB technique contributes reduced noise [18], [21]. The gate-drain capacitance in the Field-Effect Transistor (FET) is neutralized by using TFB technique [9]. These benefits come at the cost of chip area and design complexity [21], [27].

The transformer based topology is preferred for improving noise and matching networks. CR technique is also preferred to achieve for low power. To decrease the signal loss and undesired coupling from layout point of view the GCPW) (Grounded Co-Planar Waveguide) structure is utilized [17]. Compared with the two separate inductors (gate and source), the LNA design with transformer occupies less chip area and better quality factor. By using transformer based technique,the matching network insertion loss can be minimized and improves NF. TL and inductor (lumped) are the two basic components used to model the LNA circuit [15]. The TL offers a very much characterized Electro Magnetic (EM) condition that speeds up the structure at the cost of chip area.The smaller dimensions are offered by lumped inductor but is more exposedto coupling that degrades the performance of the LNA. It requires standard EM simulations which leads to lengthy design cycle [15].

B. Existing LNA Designs

Literature review on different LNA designs with respect to process technologies, gate length and LNA topologies are discussed and summarized in the present section.

LNA circuits working in the V-band have been existing for several decades today. Bharatha Kumar et al., [8] have demonstrated 4 stage bidirectional LNA in 0.18µm SiGeBiCMOS process from (54 to 65) GHz by using transistor bias control and low-loss coplanar waveguide structures. The LNA exhibits 18.8 dB of gain, NF of 7.7 dB, P_{1dB} of -18.5 dBm and consumes 19.9 mW of power. Po-Yu Chang et al., [21] have published four cascaded CS stage LNA in 90 nm CMOS operating at 60 GHz. The LNA achieves a peak gain of 12.5 dB and a 5.4 dB of minimum noise figure (NF_{min}).TheP_{DC} of the LNA is 4.4 mW from a 1.0 V supply. Aili Wang et al. [27] developed three stage CS LNA in 65 nm LP CMOS process operating at 60 GHz. The circuit achieves a gain of 22 dB, NF of 5.5 dB and the IIP3 is -10.7 dBm operating at 61 GHz with a P_{DC} of 26 mW from a 1.2 V supply. Mizutani et al., [29] have published an optimum interstage matching inductor of a cascode amplifier in 90 nm CMOS process. LNA achieved 25.6 dB gain with NF of 6 dB, P_{1dB} -2.3 dBm and P_{DC} of 26.9 mW. S_{11} is -12 dB and S_{22} is -4 dB.J.O. Plouchart et al., [30] have demonstrated 3-stage cascode LNA implemented in a 32 nm SOI CMOS technology operating at 60 GHz exhibits a peak gain of 21dB, an average 3.3 dB NF from (53 - 62) GHz and 18 mW of P_{DC}. Di Sheng Siao [28] presented a variable gain amplifier (VGA) in standard RF 65 nm CMOS process operating from (57-66) GHz. The phase compensation is achieved by using the phase between current-steering and splitting-cascade topologies. The LNA achieve 21 dB of gain, input and output return losses are -6.5 dB and -5 dB, P_{1dB} of -4 dBm, consumes 10.9 mW power and phase variation of less than 7 °. FanyiMeng et al., [31] reported a bidirectional LNA in 65 nm CMOS technology. The Rx mode features peak gain of 21.5 dB with gain greater than17 dB over (57-67) GHz, NF of 6.7 dB, S_{11} and S_{22} are -14 dB and -8 dB with P_{DC} of 39.6 mW and FoM is 4.8. Kun-Yao Kao et al., [32] presented Variable Gain(VG) LNAwith 65 nm CMOS technology which supports 60 GHz band. The current-steering architecture provides variable gain functionality. The measured peak gain is 19.8 dB at 66 GHz, 4.3 dB of NF_{min}at 60 GHz, and P_{DC} is 28.8 mW. The return loss is greater than -10 dB. M. M. Fouad et al., [33] have demonstrated two stage LNA using TFB technique using TSMC 65 nm CMOS technology. The transformer is used to neutralize with Miller capacitance of the FET. The LNA achieves transducer gain (G_t) of 12.2 dB with NF of 4.27 dB and IIP3 is 5.6 dBm, while it consumes 30 mW from 1.2 V. Hiroyuki ShitaGuo et al., [34] proposed design of three stage TFB LNA in 65 nm CMOS technology with gain improvement and noise reduction simultaneously. LNA exhibits NF_{min} of 3.6 dB at 53.5 GHz and a highest power gain of 28.2 dB at 54 GHz, P_{1dB} of 29.4 dBm and consumes 9.8 mW of power. SuryanarayananSubramaniam et al., [35] have been demonstrated design of two-stage CS LNA in 45 nm CMOS process technology and have shown the LNA operating at 60 GHz frequency. The LNA achieves gain of 17.2 dB, NF of 2.8 dB, P_{DC} of 4.88 mW, IIP3 of -14.38 dBm and FoM of 16.1.

III. 60 GHzLNA DESIGN

The V-band LNA using 65 nm with TFB technique is depicted in Fig. 1. It employs four stage cascaded CS stages, with two different TFB configurations. For noise and input matching, Gate-Source (G-S) TFB is used at input stage. Drain-Source (D-S) TFB technique is used for achieving inter-stage and output matching with enhanced power gain from second to fourth stage.

In the current LNA design, identification of transistor geometries is carried out by considering design parameters reported in [21] and further tuning of the geometrical parameters as per desired specifications. Gain peaking which is a desired requirement is achieved by introducing the inductor at the drain of first stage, which also performs inter-stage matching. P_{DC} is reduced by minimizing parasitic capacitances and accordingly the transistor geometries are identified for M_2, M_3 and M_4. The corresponding specifications of the design are operating frequency between (57 – 65) GHz, NF less than 6 dB, gain greater than 15 dB, linearity and stability within the operating range. The LNA is modeled and parameters required to identify LNA perfomance are computed by using 65 nm Berkeley Short-channel IGFET Model (BSIM4) PTM model [35].

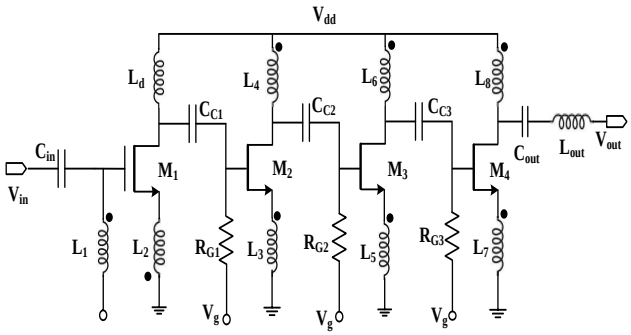

Fig.1 Circuit schematic of the proposed 60 GHz TFB LNA

In LNA design matching network of the input side plays a vital role as it greatly influences the LNA performance by gain and NF. Source degeneration is generally used to attain ideal impedances for gain (Z_{in}, opt) and NF (Z_N, opt), that eases the trade-off between parameters such as gain and NF.

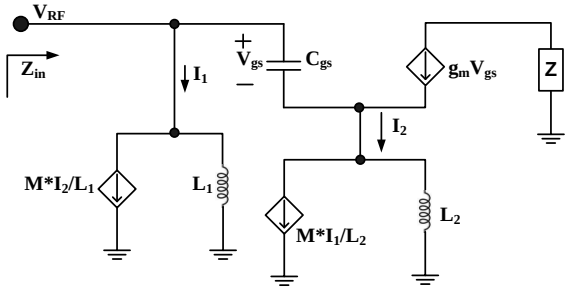

Fig. 2 First stage SSM (Small Signal Equivalent) circuit

The TFB technique used in the input stage of the LNA design not only to match the impedances but also extends the bandwidth operation [21]. The input impedance ($Z_{in}(S)$) of the LNA is calculated by using the small-signal equivalent model of the first stage as shown in Fig. 2, which is in Eq. (1) and Eq. (2).

$$Z_{in}(S) = \left(\frac{g_m.\ (k/n).(1+(k/n))+ S.\ C_{gs.}\ (1+(k/n))^2}{1+(1-k^2).S.L_2.g_m+(1-k^2).S^2.L_2.C_{gs}} + \frac{1}{SL_1}\right)^{-1} \quad (1)$$

$$Z_{in}(S) = \frac{S^3\ .\ C_{gs.}(L_1L_2-M^2)+S^2.g_m(L_1L_2-M^2)+SL_1}{S^2\ .\ C_{gs.}\ (L_1+L_2+2M)+S.g_m.(L_2+M)+1} \quad (2)$$

The transformer coupling factor is k that satisfies $M = k.\sqrt{L_1.L_2}$, where M, n and g_m are the mutual inductance, turns ratio and input transistor transconductance, the capacitance of gate to source is C_{gs}, $L_1$is the primary inductance and L_2 is the secondary inductance. The input impedances (real, imaginary) are given by Eq. (3)

$$R_e(Z_{in}) \sim \frac{1}{gm\ .((L_2/L_1)+\sqrt{L_2/L_1})} \text{and} I_m(Z_{in}) \propto$$

$$\left(1 - \omega^2 C_{gs}(L_1 + L_2 + 2M)\right) = 0 \quad (3)$$

The proportion of L_2/L_1 could be sketched to maximize g_m from smallervalue while the L_1, L_2 and their coupling are modelled to resonant with the input parasitic capacitance.

IV. LNA DESIGN PROCEDURE

In this section discussions on reverse isolation technique such as unilateralization and neutralization is presented. Discussion on designing LNA to meet parameters like gain, NF, group delay is explained.

A. LNA Unilateralization and Neutralization

The effect of C_{gd} cannot be neglected on performance of transistors with increase in operating frequency. C_{gd} adds a (non-inverting) signal path which reduces reverse isolation as well as amplifier forward gain and also decreases f_t (cut-off frequency) of the device [9] shown in Eq. (4).

$$f_t = g_m/2\pi\ (C_{gs} + C_{gd}) \quad (4)$$

The impact off_t on the input capacitance is multiplied by the Miller effect in a CS configuration shown in Eq. (5).

$$C_{eq} = C_{gd}(1 + A_v) \quad (5)$$

C_{gd}degrades amplifier performance to find alternative ways to reduce C_{gd}effects. Circuits that decrease the impact of C_{gd} are generally divided in to two groups: Unilateralization and Neutralization. Unilateralization decreases reverse signal flowand neutralization removes signal flow through C_{gd} by including additional paths. This surges S_{21} and S_{12} for a given P_{DC}, but this does not scale down the impact of C_{gd} on the input capacitance. Two examples of common unilateralization [7] techniques are cascoding of a CS-CG stage and source-coupled amplifier. Both these techniques reduces the voltage swing across C_{gd}. Miller multiplication of C_{gd} seen at the CS input and its unfavourable impacts on bandwidth are thereby decreased. For improving reverse isolation,

stability and simpler matching network two stage design is preferred, Neutralisation can be divided into differential, inductor-tuned and TFB techniques. The neutralizing capacitor C_N is used to remove the signal flow through C_{gd} in differential neutralization technique [8]. If $C_N > C_{gd}$, the differential pair drain voltages are phase shifted by 180°, the current flowing through C_N and $C_{gd}$is equal in magnitude and opposite in phase, which concludes neutralization. C_N also doubles the effective capacitance at the input and drain nodes by C_{gd}, which unfavourably affects bandwidth, gain and terminal impedances. Inductor-tuned technique uses an inductor to resonate with C_{gd}. For monolithic implementations, this technique is impractical because the inductance value is too high to be integrated.

TFB technique is the third approach used for neutralization, which proposes magnetic coupling between drain and source inductors of a CS transistor [9]. Through the transformer, feeding back a portion of the output signal helps to eliminate the feedback from output to input through C_{gd} and neutralize the amplifier. The mutual inductance and turns ratio are derived by solving equations reported in [21].

B. Selection of Transformer parameters

Transformer turns ratio and coupling factor are the important parameters to achieve C_{gd}neutralization. The ratio of coupling factor (k) and transformer turns ratio (n) should be equal to the negative sign of $C_{gs}$and C_{gd}proportion. Turns ratio of transformer should be high to maximize the gain and the value of *k* lies between -1 to +1 [18]. The mutual inductance of first to fourth stage are found to be 9.64 pH, 8.57 pH, 9.62 pH and 9.90 pH and turns ratio of the transformer is found to be 2.0 to 2.4.

C. Noise Figure

The noise factor can be expressed in Eq. (6).

$$F = 1 + \frac{R_S\gamma}{g_m}\left\{\frac{1-\omega^2 C_{gs}(L_1+L_2+2M)+j\omega L_1/R_S}{j\omega(L_1+M)}\right\}^2 \quad (6)$$

Where γ represents channel noise parameter [24]. The noise factor can be simplified under input-matching condition, expressed in Eq. (7).

$$F = 1 + \frac{\gamma}{1+n} \quad (7)$$

NF can be limited by expanding *n* as it is observed from equation (7), F is independent of frequency assuming γ is to be constant. The input matching network comprises of gate inductance (L_g) and source inductance (L_s) as TFB and input capacitance (C_{IN}) is designed to minimize the noise. For better input matching higher value of g_m is preferred, but this impacts on transistor size or P_{DC}. Additionally, the transformer quality factor and coefficient of coupling should be considered as unity.

The G-S and D-S TFB topologies are reported in [21] as G-S and D-S is used in first and subsequent stages respectively. The relationship between C_{gs}, C_{gd}, *n* and *k*can be derived as [9], [23]

$$nk = \frac{C_{gd}}{C_{gs}} \quad (8)$$

Meeting the requirements of Eq. (8), negative feedback offset and effects of Millers capacitance are reduced to achieve better gain. In practical design, C_{gd}/C_{gs}can be approximated from the transistor geometries and *k* is moderately small range (0.110–0.125).

D. Group Delay Analysis

The gain flatness and Group Delay (GD) are important factors for wideband amplifiers used to figure out the phase nonlinearity of amplifiers. In time domain signals, it is required to maintain minimum GD variationsto get non distortion amplification [30], [37]. The GD is expressed as the ratio of derivative of transfer function phase and angular frequency (ω), given by Eq. (9)

$$Group\ Delay = -\frac{\partial\emptyset(\omega)}{\partial\omega} \quad (9)$$

Where ∅ is the phase of the transfer function which is a function of angular frequency, ω.In order to reduce the GD variations, firstly, make the source and load impedance equivalent to the TL characteristic impedance. Secondly, make the signal path as short as possible in order to reduce the intrinsic transit time, which has a direct relationship with the magnitude of group delay variation and using differential transmission line instead of single-ended one is also helpful to minimize the group delay variation.

V. RESULTS AND DISCUSSIONS

LNA design carried out in previous section is modelled using schematic capture in ADS environment. ADS is well-known software for designing and optimizing microwave and RF circuits. BSIM4 technology and model files have been downloaded from predictive technology forum [41] and its parameters are brought into ADS for LNA design. The LNA design performance parameter's results such as gain, NF, IIP3, P_{1dB}, group delay and gain ripple have been obtained by performing simulation for the proposed LNA design which are shown in Fig. 3 to Fig. 8 with 65 nm technology. The TFB four stage LNA is analyzed for its gain response in the frequency range of (55-69) GHz.

A. Power Gain and Noise Figure Analysis

The optimized design of LNA in terms of maximizing gain and minimizing NF is considered along with input-output reflection coefficients. Plots of power gain (S_{21}), NF, input reflection coefficient (S_{11}) and output reflection coefficient (S_{22}) with the typical frequency are captured in Figure 3 and Figure 4. The ADS simulation results of four stage CS LNA with TFB technique has maximum gain of 24.29 dB at 63 GHz and minimum NF of 5.49 dB at 55 GHz as shown in Figure 3. There is a flat gain of 21.50 dB from (55-69) GHz.

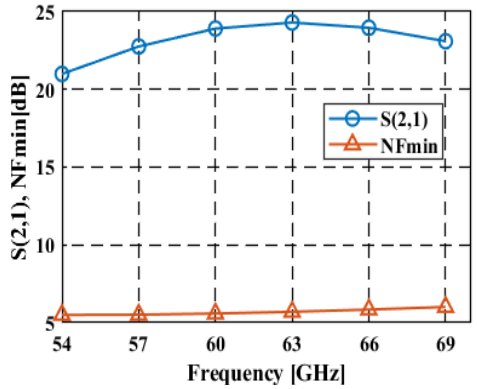

Fig.3 Gain & NF of the proposed LNA

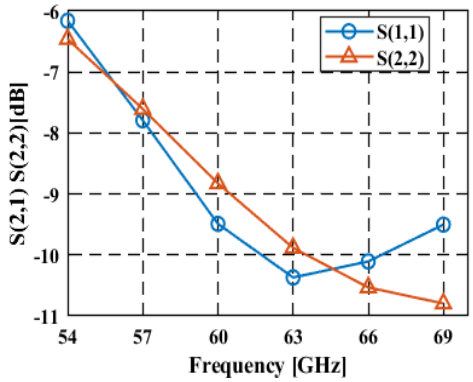

Fig. 4 S11 and S22 of the proposed LNA

The Figure 4 depicts input reflection coefficient (S_{11}) less than -8 dB from 57 GHz and -10.37 dB at 63 GHz and output reflection coefficient (S_{22}) is less than -7.6 dB and -9.88 dB at 63 GHz.

B. Phase Distortion Analysis

The group delay of the proposed LNA is shown in Figure 5 varying from 30.75 pS to 23.54 pS between (50-70) GHz frequency of operation. The Group Delay of 30.75 pS is noted down at a frequency of 60 GHz. The group delay window (Δ) is 2.1 pS for (57-65) GHz frequency range.

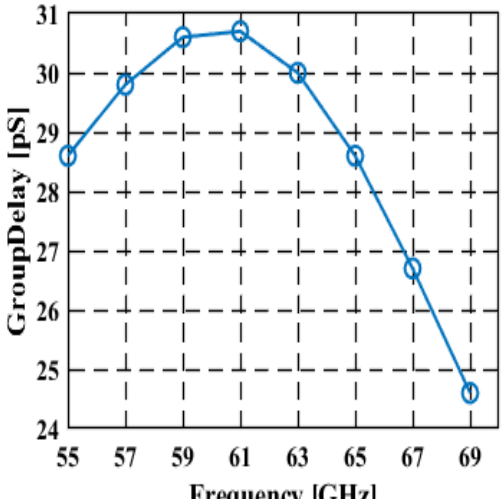

Fig. 5 Group delay of the LNA

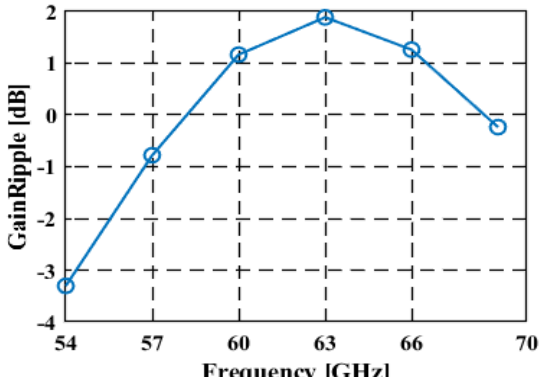

Fig. 6 Gain ripple of the LNA

In an amplifier design, the flatness is highly desired and can be achieved by controlling the ripple. The less difference between upper and lower limit of the amplitude will provide more flat band. The gain ripple of the proposed LNA is 2.67 dB between (57-69) GHz frequency of operation which is shown in Figure 6.

C. Linearity (P_{1dB} and IIP3) Analysis

Linearity is one of the most crucial factor of performance for a wireless-system, directly related to inhibitors such as spectral regrowth in both single and multi-carrier systems. Amplifiers are nonlinear, active devices. At low-power levels, the output power follows input power. At higher power levels, the amplifier's power gain starts decreasing, it enters gain compression, further increases of input power the amplifier output power saturates and no additional power results at the output. Figure 7 shows gain compression point of the LNA, two compression points are compared with respect to input power. The compression points are linear (theoretical response) and V_{out} (actual response).The V_{out}follows linear from -30 dBm to -20 dBm, 1-dB difference at -21 dBm and thereafter gain decreases with increase of input power.

Intermodulation products of higher order present in the output spectrum due to nonlinearities impacts exhibit in a LNA circuit [38]. Among the different order intermodulation products, the most disturbing one is third order because its frequency is close to the fundamental product.

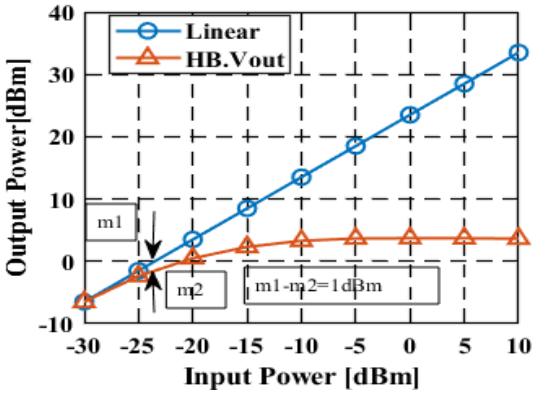

Fig. 7 P1dB of the proposed LNA

Therefore, LNA nonlinearity is widely characterized by IIP3 [39]. Two harmonics are compared with the input power. The V_{out} [1,0] (fundamental) and V_{out} [-2,1](3rd order) meets at -7 dBm of the input power. The proposed cascode LNA for 65 nm IIP3 is -7 dBm, which is better than that of the existing LNAs.

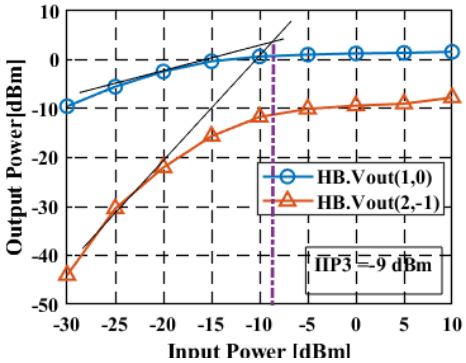

Fig. 8 IIP3of the proposed LNA

D. Stability Factor (K) and FoM Analysis

LNAs often exhibit undesired behaviour from certain input power value, which cannot be anticipated with a small-signal stability analysis. Spurious oscillations are commonly observed undesired phenomena [40]. Stability can be classified into two types. Conditional stability specifies to a network that is stable when the characteristic impedances of both input and output terminals are equal, but any mismatch on either source or load impedances that will cause it to oscillate. Unconditional stability indicates to a network that any possible impedance the amplifier should be stable. For LNA design, stability factor K is required to be satisfied as provided in Eq. (10). If the stability factor *K* is greater than one then LNA is said to be stable [36]. Figure 9 shows the stability factor *K* for the designed LNA whose value is greater than one for the entire frequency range.

$$K = \frac{1+|\Delta|^2+|S_{11}|^2-|S_{12}|^2}{2|S_{12}||S_{21}|} > 1 \qquad (10)$$

Where S_{11} and S_{22} are the input and output reflection coefficients and S_{12} is reverse isolation. The value of Δ is calculated from S-parameters which is $\Delta = |S_{11}|.|S_{22}| - |S_{12}|.|S_{21}|$. The FoMdepictsas acomponent of the Gain, NF, P_{DC} and linearity is 27 [40].

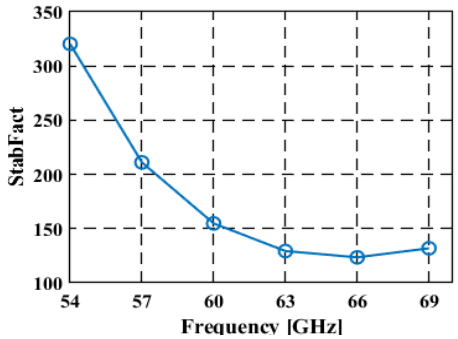

Fig. 9LNA Stability Factor

E. Gain and NF versus Gate Voltage (V_{GS}) Analysis

The analysis of gain and NF results with different gate to source voltages (V_{GS}) is performed which is depicted in Figure 10. The V_{GS} of the MOSFET is found to vary from 0.5 V to 1.0 V at 60 GHz operation. The maximum gain of the LNA is found to be 23.91 dB and NF of 5.59 dB at 60 GHz. The V_{GS} of the MOSFET is found to vary from 0.7 V to 1.0 V to achieve S_{21} between 23.12 dB to 13.96 dB and NF between 6.04 dB to 8.65 dB. The gain decreases and NF increases by increasing the V_{GS}. The maximum gain and minimum NF values are obtained at 0.6 V of V_{GS} amplifier MOSFET.

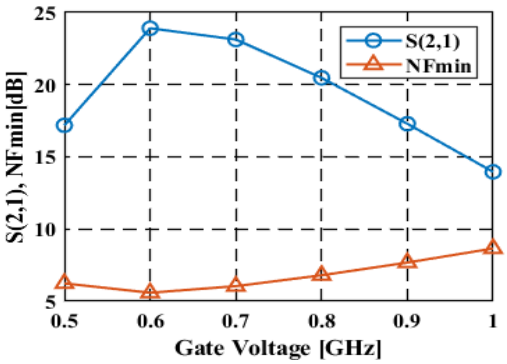

Fig. 10Gain and NF versus VGS of LNA

F. Gain and NF versus Supply Voltage (V_{DD}) Analysis

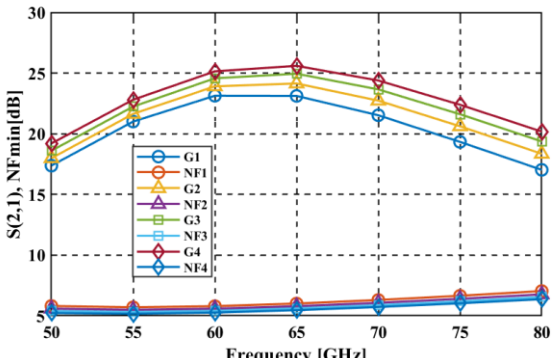

Fig. 11 Gain and NF versus frequency for different VDD

Figure 11 shows the gain and NF analysis by varying V_{DD} of the LNA. G1 and NF1 stands for simulation is carried out at the supply voltage of 0.9 V. Similar results are obtained for 1.0V, 1.1V and 1.2V supply voltage. The maximum gain of 25.14 dB and $NF_{min}$of 5.26 dB are obtained at 60 GHz with 1.2 V bias supply voltage. Similarly themaximum gain of 23.13 dB and $NF_{min}$of 5.79 dB are obtained at 60 GHz with 0.9 V supply voltage and S_{21} of 23.90 dB with NF_{min} of 5.58 dB are obtained for optimum value of 1.0 V supply for the proposed design. A Similar work has been carried out and published in [36].

The major recommendations for the design of LNA with the analysis is present in Table I. Stage - 1 of LNA is to be designed to meet NF_{min} and input matching. Stage - 2, 3 and 4 need to be designed by considering gain improvement.

The gain is increased from first stage to second stage by a factor of 323%, from second stage to third stage by a factor of 181 % and from third stage to fourth stage by a factor of 143 %. NF is increased by factors of 18%, 3.43 % and 0.89 %. Similarly P_{1dB} decreased by factors of 375%, 25 % and 5%. Group delay increased by a factors of 198% in first stage, 65 % in third stage and decreased by a factor of 81 % in second stage. Gain ripple is decreased by factors of 18% from first stage to second stage and increased by a factor of 73% from third stage to fourth stage.

Table I. Simulated Results for each Stage

Stage	**1**	**2**	**3**	**4**
S_{21} [dB]	2.75	8.89	16.12	23.91
NF [dB]	4.5	5.34	5.53	5.58
S_{11}[dB]	-5.86	-8.41	-9.35	-9.50
S_{22}[dB]	-4.77	-1.50	-1.00	-8.82
Group Delay [pS] (50-69 GHz)	1.16	2.30	1.27	2.10
Gain Ripple [dB]@ 60 GHz	0.073	0.06	1.53	2.66
P_{1dB} [dBm]	-4	-15	-20	-21
Stab. Fact(K)	>2	>4	>10	>100

Table II presents a comparison chart of various 60 GHz LNAs. The proposed LNA presented achieves the highest gain, FoM andNF_{min}against previously reported LNAs. The results indicate that the gain is improved by a factor of 11.20% and NF is improved by a factor of 35.18%.

Table II: Performance summary and comparison with the state-of-theart

Parameters	**[21]**	**[31]**	**[35]**	This Work
Technology	90-nm CMOS	65-nm CMOS	45-nm CMOS	**65-nm CMOS**
Year	2012	2016	2017	**2018**
Topology	4-Stage CS-TFB	4-Stage Cascode	2-Stage CS	**4-Stage CS-TFB**
Supply [V]	1.0	1.8	1.0	**1.0**
Frequency [GHz]	57	65.5	60	**60**
Gain [dB]	12.5	21.5	17.2	**23.91**
NF [dB]	5.4-6.5	6.7	2.8	**5.58**
S_{11} [dB]	-12	<7.0	N.A	**-9.50**
S_{22} [dB]	-30	N.A	N.A	**-8.52**
IIP3 [dBm]	-7.0	N.A	-14.38	**-7.0**
P_{1dB} [dBm]	-16.0	N.A	+4.0	**-21.0**
P_{DC} [mW]	4.4	39.6	4.88	**15**
FoM	18.7	4.8	N.A	**27**

VI. CONCLUSION

For LNA design operating in high frequency region greater than 60 GHz, CMOS technology is preferred over all other technologies such as GaN, GaAs and SiGe. In this work four stage CS LNA with TFB topology is designed considering 65 nm CMOS technology. Neutralization technique is adopted toreduce Millers effect. With TFB technique adopted for LNAdesign bandwidth extension is achieved. The inductors required for TFB can be designed using spiral inductors hence reducing area requirement. The simulation results demonstrated that the designed LNA is suitable for 60 GHz frequency band of (58–64) GHz with highest gain of 23.91 dB, FoM of 27 NF of 5.58 dBand IIP3 of -7 dBm with excellent linearity.

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