Analysis and Design of 90 nm CMOS Amplifier for UWB Applications

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Abstract*: An ultra-wideband Low Noise Amplifier (LNA) employing a Common Gate (CG) topology with load network including dual resonance is presented. This LNA has both flat Noise Figure (NF) and wideband input matching in 3.1 GHz-10.6 GHz frequency range applications. The frequency response of common gate-common source cascade topology is improved by adopting inductive series peaking technique. The proposed LNA presents 19.11 dB peak power gain at 9 GHz, 17.94 dB gain for the (4.5-9.5) GHz frequency range and 50 Ohm good enough input matching in the desired band by importing 90 nm CMOS process and model parameters to Advanced Design System (ADS) software. A fine NF less than 2.88 dB is attained in (3.1-10.6) GHz frequency range with 9 mW power dissipation from 1.2 V supply voltage. The input-output reflection coefficients (S_{11}-S_{22}) are -17.61 dB and -6.22 dB at 9 GHz respectively. The reverse isolations (S_{12}) below -50 dB is achieved.

Index Terms*: Asymmetric T-coil, Bridged shunt series, Common Gate, Common Source, Low Noise Amplifier, Series Peaking, Ultra-wideband.

I. INTRODUCTION

In recent years, model of Radio Frequency Integrated Circuits (RFIC) with CMOS process have become more popular as this technology is low cost and consistent with System-On-Chip (SoC) [1]-[9]. The Low Noise Amplifier (LNA) is an essential section in the front end of an Ultra-Wideband (UWB) RF receiver which receives weak signals from (3.1–10.6) GHz frequency range and enhances the power gain with an excellent Signal-to-Noise Ratio (SNR). Adding to it, flat-high power gain, favorable impedance matching, input-output (i.e., low S_{11} and S_{22}) and low Noise Figure (NF) performance over the entire UWB are required. In recent times, quite a few first-rate CMOS UWB LNAs have been reported in [1]–[4]. To quote an example, in [8] a reconfigurable, inductor-less, wideband with complementary Current-Reuse (CR) Common Source (CS) topology, joined with a less-current active feedback LNA is reported. Input devices used in PMOS and NMOS transistors in Common-Gate (CG) LNA are present in a complementary CR structure. This is available along with active shunt-feedback structure to enhance the current efficiency to a greater extent, reported in [11]. A two-stage LNA reported in [15] uses current-reuse technique pursued with a cascode stage in 90 nm CMOS process technology. Despite the fact that low power utilization is accomplished and NF is not acceptable. The NF and dc power consumption (P_D) exhibit a slight lower values in a single-stage cascode LNA demonstrated in [16] using 0.13 µm CMOS technology. In [14], an input matching network for wideband with dual-RLC-branch is adopted in a two stage CMOS LNA. The LNA occupies large chip area as 5 inductors are included in the design with expensive power dessipation. To minimize the power dissipation P_D of the LNA in [14], a method of self-forward body bias and forward combining techniques are described in [6]. The disadvantages incorporate seven inductors altogether and degraded NF.

Distributed Amplifier (DA) topology can afford high-flat gain and wideband input matching, but high power utilization and moderately considerable chip area as the discomforts when used in UWB applications [5]. The LNA reported in [6] incorporated RC feedback technique to reach admissible broadband matching and flat gain. Unfortunately, it cannot fulfil the prerequisites of large gain and minimum NF at low power. The two-stage UWB LNA is implemented in [7] by using reactive feedback topology to enhance the circuit execution capability in (3-11) GHz frequency range. The increased space bound by the transformer-feedback technique circuit is a detriment for the total chip volume. The conquer approach in alignment of gain and noise performance for narrowband applications is the inductive degenerated CS amplifier [17]. A speculation of this circuit for wideband applications is accomplished by substituting gate inductor with multiple reactive networks, in order that the wide-ranging reactance occurring at input side resonates throughout a large frequency range [15][17]. Such viewpoint experiences the large group-delay variations caused because of presence of more resonances at the input side of the matching network for UWB as an obstacle. Additionally, it expects medium to wide silicon region and presents a massive insertion-loss which attenuates the amplifier power gain and NF.

II. LITERATURE REVIEW

Literature review on different LNA designs with respect to process technologies, gate length and LNA topologies are discussed and summarized in Table I

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Table I. Literature review on various LNA Topologies and Technologies

Ref. No	Year	Tech/L(nm)	Topology/ Stages	Freq. [GHz]	S_{21} [dB]	NF [dB]	S_{11} [dB]	S_{22} [dB]	IIP3 dBm	P_{1dB} dBm	P_{DC} [mW]	FoM
[8]	Marcelo De Souza 2017	CMOS/130	CR-CS AFB	0.1-2.1	19.2	2.4	---	---	8.6	---	3.11	35.1
[9]	Nan Li 2017	CMOS/130	CG	3-12	13.5	4.3	<-11	---	-7	----	8.5	3.41
[10]	Mahdi Parvizi 2016	CMOS/130	CG	0.1-2.2	12.3	4.9	<-9	<-10	-10	---	0.4	17.9
[11]	Mahdi Parvizi 2015	CMOS/90	CR-resistive shunt FB	0.1-7.0	12.6	5.5	---	---	-9	-18	0.75	20.89
[12]	Meng-Ting Hsu 2014	CMOS/180	Cascode	3.1-10.6	10.8	5.5	-8.1	<-9.5	-6.4	---	6.4	5.1
[13]	K. Yousef 2014	CMOS/180	CR-CS	3.1-10.6	12.25	3.8	<-10	<-8.2	2.5	-7	18	---
[14]	Chia-Hsing Wu 2012	CMOS/180	CR cascode	3.1-10.6	12.52	2.87	---	---	-6.5	-16	11.8	4.4
[15]	G. Sapone 2011	CMOS/90	CR cascode	7.6	12.5	3-7	-9	---	---	-12	7.2	---
[16]	Giang D. Nguyen 2008	CMOS/ 130	Cascode	2.2-9.0	11.3	3.9-4.6	<-9	---	<5	---	30	---
[17]	Andrea Bevilacqua 2004	CMOS/180	Cascode	3.1-10.6	9.3	4	-9.9	---	-6.7	---	9	---

Marcelo De Souza [8] demonstrated current reuse CS LNA in CMOS 0.13 µm echnology. This architecture is grounded on a complementary CR-CS technique along with a low-current active feedback for multi-standard applications. The LNA reaches 2 dB minimum NF (NF_{min}), 21.1 dB of voltage gain, 14.3 dBm of IIP3 and power consumption of 7 mW. The amplifier draws 1.5 mw power in low power mode while providing 2.6 dB of NF, 21 dB of power gain and 4.7 dBm of IIP3. Nan Li [9] has reported an ultra-wideband LNA in 130 nm CMOS technology. The dual resonance and broadband input matching. Addition of series peaking inductor to CG-CS topology favors the extension of frequency response. The flat-high power gain of (13.5±1.5) dB with input return loss 13 dB and 4.3 dB ±0.4 dB of flat NF are obtained in (3-12) GHz frequency band. The die area of 1.09x0.8 mm^2 is occupied by the fabricated LNA including pads and circuit draws a 8.5 mW power 1.2V supply. Mahdi Parvizi [10][11] presented the CG low-noise amplifier design in 130 nm IBM CMOS technology. In this LNA design, the complementary CR architecture adapts PMOS and NMOS transistors as input devices. The LNA has measured results of gain 12.3 dB, 4.9 dB of NF_{min}, (IIP3) of -10 dBm, less than 9 dB of S_{11}, S_{22} is below -10 dB while drawing only 400 µA from a 1V power supply. The same team has published an ultra-low power LNA in 90 nm CMOS process with CR-series inductive peaking technique in 2015. The results demonstrate 12.6 dB of voltage gain, 5.5 dB of NF, -9 dBm of IIP3 and -18 dB of P_{1dB} in (0.1-7) GHz bandwidth. Meng-Ting Hsu et. al., [12] proposed a RC-feedback and FBB technique cascode LNA using 0.18 µm TSMC CMOS technology for (3.1-10.6) GHz frequency range. The measurement results exhibit 10.8 dB maximum power gain (S_{21}). The input reflection coefficient, S_{11} is less than -80.1 dB, output reflection coefficient, S_{22} is smaller than -9.5 dB. A NF_{min} of 5.5 dB, -6.4 dBm of IIP3 and 6.4 mW power dissipation from 1.1 V supply voltage have been obtained. K. Yousef et. al.,[13] demonstrated the design of CS based CR LNA for UWB functions in 0.18 µm CMOS technique with limited variations in group delay and optimized noise performance. Through this structure 12.25 dB flat gain with less than 3.8 dB NF are attained along with ±25 ps group delay variation using 0.18 µm CMOS technology. The wideband matching for input side is fulfilled by implementing the poor resistive-capacitive shunt feedback approach. The optimum group delay variations are obtained by terminating the output stage with resistor and series peaking element. The measured results of LNA include 2.5 dBm and -7.0 dBm of IIP3 and 1dB compression point (P_{1dB}) respectively at 5.5 GHz. Chia-Hsing Wu et al., [14] has described CR cascode 0.18 µm CMOS technology LNA for UWB functions with superlative linearity property (±15.8 ps variation of group delay). The LNA exhibits 11.8 mW of power dissipation, 10.2 dB input return loss, a flat-high gain of (12.52 ± 0.81) dB and (2.87 ± 0.19) dB of low-flat NF over the complete UWB frequency range. The third order intercept point and 1 dB compression point results are 6.5 dBm and 16 dBm respectively, at a frequency of 6 GHz.

G. Sapone et al., [15] has developed 2 stage single ended LNA in 90 nm CMOS technology for UWB applications. The input matching at the first stage is established with CR topology for (3-10) GHz frequencies. A resonant loaded cascode amplifier is used at the second phase to enhance reverse isolation and power gain. Measurement results indicate 12.5 dB of power gain at 7.6 GHz 3 dB bandwidth, 3 dB of NF_{min}, a reverse isolation finer than

45 dB up till 10.6 GHz, 12 ps of group delay variation and consumes 6 mA from 1.2 V power supply. Giang D. Nguyen et al., [16] implemented LNA using 130 nm CMOS technology. The architecture provides 11.3 dB gain, (3.9-4.6) dB of NF and (3.2 – 5) dBm of IIP3 over a 3 dB bandwidth at (2.2-9) GHz with 30 mW power consumption from a 1.2 V supply. Andrea Bevilacqua et al., [17] demonstrated 180 nm CMOS LNA. The amplifier exhibits a 9.3 dB power gain with S_{11} of -9.9 dB over the bandwidth, 4 dB of NF_{min} and 6.7 dBm of IIP3 while consuming 9 mW power.

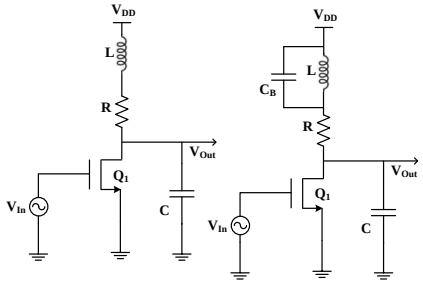
III. LIMITATIONS OF WIDE-BAND AMPLIFIER

A wide-band amplifier be required to adhere near-consistent power gain and phase linearity over its frequency of interest. The bandwidth prerequisites of wideband amplifiers are constantly developed for higher step forward environment systems. While device scaling constantly decreasing to adapt faster transistors near upper cutoff frequencies, it is even demand to improve the bandwidth of amplifiers using various techniques which empower us to do as such for a particular process technology. There are various approaches have been developed to enhance the bandwidth of the amplifiers in recent decades [18][19][22]. An advancement in the amplifier radio bandwidth is often accompanied by an analogous fall in its lower-frequency voltage gain. There are couple of mechanisms to broaden the amplifier bandwidth. These methods are described in detail in this section.

A. Bridged Shunt Peaking

In bridged shunt peaking method, bandwidth extension is accomplished by shunt peaking approach in which an inductor is in sequence with resistive load shunts the capacitor C connected at the output terminal (Fig. 1(a)).

$$Z(s)_\delta = \frac{V_{Out}}{V_{In}} = \frac{R+sL}{1+sRC+s^2LC} \quad (1)$$



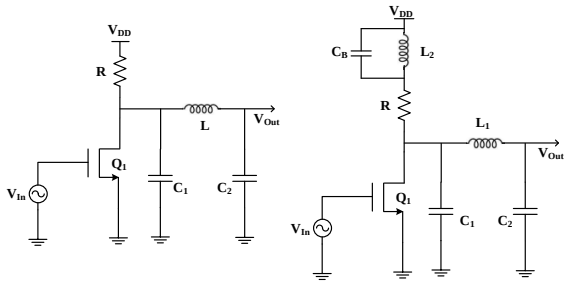
(a) (b)

Fig. 1: CS amplifier (a) shunt peaking approach. (b) bridged-shunt peaking method [20]

The -3 dB bandwidth is extended when inductor presents a zero in equation (1) that enhances the impedance with frequency and coordinates the declining impedance of capacitor. But additionally it results to peaking in the response. Subsequently, a few methods are required to exclude peaking with full-scale Bandwidth Extension Ratio (BWER). One drive is to add parallel combination of inductor and capacitor that must be adequate to deny peaking but compact enough to not substantially modify the gain performance.

B. Bridged-Shunt-Series Peaking

In this approach, an inductor is added to split the capacitor present at the load into two essential components as part of capacitive splitting function to achieve significant BWER where in drain parasitic capacitance C_1 is very much important, Fig. 2 (a). The response of the amplifier provides the additional bandwidth extension by capacitive dividing action. The transistor charges $C= C_1 + C_2$ when inductor is not connected, but with incorporating inductor L_1, initially capacitor C_1 is charged as L_1 delays flow of current to the remaining portion of the network. This step down the rise time at the drain and widens the bandwidth [21]. So that the combination of bridged shunt with inductive peaking approach and capacitive splitting of series peaked circuit provides the bridged-shunt-series-peaked network as shown in Fig. 2 (b).



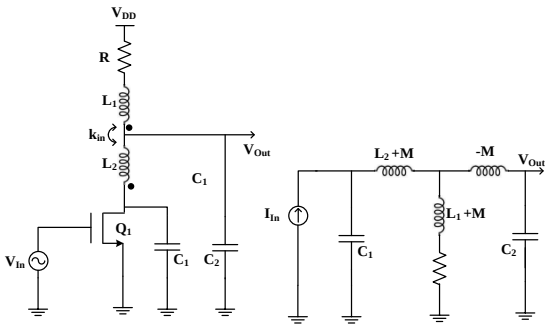
(a) (b)

Fig. 2: A CS amplifier with parasitic capacitance at drain terminal (a) Circuit coupled with series peaking. (b) Bridged-shunt-series peaked network [20].

C. Asymmetric T-Coil Peaking

A method of bridged-shunt-series peaked network provides large BWER with a parasitic capacitance ratio, $k_C > 0.3$ ($k_C = \frac{C_1}{C}$). However, as the increased value of load capacitance ($k_c \leq 0.3$) a large BWER is achieved, but the combined action of capacitive splitting of L_2 and coupling of C_B turn into powerless. This restriction is overcome by the transformer magnetic coupling force. In the asymmetric T-coil-peaked circuit amplifier ($L_1 \neq L_2$) [23] [Fig. 3(a)], a negative mutual inductance is accomplished by wounded coils. The secondary of inductor L_2 supports capacitive splitting to allow initial charging through C_1, similar bridged-shunt-series peaked amplifier. Later, the current starts to flow in L_2 and then to C_2. In view of series connection of capacitor C_2 in addition to negative mutual inductance (-M) element of the T-coil there is an initial boost in the current flow to C_2 due to the negative coupling action. This action grants an enhancement in rise time and in turn BWER. Fig. 3(b) shows the T-model of the transformer with small signal equivalent circuit. The relationship between coefficient of coupling (k_m) and the mutual inductance (M) is given as,

$$k_m = M/\sqrt{L_1 L_2}.$$



(a) (b)

Fig. 3: A method of asymmetric T-coil peaking (a) Drain parasitic capacitive circuit (b) Equivalent circuit with a T-model of the transformer.

IV. UWB LNA CIRCUIT DESIGN

The Fig. 4 shows the designed wide-band LNA. It comprises two stages utilizing CG cascade (Q_1) and cascade of Q_2 and Q_4. To accommodate transformation of output impedance source follower buffer (Q_4 and Q_5) is used. The small-signal equivalent circuit of CG with the cascade for wideband matching at input is presented in Fig. 5. The impedance at the input side is given by equation (2).

$$Z_{in}(s) = (C_{gs1} \| L_s) \| \left\{ \frac{1}{g_{m1}} \left[1 + \frac{Z_{L(S)}}{r_{ds}} \right] \right\} \qquad (2)$$

Where g_{m1} is trans-conductance of Q_1, r_{ds} is the output resistance of Q_1. The capacitance C_{gs1} adds the parasitic capacitance between gate and source of transistor Q_1 and an inductor L_S is connected to source of Q_1. C_{D1} and Z_L represent parasitic capacitance and load impedance at the drain of Q_1 respectively including C_{gs2} of the following cascade stage. Channel length modulation in nanoscale CMOS technologies causes shortened channel resistance r_{ds}; from (2), the input impedance Z_{in} turns into a strong function of Z_L.

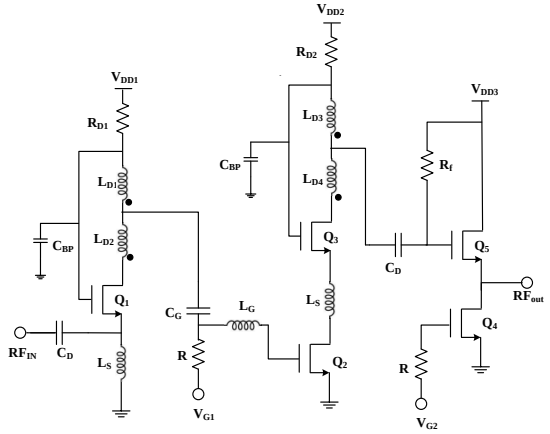


Fig. 4: Schematic of the proposed LNA

The dual-resonance load network provides the good impedance matching over the wideband range as shown in Fig. 5. For low and high frequencies two resonances are introduced. The C_{gs2} presents a high impedance path ($L_{D1} \| L_{D2} \| C_{D1}$) at the output and at the input, C_{gs1} and L_S are resonated simultaneously, selecting less resonance frequency $\omega_{o,\,low}$.

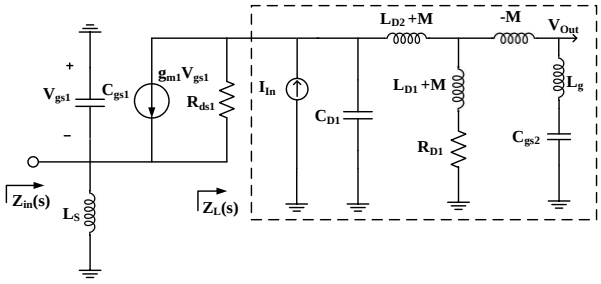


Fig. 5: The CG stage small signal equivalent circuit with load network at the drain of M_1

The overall inductance is reduced by the shunt connection of L_G-C_{gs2} and L_{D1}, resulting to high resonance frequency $\omega_{o,\,high}$. Several factors are involved in designing the asymmetric T-coils. Remarkably, the essential magnetic coupling ratio k_m (0.3-0.7) is moderately low, which normally prohibits interleaved T-coil arrangement [24]. The design complexity issues of a symmetric coil can be avoided at the cost of required non-unity turns ratio. Ultimately, architectures which limit parasitic impacts between windings are attractive. The first CG stage of the LNA exhibits the dominated NF given by the equation (3).

$$NF = 1 + \left(\frac{\gamma}{\alpha}\right) + \left(\frac{r_{ds}}{r_{ds} + Z_L(s)}\right) \qquad (3)$$

where $\alpha = g_m/g_{d0}$ is transistor trans-conductance to the channel conductance ratio at zero V_{DS} and the channel thermal noise coefficient is γ. The increase in load impedance $Z_L(s)$ for given r_{ds}, the NF is reduced as depicted in equation (3). It is required to have a load network with high impedance over wide range of frequency to achieve low and flat NF. In the present circuit structure, the load network provides large impedance over the wideband by presenting dual resonances at low and high frequencies. Conventional circuit design provides a non-flat response of NF with large value at low and high band and smaller value in the middle band independently. On the contradictory, a response of flat NF can be attained by adopting dual-resonant circuit over the total range of frequency. The approach of CG stage (Q_1) and cascade stage (Q_2 and Q_3) united with asymmetric T-Coil peaking bandwidth extension technique presented in [20] is applied to attain wide band and flat gain response. The capacitive splitting function of L_{D2} allows the initial charging current to flow only to drain to source capacitance C_{ds}. Next the current set-ups to flow in L_{D2} and proceed to C_{gs}. As the series connection of load capacitor C_{gs} with the negative mutual inductance (-M) of the T-coil, the negative magnetic coupling accommodates an initiatory boost to flow of current to C_{gs}. This takes into account an enhancement in rise time along with BWER. The gain falling-off of the first CG transistor (Q_1) is balanced by connecting L_G together with L_{D1} (bridged-shunt-series-peaked network). A low-Q shunt peaking at the center band is achieved by the second cascade stage. The inductor L_G provides high-flat power gain of LNA over the wideband of interest.

V. RESULTS AND DISCUSSIONS

The LNA, the critical component of RF front end is designed and examined for its performance in consideration of parameters such as high gain, stability, NF_{min} and linearity. Simulation results of gain (S_{21}), NF, 1 dB compression point (P_{1dB}), third order intercept point (IIP3), input-output reflection coefficients and stability with BSIM3 Predictive Technology Model (PTM) for 90 nm are obtained for the amplifier design [25].

The standard 90 nm CMOS process is supported to design the UWB LNA. The simulated gain, S_{21} with 50 Ω input impedance matching and noise figure are plotted in Fig. 6. The designed architecture has 19.11 dB peak gain at 9 GHz, and greater than 10 dB from 3.4 GHz to 11 GHz. The flat gain of 17.94 dB is obtained from 4.5 GHz to 9.5 GHz. The 2.88 dB of NF_{min} at 6 GHz and an average of 3.3 dB flat NF for frequencies 3.5-10.6 GHz are achieved. The input-output reflection coefficients (S_{11}, S_{22}) are shown in Fig. 7. As can be seen, S_{11} of less than -12.9 dB for (3-10) GHz and at 9 GHz -17.61 dB. The S_{22}, average output reflection coefficient is under -5.46 dB for entire frequency range and less than -6.22 dB at 9 GHz. The S_{12}, the reverse isolation below -50 dB is achieved.

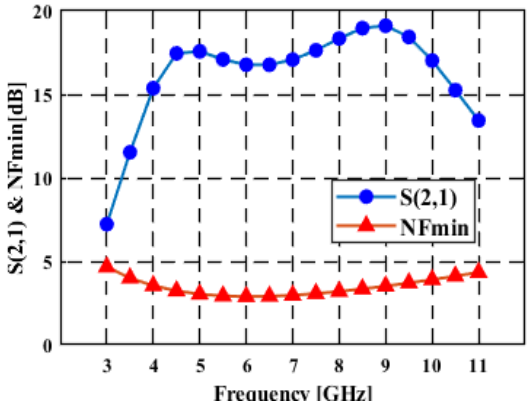


Fig. 6: S_{21} and NF of the LNA

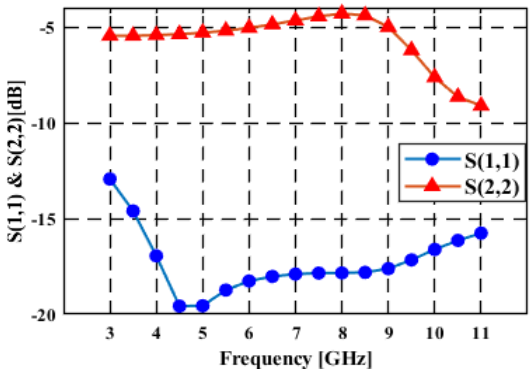


Fig. 7: S_{11} and S_{22} of LNA

Fig. 8 shows P_{1dB} of the amplifier, the actual response (V_{out}) and linear response are compared with respect to input power. The actual response coincide with the theoretical response from -30 dBm to -21 dBm, there is a difference of 1dB at -20 dBm and the gain decreases with further increase of the input power. Fig. 9 shows the plot of fundamental power (V_{out} [1, 0]) and third order power (V_{out} [-2, 1]), two harmonics, compared with respect to input power. Both are at -13 dBm of the input power. The value of stability factor (K) is found to be more than 1 by analyzing the Fig. 10 for operating frequency range of (3-11) GHz.

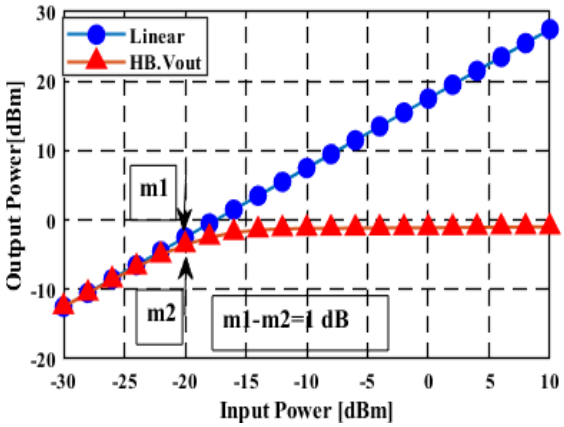


Fig. 8: Gain Compression Point off the LNA

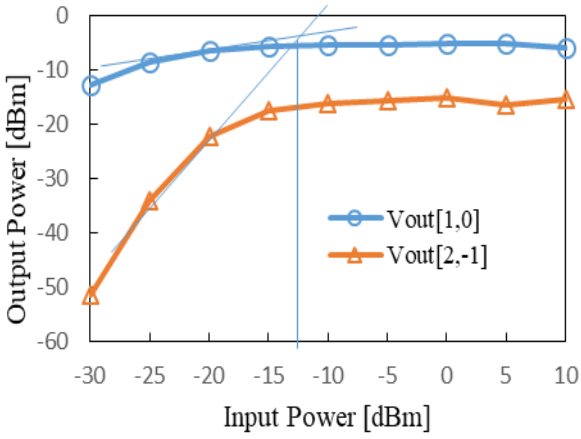


Fig. 9: IIP3 of the LNA

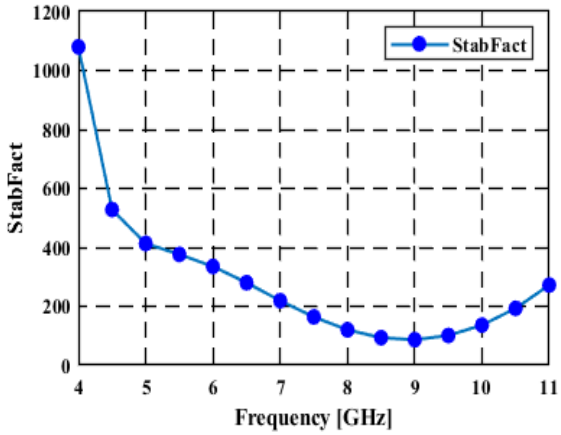


Fig.10: The LNA Stability Factor (K) response

The performance of wideband LNA is evaluated by using the suitable value of Figure of Merit (FoM) [5]. The FoM of the designed LNA is 8.47.

$$FoM\left[\frac{GHz}{mW}\right] = \frac{S_{21}.BW[GHz]}{(NF-1).P_D\,[mW]} \quad (4)$$

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Table II. Comparison of the proposed LNA with previously published works for UWB applications

Parameters	[15]	[14]	[11]	[9]	**This Work**
Technology (nm)	90	180	90	130	**90**
Frequency (GHz)	2.6-10.2	3.1-10.6	0.1-7	3-12	**3.1-10.6**
Peak S_{21} (dB)/ Freq	12.5	12.52	12.6	13.5	**19.11**
S_{11} (dB)	-9.0	< -10.25	< -10	< - 11	**< -12.90**
S_{22} (dB)	---	< -10	< -9	< - 10	**< -5.46**
NF_{min} (dB)	3-7	2.87	5.5	4.3	**2.88**
IIP3 (dBm)	---	-6.5	-9	-7	**-13.00**
P_{1dB} (dBm)	-12	---	-18	--	**-20.00**
P_{DC} (mW)	7.2	11.8	0.75	8.5	**9**
FoM	---	4.4	6	3.41	**8.47**
Stability Factor (K)	---	---	---	---	**K > 1**

Table II provides the comparison of the performance of the prototype amplifier with state-of-the-art designs narrated in the latest literature for UWB applications. Nan Li [9] has proposed a bandwidth extension technique of bridged-shunt series-peaking using CG topology. In [9] 3 GHz to 12 GHz, a flat-gain is around 13.5 dB, this work shows 17.94 dB flat-gain for 4.5 GHz to 9.5 GHz frequency. This paper has demonstrated a LNA, which achieves better gain, NF_{min} and FoM when compared to the previous designs in different technologies. The ADS simulation results indicate that gain, NF and FoM are improved by 24%, 33% and 24% respectively.

VI. CONCLUSION

A wideband inductively degenerated cascade LNA for UWB functions has been demonstrated in 90 nm RF CMOS technology for (3.1-10.6) GHz frequency range. The present paper is concentrated on high-gain, flat-low NF and good matching with low power. By employing asymmetric T-coil peaking technique with common gate-common source cascade topology a good input matching, a wide bandwidth, low power and flat-gain response are achieved. The 90 nm BSIM3 model parameters are employed to arrive transistor geometry for designing the cascade amplifier circuit. The UWB LNA achieves a maximum gain of 19.11 dB, NF_{min} of 2.88 dB, P_{1dB} of -20 dBm and -13 dBm IIP3 with 9 mW power dissipation. The proposed LNA compared with other UWB techniques has high gain flatness, low-flat NF and a higher FoM used in front end of RF receiver wireless sensor network applications.

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