An 86 dB Gain 18.06 mV_{rms} Input-referred Noise LNA for Bio-medical Applications

G. Revanth Kumar, K. Naga Sunanda, M. Durga Prakash

Abstract*: This paper admits a LNA (low noise amplifier) designed by taking bio-medical applications in to considerations. The amplifier is designed based on two gain stages, supply insensitive gain stage and inverter gain stage. Input-referred noise of the proposed amplifier is 18.02 mV_{rms} and it consumes a power of 0.012 mW. The amplifier produces a gain of 86.5 dB. Bandwidth of the proposed amplifier is 227 Hz with cut-off frequencies as 227 Hz (higher) and 1 mHz (lower). The entire system is built in 45-nm technology with supply voltage of 0.6 V.

Index Terms*: Low Noise Amplifier, gain, bandwidth, input referred noise.

I. INTRODUCTION

Electronic devices have very huge demand in biomedical applications like neural recording systems, ECG, EKG etc. LNA is critical for interfacing the machine with the extracellular signals. As these signals are very weak, they exhibit the amplitudes between 50µV-500 µV, and noise levels between 5µV-10µV [1]. Designing extracellular interfaces for observing brain and heart activity became very tough task for designers. There is a great demand for LNA's in biomedical engineering that allows technicians to continuous monitoring for extracellular signals. The purpose of LNA is that, they must be capable of observing and amplifying the very low amplitude and low frequency signals.

Low noise amplifiers are also called as neural amplifiers and bio potential amplifiers that are only preferred for amplifying the very low frequency and amplitude signals. Misreading or mis matching of neural signals from the neural sysytems to the neural interfaces results failure in monitoring patients health activity, for the prevention of these situations we need a neural inerfaces like Low noise amplifiers.

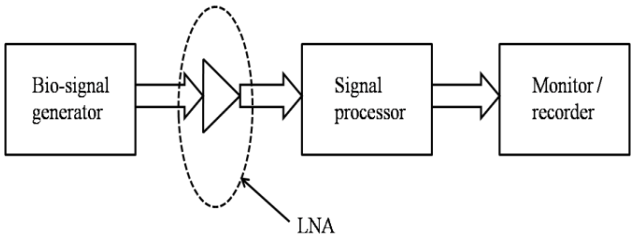

Fig. 1. Block diagram of Bio-signal processing system.

From the last years there are several Bio-amplifiers are investigated by the research fellows to achieve high bandwidth, and small chip area. Shahed enamul *et al.* designed an ultra-low-power and low-noise Bio-amplifier in 0.13-µm standard RF CMOS process. It has a bandwidth of 9.51 kHz with input noise of 0.91µVrms and 198.6nW power is dissipated [1]. Harrison *et al.* designed low power and noise amplifier in 1.5-µm technology. It has a bandwidth of 7.2 kHz with an input noise of 2.2µV_{rms} and dissipates a power of 80µW [2]. Salhi *et al.* designed low voltage, low noise bio-signal amplifier using 130-µm CMOS technology. It produces a gain of 75dB and absorbs 1.24µW with input noise of 0.91nV^2/Hz [3]. J.kim *et al.* designed low-power neural amplifier in 0.35-µm CMOS process. It has a bandwidth of 11.1 kHz and an input noise of 14.5µV_{rms} and a power dissipation of 220nW [4]. J. Holleman *et al* presented a sub microwatt low noise amplifier which is used for neural signal recording application. The amplifier is designed in 0.5-µm SOS Bi-CMOS technology. It exhibits 3.5µV_{rms} of input noise and provides the gain between 36 to 44 dB. It requires 1V to operate and consumes only 805nA [5]. J. Ruiz-Amaya *et al* presented a low noise amplifier for bio medical spike signal recording interfaces. The system is designed based on feedback network using two stages OTA. The amplifier is designed using 0.13-µm CMOS technology. It exhibits 3.8µV_{rms} of input-referred noise and provides the gain between 46 dB. It takes 1.92 µW and operates at 1.2V. It provides a bandwidth of 192 Hz–7.4 kHz [6]. Fig.1 represents the whole block diagram of Bio-signal processing system. The LNA is theoretically simulated using the small signal analysis [7]. An inverter based gain stage is used in designing the LNA, which helps in producing the high gain to the amplifier [8]. LNA has been simulated practically in transient analysis, ac analysis, dc analysis and noise analysis for calculating gain, cut-off frequencies, power consumption, band width etc. [9]. K. L. Baishnab *et al* designed A Low Power, LNA for Neural Signal processing. It uses an OTA which is built using folded cascode architecture. The amplifier presents a good noise performance with input-referred noise 3.22 µV/√Hz and had a band gain of 42 dB. The LNA dissipates very low power nearly 630 nW [10]. Chao Fang *et al* designed an ultra-wideband LNA which produces a gain of 13 dB only with noise of 3.4 dB. The designed LNA consumes a DC power of 12.9 mW [11]. Xiao Yang *et al* designed a Low power LNA with chopping technique. The measured input-referred noise for the LNA is 39nV/ Hz, with a power consumption of 117µW [12].

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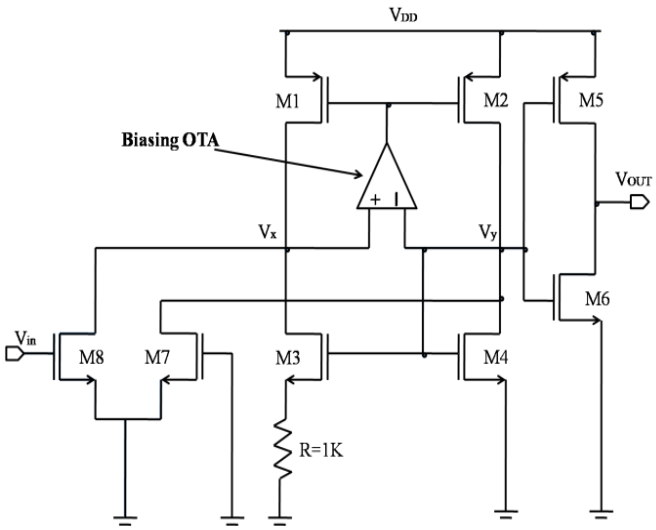

Fig. 2. Schematic diagram of LNA.

This work presents a low noise amplifier which is designed based on beta multiplier reference (BMR) based differential first gain stage and a CMOS inverter based second gain stage. The proposed amplifier is designed in 45-nm standard CMOS process, capable of recording the biomedical signals in between the range of 0.001 Hz to 227 Hz. The amplifier has a gain of 86.7 dB. It consumes a power of 0.012 mW with 0.6V supply voltage and the input-referred noise is 18.02 mV_{rms}.

II. LNA DESIGN

The amplifier is designed using nMOS differential input stage *(M_x-M_y)*, a beta multiplier reference (BMR) circuit *(M_1-M_4)*, and a CMOS inverter *(M_5-M_6)* [1]. The schematic structure of the proposed LNA is shown in figure 2.

A. Beta multiplier reference circuit gain stage:

The differential amplifier circuit produces the first amplification stage. The beta multiplier reference circuit should be used for supply independent biasing. From the BMR circuit we can write [9],

$$V_{GS,M4} = V_{GS,M3} + V_M R \qquad (1)$$

Where, I_M represents reference current of the BMR circuit, R represents bias resistance, V_{GS} represents gate-to-source voltage of the particular MOSFET. The gate to source voltages of M_3 and M_4 in (1) must be related as [1], $V_{GS,\,M4} > V_{GS,\,M3}$.

The amplifier is designed to operate in sub-threshold region. The sub-threshold drain current can be calculated as [8],

$$I_M = I_{D0}\left(\frac{W}{L}\right) exp\left(\frac{qV_{GS}}{nkT}\right) \qquad (2)$$

Where, I_{D0} represents technology current, q represents electrical charge, n represents sub-threshold slope parameter, k represents Boltzmann constant, T represents absolute temperature and the width to length ratio of MOSFET is represented as *(W/L)*.

To make biasing point highly insensitive to temperature and supply voltage, the BMR circuit uses an operational transconductance amplifier (OTA). To calculate the first stage gain, we have to perform small signal analysis.

The output resistance of the half-folded cascode circuit is [7],

$$R_{cascode} = r_{01} || g_{m3} r_{03} R, \qquad (3)$$

Where, $R_{cascode}$ represents equivalent output resistance of the cascode amplifier, g_{m3} represents transconductance and r_{03} represents output resistance of the corresponding MOSFET *i.e*, M_3.

Now, the first stage gain can be calculated as [4],

$$A_{V1} = -g_{mx}\,(r_{01} || g_{m3} r_{03} R), \qquad (4)$$

Here, g_{mx} represents transconductance of the corresponding MOSFET *i.e*, M_x, A_{V1} is the gain of first stage of amplifier. From (4), it is clear that gain is constant for any variation input.

B. CMOS inverter Circuit gain stage:

To obtain high gain for the amplifier we have to use a CMOS inverter in the middle of transistor region. Hence, for the second amplification stage we can use a CMOS inverter [8]. The small signal gain of CMOS inverter is [8],

$$A_{v2} = -(g_{m5} + g_{m6})(r_{05} + r_{06}), \qquad (5)$$

Here, A_{V2} represents gain of CMOS inverter, g_{m5},g_{m6} and r_{o5},r_{06} represents transconductance and output resistance of the corresponding MOSFETs M_5 and M_6.

Hence, LNA overall gain can be calculated by multiplying the gain of both stages,

$$A_v = A_{v1} A_{v2} \qquad (6)$$

By using (4) and (5) we will get,

$$A_v = -g_{mx}\,(g_{m5} + g_{m6})(r_{01} || g_{m3} r_{03} R)(r_{05} || r_{06}) \qquad (7)$$

Where, A_V represents the total gain of LNA.

III. OTA DESIGN

The diagrammatical representation of LNA is in fig 3. It utilizes a transconductance amplifier (OTA). Fig shows the diagrammatical representation of the OTA and the OTA design contains several features. By using the two stage architecture OTA was designed and these are used for large swing and high open loop gain. OTA uses a magnifying structure which is fed with PMOS input transistors in sub-threshold region in its first stage to obtain better blink noise performance and minimized gm/ID ratio. A

conventional pair is used to avoid common mode and noise produced by power supply. The amplifier is modeled in a way that it has the ability of recording bio-medical spike signals or very weak signals.

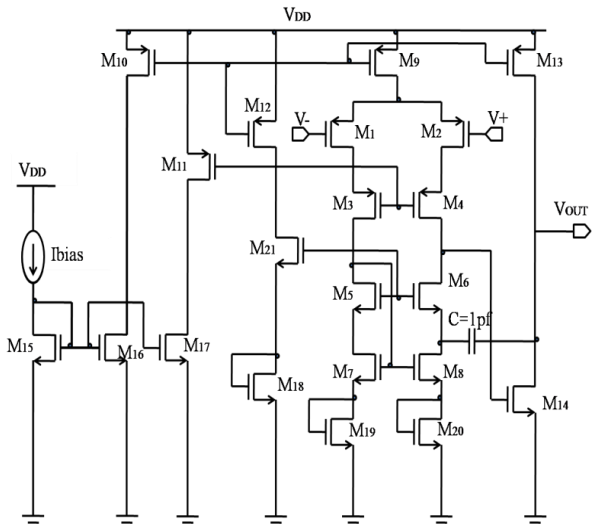

Fig. 3. Schematic diagram of OTA.

Using the resisters in OTA schematic causes to produce noise in source degeneration current sources, by taking correct resistor values. To raise the output impedance *M3* and *M4* are cascaded with input differential pair transistors. To obtain large output impedances by *M16, M17* source degenerated current sources are modeled.

IV.RESULTS AND DISCUSSIONS

The LNA is simulated using Cadence Virtuoso Tool in 45-nm technology. Proposed LNA produces a gain of 86.7 dB. Gain response plot of the proposed LNA is shown in fig 4. It allows the signal ranges from 0.001Hz to 227Hz.

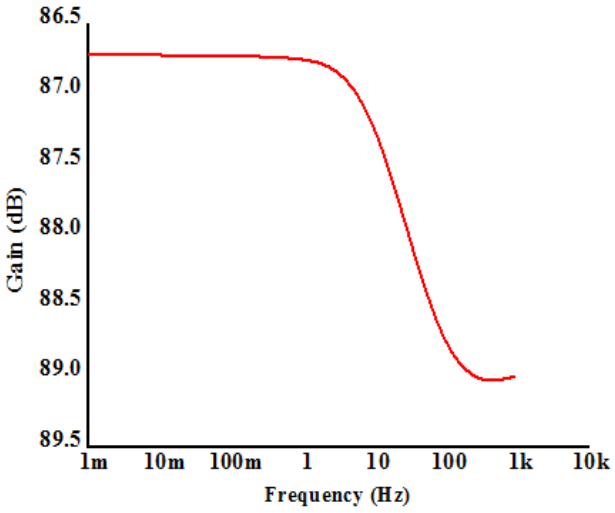

Fig. 4. Gain response of proposed LNA.

Input-referred noise response of the proposed LNA is in fig 5. The LNA attains a gain of 86.7 dB which is very good and better than previous works. From Figure 4 it is clear that, it has a constant gain up to 80 Hz and then it decreases slowly. Gain is constant fro 1 mHz, which is very low frequency. To calculate Bandwidth, lower cut off frequency and higher cut off frequency we have to add -3dB to the maximum output or dB. By adding -3dB we obtained the bandwidth 227 Hz , lower cut off frequency and higher cut off frequency are noted as 1mHz and 227Hz.

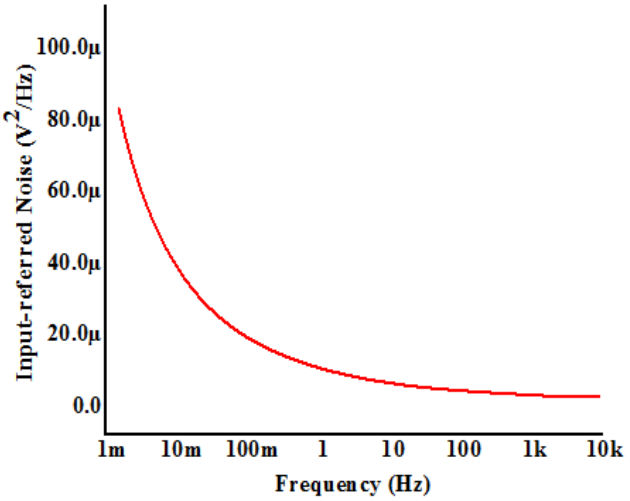

Fig. 5. Input-referred noise response of the LNA.

Input-referred noise of proposed LNA is varies for different frequency levels. The above figure.5 is obtained from different input-referred noise levels at particular frequencies. Here frequency is taken on horizontal axis and input referred noise is taken on vertical axis. Input-referred noise values are represented in V^2/Hz and frequency values are represented in Hz.

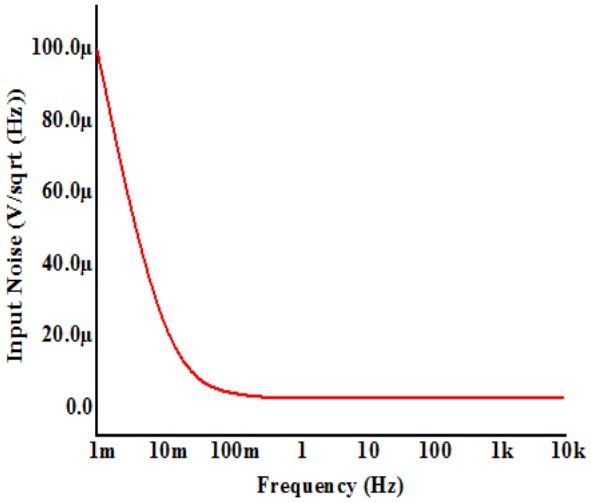

Fig. 6. Input noise response of the LNA.

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TABLE I. Comparing LNA parameters with previous work.

Parameters	This work	[1]	[2]	[3]	[4]
CMOS technology	45-nm	0.13-µm	1.5-µm	0.13-µm	0.35-µm
Supply voltage	0.6 V	0.6 V	±2.5 V	±0.6 V	±0.9 V
Power consumption	0.012 mW	198.6 nW	80 µW	1.24 µW	220 nW
Gain	86.7 dB	24.94 dB	40 dB	75 dB	28.9 dB
Bandwidth	227 Hz	9.51 KHz	7.2 KHz	18.8 KHz	11.1 KHz
Higher cut-off frequency	227 Hz	9.51 KHz	-	19 KHz	11.2 KHz
Lower cut-off frequency	0.001 Hz	0.01 Hz	0.13 Hz	-	0.1 Hz
Input-referred noise	18.02 mVrms	0.91 µVrms	2.2 µVrms	0.91 nV^2/Hz	14.5 µVrms

µm= micro meter, V = volt, nm=nano meter, mW= mille watts, µW= micro watts, nW= nano watts, Hz= hertz, K= kilo, V_{rms}= rms value of Voltage

Table1 represents the performance of low noise amplifier and compares with the previous work. The parameters like gain, bandwidth, lower-cut off frequency, higher cut off frequency, power consumption and input noise of the LNA are well defined. Gain of the LNA is very good when differentiated to the other works bandwidth of the LNA is also good enough as it is capable to amplify very weak signals. The input-referred noise (output noise divided by amplifier gain) of the LNA is also better than previous works. Additionally, table describes about the different CMOS technologies used in previous works and their operating voltages.

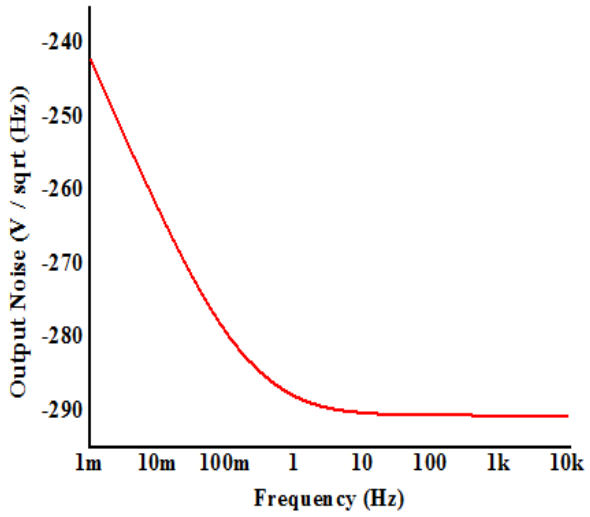

Fig. 7. Output noise response of the LNA.

Figure 6 and Figure 7 represents the input noise response and output noise response of the low noise amplifier. These graphs are obtained by performing noise analysis ranging from 1mHz to 10KHz frequencies in cadence virtuoso tool. Above graphs describes different noise values at particular frequency levels. Noise values are represented in V^2/Hz on vertical axis and frequency is representing in Hz on horizontal axis. The decrease in noise levels from input noise response to output noise response is very clear from Figure 6 and Figure 7.

V. CONCLUSION

A new LNA has implemented for biomedical applications. The LNA is designed based on two stages, first gain stage is beta multiplier reference (BMR) based differential stage and the second gain stage is based on CMOS inverter. The total gain will be multiple of two stages. The LNA is implemented in 45-nm CMOS technology. The gain of the amplifier is 86.7 dB operates at 0.6V and consumes only 0.012 mW. The input-referred noise of the proposed LNA is 18.02 mVrms and the bandwidth of the proposed LNA is 227Hz which is helpful for Bio-medical applications.

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