Design of Efficient 16 Bit Crc with Optimized Power and Area in Vlsi Circuits

B.Balaji, N Ajaynagendra, Erigela Radhamma, A Krishna Murthy, M Lakshmana Kumar

Abstract*: *In Very-Large-Scale Integration (VLSI) application power and area are the vital factors for any digital circuits.This paper presented 16 bit Cyclic Redundancy Check (C RC) mapped in version v14.20-s013 1 of Cadence Encounter(R) RTL Compiler. The codes in numerous instances are visible to be advanced at block lengths of realistic hobby when they're used on low-noise BCCs.. By expeditiously mapping on cadence tool, Power is achieved small. The results of conversion are viewed mistreatment RTL synthesis cadence VIRTUOSO at 45nm technology. Supported digital signal process (DSP) architectures, the code for proposed low power is generated mistreatment 16 bit Cyclic Redundancy Check (CRC).

Index Terms*: *16 bit Cyclic Redundancy Check (CRC), Low Power, Low Area, High Level Synthesis, DSP, LUTs VLSI.

I. INTRODUCTION

Cyclic Redundancy Code (CRC) are a general form of cyclic codes. Which are extensively used for error detection purpose[1], [2]. A CRC encoder appends p-parity bits to an input binary string in the sort of way that the resulting code words match to polynomial multiples of a generator polynomial g(x) of degree p. we will denote a CRC-code with p parity bits as a CRC p-code. The most advantageous minimal Power and Area available by way of a few CRC-sixteen codes is determined for all block lengths. For several normal low-noise BCCs the minimum undetected blunders opportunity potential with a few CRC-16 codes is given for all blocks.

The design of composite chips has supported a chain of transformations over the last 20 years. Within the last few years, layout for low power has initiated to change once more how designers' technique complicated Silicon on chip (soc) designs. The increase in chip thickness drives the acceptance of synthesis presents the brilliant increase within the era of hundreds of thousands of gate designs, engineers uncovered that there has been a restrict to how an awful lot new Register Transfer Logic (RTL) will be aided for a new chip design. Depending on the application, CRC-codes are used at a Constant block length n, at variable block lengths, i.e., the generated Code words both all have a hard and fast wide variety of digits or their length can range from message to message. This regularly performs an essential position in receiver synchronization. R.Henkmat [2004] proposed a brand new model to calculate interference stages in wireless multi-hop advert-hoc networks. Robert C B.aumann [2005] provided radiation-prompted smooth errors in advanced semiconductor technologies. The as soon as- ephemeral radiation-precipitated tender errors has a key 14 danger to advanced business electronic components and systems. The smooth mistakes have the potential for inducing the best failure price of all other reliability mechanisms combined. to save you the accumulation, TMR is often matched with reconfiguration strategies which include complete reconfiguration, partial reconfiguration (PR), or scrubbing. Many of the previous studies used TMR with scrubbing or dynamic partial reconfiguration (DPR). DPR enables in losing the configuration time and is appropriate for a combinational circuits

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II. LITERATURE REVIEW

Cyclic Redundancy checks (CRC) is employed for detecting the corruption of digital knowledge throughout the transmission, process or the storing of information. The CRC treats the info bits as a binary polynomial with a selected breadth, then it calculates the rest from the division of information bits with a generator polynomial. At the receiver facet, the information with the substantiation divided by a similar polynomial, if the result was achieved to be zero that confirms the information was received properly. it's far honestly unreasonable for any statistics reporting or verbal exchange intermediate to be one hundred% ideal of the time over its whole predicted beneficial life [1][2][3][4]. as greater bits are arranged right into a square centimetre of disk garage, as statistics sending speeds growth, the likelihood of blunders will increase sometimes geometrically. therefore, errors detection and correction is vital to strong information transmission, storage, and renewal. test digits appended to the cease of a long quantity can provide a few safety towards data enter mistakes. longer data streams have needed a more efficient and sensible errors detection gadget. Mathematically, a k-bit message may be considered because the coefficients of a polynomial $B(x) = bk\text{-}1x^{k-1} + \ldots + b1x^1 + b0x^0$.. the most large bit leads the information circulation. Moreover, an (m+1) bit generator polynomial $P(x) = x^m + pm\text{-}1x^{m-1} + \ldots + p1x^1 + p0x^0$ of order m is selected. Calculations are completed in modulo-2 mathematics. The CRC is the remainder of the department of xm B(x) by P(x) and can be appended to the message [4].

A. Cyclic redundancy

check

From the transmission side (antenna), the r bits are checked using linear codes, i.e. CRC codes, are generated at the outlined rule per the bits binary transmitted codes. The check codes are then hooked up to the transmission knowledge. At the receiving end (antenna), the check is done per the rule between data codes and also the CRC codes to create positive if there are some faults (errors) within the transmission method.

B. **CRC polynomial:**

It describes a way for locating cyclic redundancy check polynomials for systems for transmission over trifocal channels that inscribe info in multiple voltage levels. in orderthat the ensuing redundancy check offers smart error protection and is economical to implement. The codes that we tend to construct have a playing distance of three or four. We tend to discuss some way to cut back burst error in parallel transmissions and a few tricks for economical implementation of the register for these polynomials. we tend to illustrate our techniques by discussing a selected example wherever the amount of levels is nine, however they're applicable generally.

$$BCC = n - k.....(1)$$

A data info polynomial G(x) is branched by a selected generator polynomial operate P(x), the result's broken and also therest is truncated to sixteen bits and appended to the data as a BCS. The division isn't accomplished with the quality arithmetic division. Instead, the modulo-2 division is employed, since this remainder springs from AN exclusive or (XOR) procedure.

16 bit-CRC will be expressed as

$$G(x) \div P(x) = Q(x) + R(x).....(2)$$

Where

G(x)=Information polynomial
P(x)=Generator polynomial
Q(x)=Quotient
R(x)=Remainder

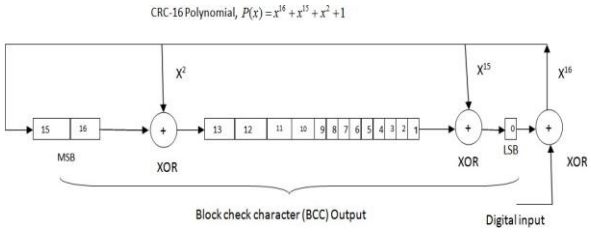
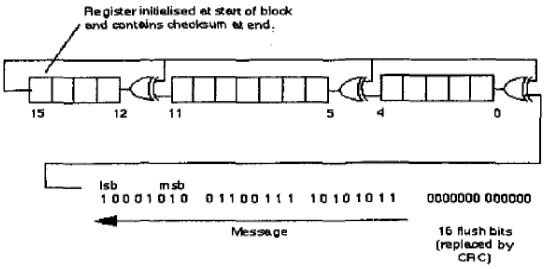


FIG.1: BLOCK CHECK CHARACTER

Fig.2: Cyclic Redundancy Checker



C. **Bit-to-symbol block**

The four least vital bits (namely LSBs) (b0, b1, b2, b3) of every set is depicted into one information sort and also the four most important bits (MSBs) (b4, b5, b6, b7) of every set is mapped into the subsequent information sort. Any cluster of the protocol information unit is processed through the bit-to-symbol (BTS) block incessantly, starting with the Preamble field (PF) and gap with the top set of the PSDU.

II. LOW POWER ANALYSIS

2.1 DYNAMIC POWER:

The power consumed by a System on Chip is sum of dynamic power and static power.
Dynamic power is that the power dissipated/ consumed once the fabric is in active mode. Whenever the device is in active mode the ability dissipated within the device is termed as Static power, however the signal values are unchanged.

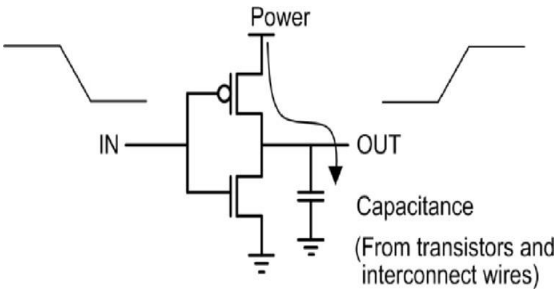


FIG 3: DYNAMIC POWER

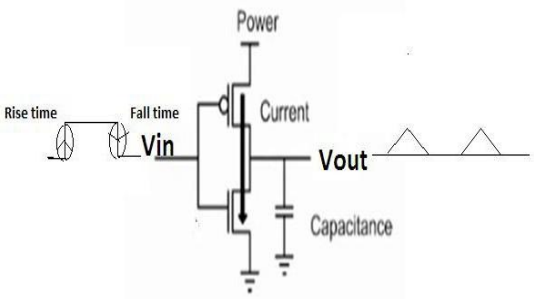


FIG 4: Static Power

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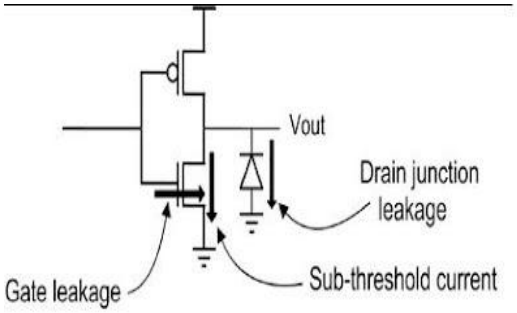

FIG 5: LEAKAGE CURRENTS

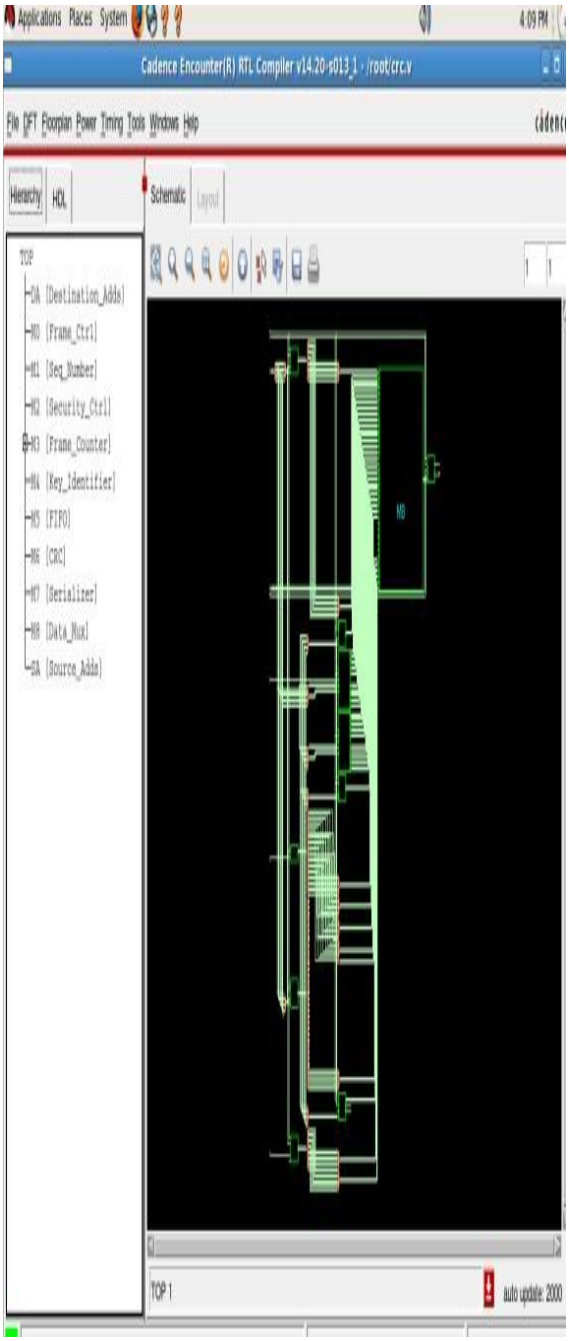

FIG 6:16 BIT CRC SCHEMATIC DIAGRAM OF 45NM TECHNOLOGY

$$P_{STATIC} = I_{Static} V_{dd} \text{.....(3)}$$

$$P_{Short-circuit} = I_{SC} V \text{.....(4)}$$

$$P_{Leakage} = V_{dd} (I_s I_G I_D) \text{.....(5)}$$

$$P_{Total} = P_{Dynamic} + P_{Leaksge} \text{.....(6)}$$

$$P_{Total} = (\alpha C_L V^2{}_{dd} \ f_{CLK}) V_{dd} (I_s I_G I_D)$$

IV. SYNTHESIS AND SIMULATION RESULTS

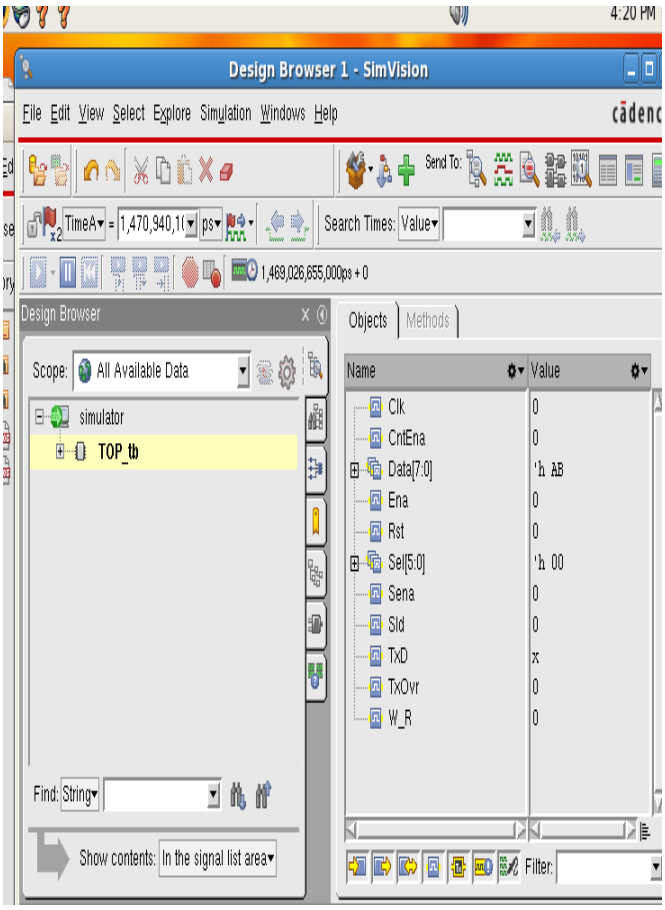

Figure 7: 16 bit CRC design browser 1-simvision 45nm Technology

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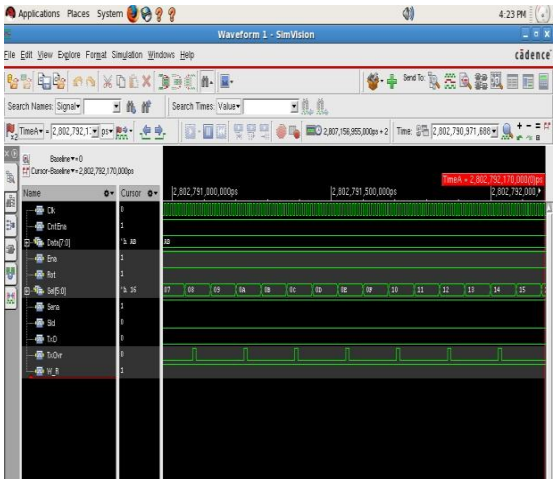

Figure 8: 16 bit CRC of Simulation Result of 45nm technology.

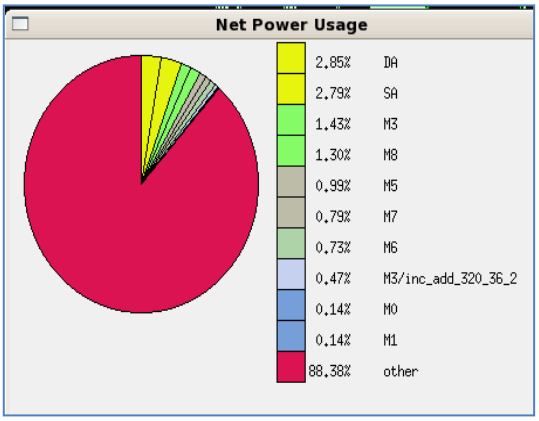

FIG 9: net power usages

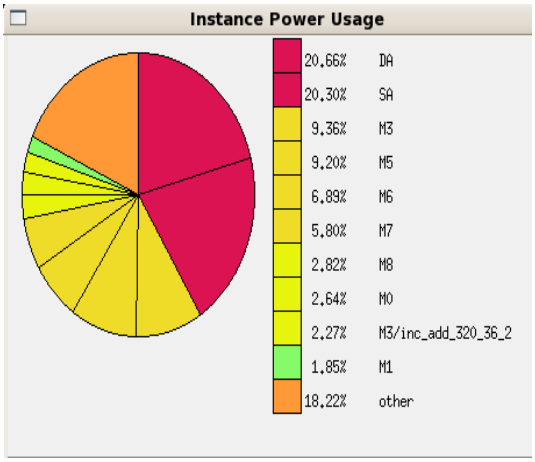

FIG 10: instance power usage

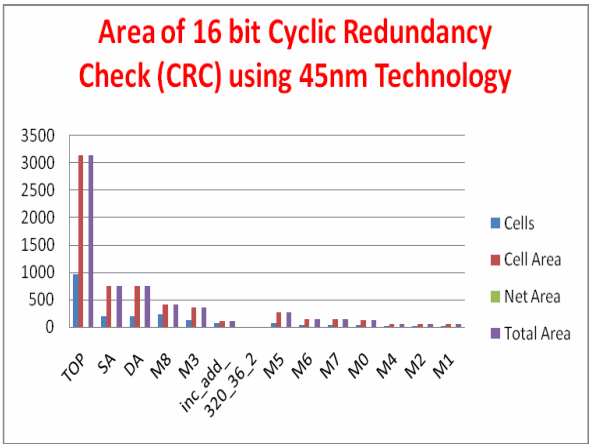

FIG 11 gives the area of 16 bit CRC in 45nm technology.

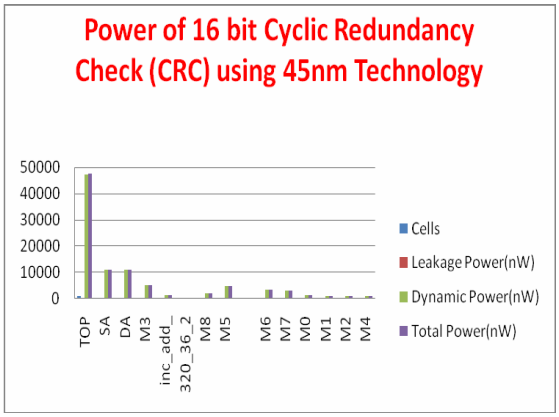

FIG 12 gives the area of 16 bit CRC in 45nm technology.

Table 1 16 bit CRC power dissipation using cadence tool 45nm

Model	Structures	Leakage Power in nW	Dynamic Power in nW	Total Power(nW)
TOP	963	161.258	47155.45	47316.708
SA	197	41.02	1087.3	1128.32
DA	197	42.65	11108.12	11150.77
M3	125	21.012	5089.56	5110.572
inc_add_320_36_2	61	6.859	1285.25	1292.109
M8	234	20.485	1923.117	1943.602
M5	62	13.213	4815.24	4828.453
M6	29	8.504	3604.23	3612.734
M7	39	8.128	3115.946	3124.074
M0	32	7.417	1301.483	1308.9
M1	16	3.654	921.727	925.381
M2	16	3.743	931.727	935.47
M4	16	3.764	941.727	945.491

V. CONCLUSION

In this research paper, we simulated mapping style into cadence tool using 16 bit Cyclic Redundancy Checker (CRC). Table II represents 16 bit CRC of area at 45nm technology, table 2 represents 16 bit CRC of power dissipation at 45nm technology and table 3 represents 16 bit CRC of delay at 45nm technology and power of circuit at 0.7V. With the aid of DSP architectures, the code is generated which resulted in low power and area efficient

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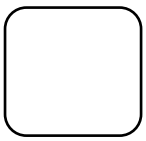

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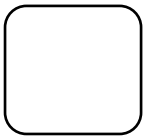

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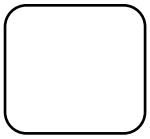

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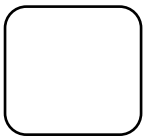

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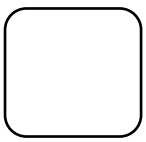

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