

Design and Performance Evaluation of Hybrid Vedic Multipliers

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Abstract: Multipliers are one of the essential building blocks of several computational units. The computational units speed is determined by the multipliers speed. To improve the computational units speed, faster multiplier must be necessary. The Vedic multiplier is competent of performing faster multiplication operations. In Vedic mathematics, Urdhva Tiryakbhayam (UT) sutra discards the non essential steps in multiplication operation which in turn increases the speed performance of a multiplier. In this paper, design and performance evaluation of hybrid 8-bit and 16-bit UT Vedic multipliers are presented. The performances of proposed hybrid UT Vedic multipliers are improved by reducing the garbage outputs, constant inputs, quantum cost, number of total gates, Total Reversible Logic Implementation Cost (TRLIC), LUT's, consuming power and improving speed compared with other existing conventional and reversible UT multipliers.

Index terms: Urdhva Tiryakbhayam, Vedic mathematics, quantum cost, constant inputs, garbage outputs, Verilog HDL, Xilinx Vivado design suite.

I. INTRODUCTION

Swami Sri B.K.Tirthaji was rediscovered mathematics in between 1911 and 1918 and it is mostly based on sixteen rules which are titled as Sutras. Each individual formula has its own importance and is capable of solving a mathematical problem in different branches of mathematics. In Vedic mathematics, the UT sutra is the one of the multiplication algorithm. The Sanskrit words Urdhva and Tiryakbhayam means vertically and crosswise respectively. The UT algorithm is suitable for Decimal, Binary and Hexadecimal multiplications. The main idea behind this sutra is that partial product generation be able to done and then the parallel addition of generated partial products is performed which leads to reduction in the computational time. Multiplication is one of the arithmetic operations that are widely used in several applications such as ALU, MAC and DSP etc. In DSP units, multipliers are very much essential to perform filtering, FFT, convolution, correlation, wavelet compression and processor design [1].

Reversible gates are very demand for the upcoming technologies as they are famous to produce zero power dissipation for ideal conditions. It has wide applications in quantum computation, Optical information processing, DNA computing, low power CMOS, cryptography and nanotechnology [2-4]. Reversible logic theory mainly depends upon Landauer's principle. According to this principle, energy dissipated for every irreversible bit operation is at least $kT \ln 2$, where $k=1.3806505 \times 10^{-23}$ (Joule/Kelvin) is the Boltzmann's constant, temperature is 'T' at which operation is performed and $\ln 2$ is natural logarithm of 2.

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For every logical operation which is not reversible heat will be dissipate for every bit of information that is lost although they are implemented using dissimilar integration techniques. There will be loss of information when the inputs cannot be recovered from circuit's outputs. Reversible logics naturally acquire care of heating since in reversible designs the inputs can be uniquely recovered from its corresponding outputs [5-8].

II. RELATED WORK

Islam et al., [8] introduced a low cost quantum realization of reversible multiplier. The developed multiplier is good but their TRLIC value is high. T.R.Rakshith and Rakshith Saligram [2] introduced UT Vedic multipliers using reversible logic. The developed UT multipliers are effective but their TRLIC value is high. These UT multiplier designs are coded using Verilog HDL and simulated using Xilinx 9.2i simulator. P.Gowthami and R.V.S.Satyanarayana [1] introduced area efficient UT multipliers using reversible logic gates. The developed UT multipliers are effective but their TRLIC value is high. These multiplier designs are coded using Verilog HDL and simulated using Xilinx 14.3 simulator. Later Yogeswari et al., [9] introduced 8-bit and 16-bit reversible UT multipliers using reversible DPG and PG gates based ripple carry adders. These UT multipliers are more effective but their TRLIC value is high. These designs are coded using Verilog HDL, simulated and synthesized using Xilinx Vivado FPGA design suite.

III. REVERSIBLE LOGIC GATES

A. Peres Reversible Gate

Peres gate is a 3*3 reversible logic gate which is shown in figure 1. The three inputs are considered as P, Q, R and the three outputs are considered as X, Y, Z. Peres gate has a low quantum cost compared to other gates. Its quantum cost is four. Peres gate is mainly used as half adder by forcing the input R to zero thereby getting output (sum) from Y and output (carry) from Z. Peres gate is composed of two XOR gates and one AND gate. Peres gate is universal logic gate and all the basic logic functions can be implemented using the Peres reversible gate only. This gate can be realized as the universal gate as all the basic gate functions can be implemented by Peres gate alone. A single Peres can generate and propagate outputs when the last input $R = 0$.

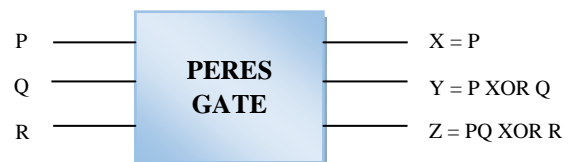


Fig. 1 Peres reversible gate

B. BME Reversible Gate

Design and Performance Evaluation of Hybrid Vedic Multipliers

BME is a 4*4 reversible logic gate which is shown below figure 2. The four inputs are considered as P, Q, R, S and the four outputs are considered as W, X, Y, Z and its quantum cost is five. BME gate is mostly used to generate partial products in the multiplication process.

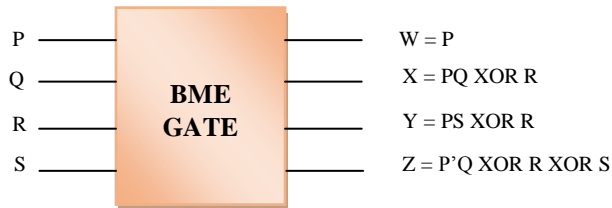


Fig. 2 BME reversible gate

C. DPG Reversible Gate

DPG is a 4*4 reversible logic gate which is shown below figure 3. The inputs are considered as P, Q, R, S and the outputs are considered as W, X, Y, Z and its quantum cost is six. The DPG gate can work singly as a full adder.

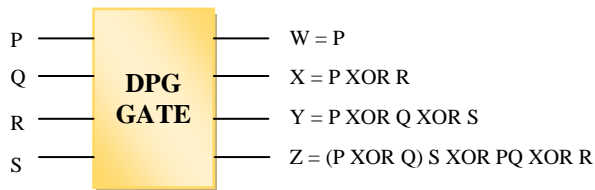


Fig. 3 DPG reversible gate

D. CNOT Reversible Gate

The most commonly used two input gate is the CNOT reversible logic gate which is titled as controlled NOT gate, essentially a reversible version of an XOR gate. It can also call that a Feynman 2-input gate. It is a 2*2 reversible logic gate which is shown in figure 4. The output of the CNOT reversible gate corresponds to the results of a classical XOR gate. Its quantum cost is one. CNOT gate requires copying the desire outputs and performing XOR operations.

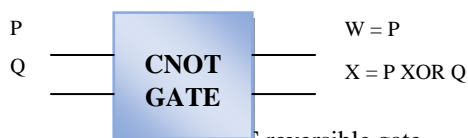


Fig. 4 CNOT reversible gate

E. BVF Reversible Gate

It is a reversible 4*4 bit double XOR logic which is shown in figure 5. The considered inputs are W, X, Y, Z and the considered outputs are P, Q, R, S and its quantum cost is two. BVF gate can be used as a fan-out gate with B = 0 and D=0 conditions.

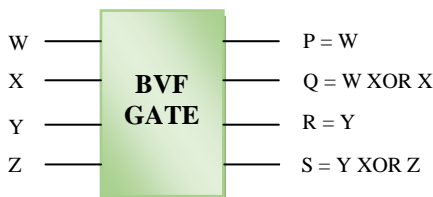


Fig. 5 BVF reversible gate

F. RMUX1 Reversible Gate

RMUX1 gate is a 3*3 reversible logic gate which is shown in figure 6. The inputs are considered as W, X, Y and the outputs are considered as P, Q, R and its quantum cost is four.

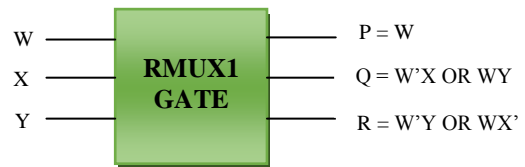


Fig. 6 RMUX1 reversible gate

G. Reversible OR Gate

Reversible OR gate is a 3*3 bit logic gate which is shown in below figure 7 and its quantum cost is four. This gate is obtained from RMUX1 gate.

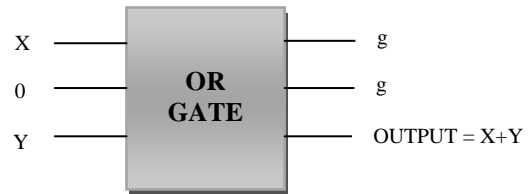


Fig. 7 Reversible OR gate

IV. PROPOSED WORK

A. Hybrid Vedic 4-bit UT Multiplier

The proposed 4-bit reversible UT multiplier block diagram is shown in figure 8. It consists of four reversible 2-bit UT multipliers, two 4-bit reversible ripple carry adders, reversible OR gate and reversible two half adders. The reversible 2-bit UT multiplier consists of one reversible BVF gate, two reversible BME gates, one PERES reversible gate and one CNOT reversible gate. The reversible 2-bit UT multiplier is shown in figure 9. The 4-bit reversible ripple carry adder consists of three DPG reversible gates and reversible PERES gate. The reversible 4-bit reversible ripple carry adder block diagram shown in figure 10. The OR reversible gate is shown in figure 7 and PERES gate is act as a half adder for a zero value is assigned to third input condition.

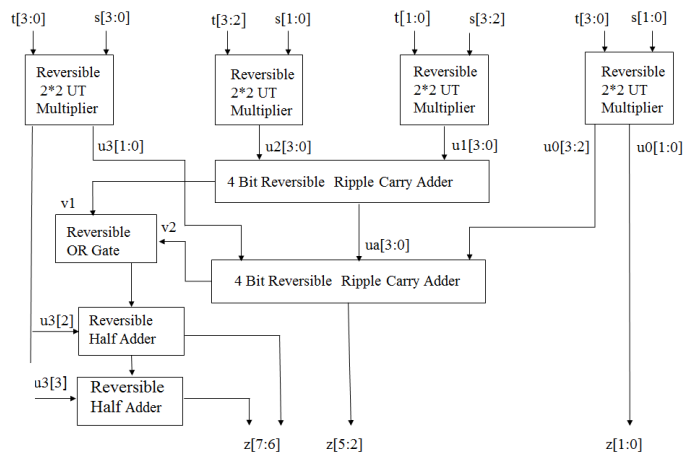


Fig. 8 Reversible 4-bit UT Vedic multiplier

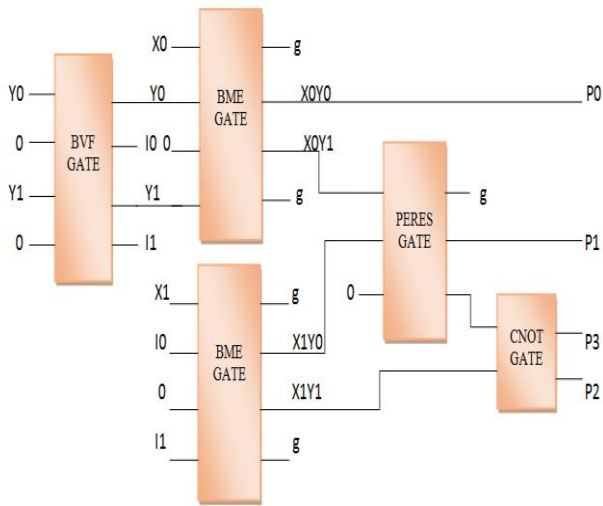


Fig. 9 Reversible 2-bit Vedic UT Multiplier

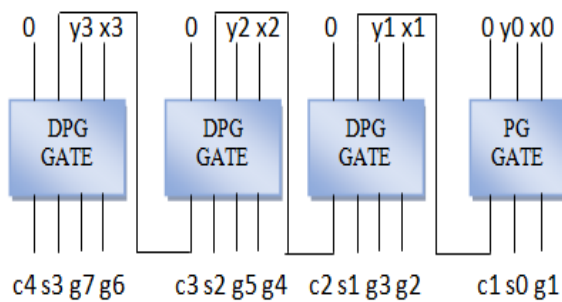


Fig. 10 Reversible 4-bit Ripple Carry Adder

B. Hybrid Vedic 8-bit UT Multiplier

The proposed 8-bit hybrid UT multiplier is designed using four 4-bit reversible UT multipliers and three conventional 12-bit arithmetic adders. The proposed hybrid 8-bit UT multiplier block diagram is shown in figure 11. Further it is coded using Verilog HDL and simulated using Xilinx Vivado simulator.

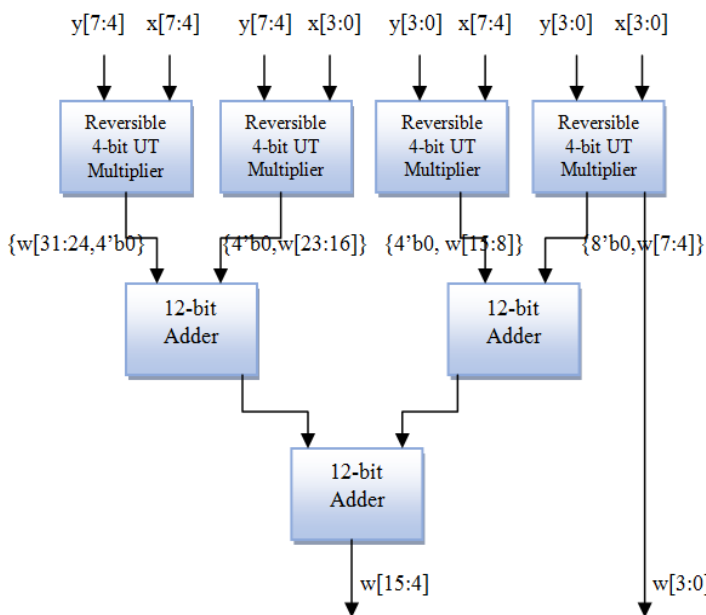


Fig. 11 Hybrid 8-bit UT Vedic Multiplier

C. Hybrid Vedic 16-bit UT Multiplier

The proposed hybrid 16-bit UT multiplier is designed using four hybrid 8-bit UT multipliers and three conventional 24-bit arithmetic adders. The proposed hybrid 16-bit UT multiplier block diagram is shown in figure 12. Further it is coded using Verilog HDL and simulated using Xilinx Vivado simulator.

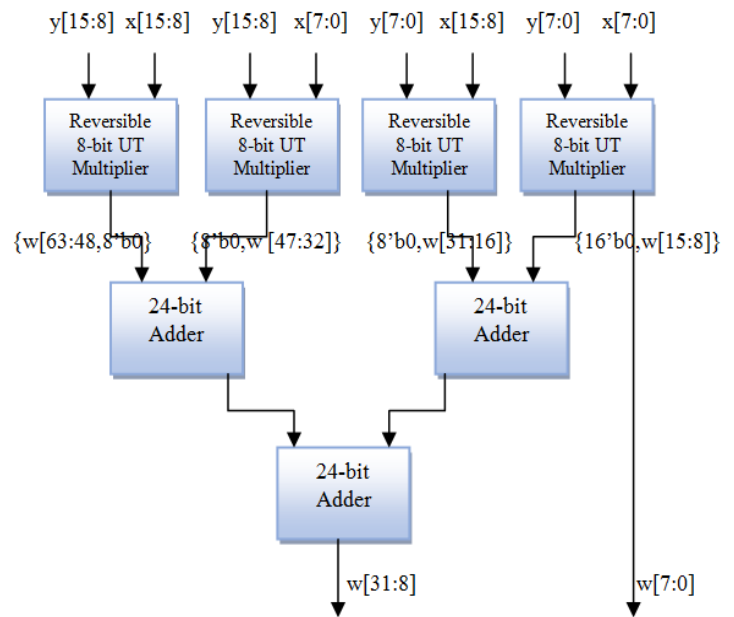


Fig. 12 Hybrid 16-bit UT Vedic Multiplier

V. RESULTS

The performance evaluations of 4-bit, 8-bit and 16-bit Urdhva Tiryakbhayam Vedic multipliers are illustrated in below table 1 and table 2. The proposed hybrid UT multiplier designs are functionally verified through a logic simulation process. To perform simulation, test benches are created for the proposed hybrid UT multiplier designs. The Verilog HDL is used to code the designs; simulation and synthesis processes are carried out using Xilinx FPGA Vivado design suite. The figure 13 shows the simulation waveform for hybrid 8-bit and figure 14 shows the simulation waveform for hybrid 16-bit Urdhva Tiryakbhayam Vedic multipliers. Table 3 gives the performance evolution of proposed and existing UT multipliers synthesis results.

TABLE 1 Performance evaluation of 4-bit UT Vedic Multipliers

Parameters	4-bit UT Vedic Multipliers		
	Existing [1]	Existing [2]	Proposed
Number of gates	31	37	31
Constant inputs	31	29	31
Garbage outputs	40	62	38
Quantum cost	128	162	124
TRLIC	230	290	224

Design and Performance Evaluation of Hybrid Vedic Multipliers

TABLE 2 Performance evaluations of 8-bit and 16-bit UT Vedic Multipliers

Parameters	8-bit UT Vedic Multipliers				16-bit UT Vedic Multipliers			
	Existing Reversible [1]	Existing Reversible [2]	Existing Reversible [9]	Proposed Hybrid	Existing Reversible [1]	Existing Reversible [2]	Existing Reversible [9]	Proposed Hybrid
Number of gates	145	169	145	124	621	717	621	496
Constant inputs	145	137	143	124	621	589	607	496
Garbage outputs	198	286	186	152	866	1218	810	608
Quantum cost	628	764	604	496	2740	3284	2628	1984
TRLIC	1116	1356	1078	896	4848	5808	4666	3584

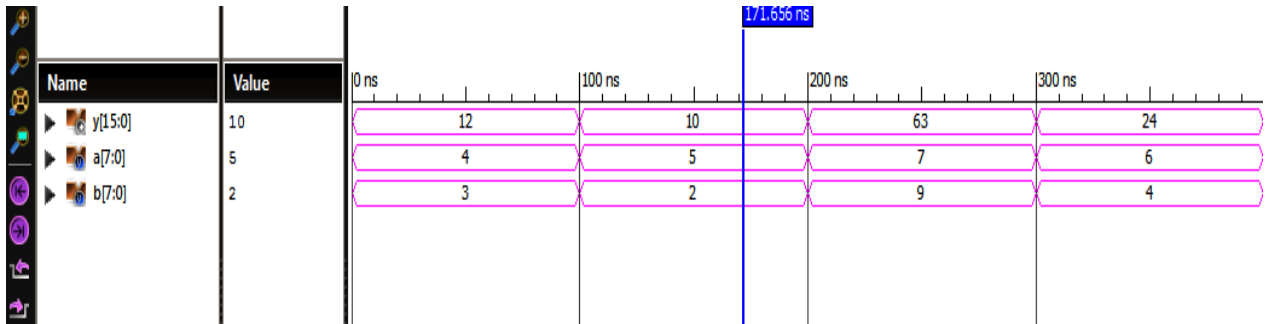


Fig. 13 Simulation waveform for 8-bit hybrid UT Vedic Multiplier using Xilinx Vivado simulator

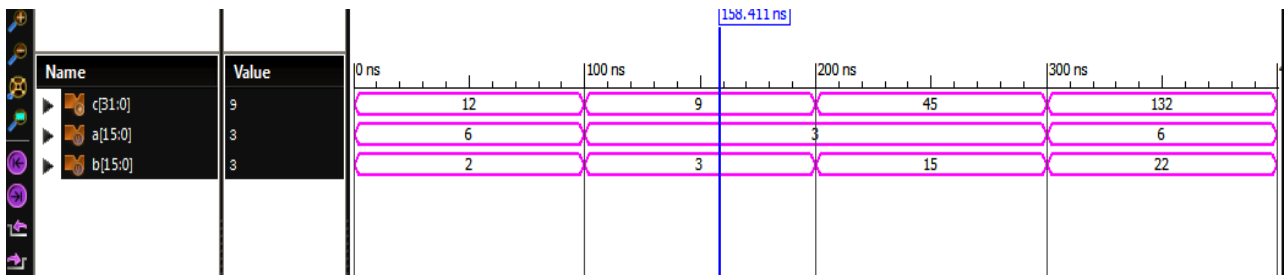


Fig. 14 Simulation waveform for 16-bit hybrid UT Vedic Multiplier using Xilinx Vivado simulator

TABLE 3 Performance evaluations of UT Vedic multipliers synthesis results using Xilinx Vivado design suite

Parameters	8-bit UT Vedic Multipliers				16-bit UT Vedic Multipliers			
	Conventional	Existing [1]	Existing [9]	Proposed Hybrid	Conventional	Existing [1]	Existing [9]	Proposed Hybrid
Used LUT's (Total -53200)	86	102	91	78	364	420	406	351
Dynamic Power (W)	12.858	12.482	12.434	12.409	32.561	34.859	33.945	31.946
Total Power (W)	13.898	13.522	13.474	13.449	33.601	35.899	34.985	32.986
Delay (ns)	15.102	14.138	13.330	13.192	23.021	21.647	22.848	21.327

Among all the UT Vedic Multiplier architectures in this paper, the proposed Hybrid multiplier architectures is found to be less number of gates, less quantum cost, less constant inputs, less garbage outputs, less TRLIC, consuming less power and faster speed.

VI. CONCLUSION

In this paper, Urdhva Triyakbhayam based hybrid Vedic multipliers, which is a formula of Vedic mathematics, was designed and compared. The

obtained TRLIC results of proposed hybrid Vedic multipliers are compared with the existing reversible multipliers. Further, proposed hybrid UT multipliers are coded using Verilog HDL, simulated and synthesized using Xilinx FPGA Vivado design suite. Finally, it is concluded that the proposed hybrid UT Vedic multipliers gives reduction in the TRLIC, garbage outputs, constant inputs, quantum cost, number of gates, used LUT's, consuming power and overall delay. In future, proposed 8-bit and 16-bit hybrid Vedic UT multipliers can be used in MAC design, DSP units and low power VLSI applications.

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