A FinFET Based Adaptive Filter Design Using Evolitional Algorithm for Noise Suppression

Udara Yedukondalu, V Vijayasri Bolisetty, Udara Srinivasarao

Abstract: This paper presents the implementation of an adaptive filter component using FINFET. The proposed is an analog adaptive filter based on CMOS algorithm. The existing CMOS based circuits suffer from short channel effects below 35nm. The proposed circuit reduces the power by reducing the leakage current. A FINFET based op-amp and four quadrants multiplier becomes the part of the adaptive filter. When compared to CMOS the FINFET based op-amp and four quadrants multiplier reduces the power. The evolutionary methodology approach using Artificial Bee Colony and Particle swarm optimization for the optimization of multichannel adaptive filter.

Index Terms: CMOS, FINFET, adaptive filter, LMS, four quadrant multiplier, Op-amp.

I. INTRODUCTION

The advancement in VLSI design have made the electronics products as smaller as possible. This has happened due to the reduction of device size in nanoelectronics. Eventhough CMOS circuits are found to be efficient below 35nm the technology is troublesome. In biomedical and communication systems adaptive filters (Xinwang, 2010) plays a vital role in removal of noise and identification of signals. Evolutionary algorithm based filter design were investigated in past (Julian Miller, 1999). Programmable filters have evolved in recent past to replace the conventional chips (Seo, 2018). A new approach to design a adaptive filter using evolutionary algorithm is implemented in FinFET.

For Noise cancellation adaptive filters were used due to its self-learning process. The filter coefficients are updated adaptively with respect to the noise strength. By adjusting the coefficients adaptively the error is minimized. The existing optimization techniques for adaptive filters are based on Least Mean-Square (LMS), gradient-based techniques., and Recursive Least-Square (RLS) method. The algorithms belongs to the gradient based techniques. These LMS and RLS based algorithm plays a vital role in designing digital noise cancellers in various applications like speech processing, extraction (Ravindrakumar and Bommannaraja, 2014) and speech enhancement (Goswami et al, 2014). But in literature several other optimization algorithms are presented. The methods are based on the particle swarm optimization, Artificial Bee Colony (Gao et al, 2013, Karaboga, 2010), etc. methods. These optimization techniques were more suitable for adaptive equalization (Cheded et al, 2011). Zhao et al (2013) used the bee colony algorithm to design the digital filter design. The method was suitable for DSP application. Real parameter optimization was done using the ABC algorithm (Kay, B. and Karaboga, D, 2012). The global optimization increases when these optimization is used.

II. BACKGROUND METHODOLOGY

The block diagram of ANC filter with ABC is shown in Figure 1.

2.1. ABC ALGORITHM

In ABC adaptive algorithm the position the bee position is equavated to the coefficient of the adaptive filter. The initial random population or the filter co-efficients are generated according to equation below

\[ x_{ij} = x_{\text{min},j} + \text{rand}(a) \times (x_{\text{max},j} - x_{\text{min},j}) \]  

(1)

‘a’ takes the value between -1 to +1. ‘i’ is the colony size and j is the dimension value in the colony which represent the filter coefficient of the adaptive filter. The probability of optimized position or coefficient value is determined by the equation

\[ p_i = \frac{\text{fit}_i}{\sum_{n=1}^{\text{SN}} \text{fit}_n} \]  

(2)

Once new location are generated probability selection process is carried out with the fitness value fit and SN chosen index value.

To optimize the coefficient value the ABC algorithm uses a scaling factor (sf) which produces the
The coefficient of the filter is found using the equation
\[ x_{s,j} = \begin{cases} 
  x_{s,n,j} + \phi_{s,j} *(x_{s,n,j} - x_{s,n}) & \text{for } sf \\
  x_{s,n,j} & \text{otherwise} 
\end{cases} \]  

(3)

The magnitude of perturbation is controlled by the scaling factor. The adaptive filter co-efficients are updated using the evolutionary methods. The algorithm can be applied to any number of channels. The LMS optimization of uses instantaneous estimation of vectors based on input d (n) and error e(n) using the below equation.

\[ \nabla (n) = -2e(n)[d(n)] \]  

(4)

In conventional methods the filter coefficients are updated as

\[ h(n + 1) = h(n) + \mu e(n)[d(n)] \]  

(5)

Which is a gradient estimation.

The estimation requires the knowledge of data x(n) alone and not the knowledge of cross correlation.

\[ e(n) = [h(n)] + \mu e(n)[d(n)] \]  

(6)

In gradient vector estimate for multichannel system can be coined by the equation

\[ d(n) = q(n)[F(n) + M(n) + q(n) \]  

(7)

Where \( d \) is the input and \( N \) is the noise representing low and high frequency component. The coefficient of the filter is estimated based on the data input and previous stage output.

### 2.2. PSO Algorithm for multichannel system

The PSO algorithm can be used to solve any nonlinear equations. Here a random swarm is initiated, velocity and position updates are made. The particle fitness is evaluated based on selected fitness function. The position is updated in each training update. The inertia weight parameters provides better efficiency and convergence.

In this method, for the best possible positions with least swarm is optimized.

\[ p(n + 1) = W(n) + \mu(n), O(error,(n),d(n),\phi(n)) \]  

(8)

### 2.3. Modular structures

The modular structure for a analog adaptable filter is shown in figure 2 (Jose,2008, Carusone and D.A. Johns,2000). The elements are transfer functions, integrators, multipliers and summers.

![Figure 2. Adaptive Modular filter](image2)

The other modules are delay line and velocity control of convergence (Manish et al,2015). Several architectures for

### 2.4. FinFET Device Structure

In the advancement of nanometer technologies the chip density and operating frequency have increased. The usage of power through battery is a main problem if the number of features is increasing in the application. The power supplies in non portable devices have different challenges in the design of cooling system and alternate power options. The other major concern is problems occurring due to high package density. Within the power budget the main design goal for VLSI is to be meeting with the required performance. The Fin type Field Effect Transistors (FinFET) replaces the bulk CMOS in 32 nm. The second order effects are troublesome when scaling of transistors are adopted (Prateek Mishra et al. 2011) for addressing the challenges posed by continued scaling. The fabrication of FinFET’s is compatible with the CMOS which helps in rapid deployment.

New Integrated circuits are emerging in market using FinFET technology. Especially in computational and communication integrated circuits manufactured using advanced technologies like 65 nm and 45 nm. Figure 3.(a) & (b) shows the FinFET transistor device layout and structure formed on Silicon On Insulator fabrication technique. It is a single gate stacked on top of two vertical gates. The device has very good control over current when compared to CMOS.

![Figure 3 (a) Views of the FinFET Layout](image3)

(Source: Choi et al. 2002)

Figure 3 (b) FinFET device structure

### III. PROPOSED METHOD

The different blocks of the adaptive identifier has the opamp and multiplier as the major blocks. The different blocks of the adaptive filter identifier is given below.
3.1. Analog Delay Line: The analog delay is a second order low-pass filter. The cut off frequency is fixed at 100 KHz and belongs to type Butterworth. To improve the rejection ratio the order can be increased but the bandwidth will reduce.

3.2. Operational Amplifier: To improve the gain and CMRR, a operational amplifier based low-pass filters is designed. In figure 4 shows the internal structure of operational amplifier using the CMOS technology in 32nm.

3.3. Integrator

An integrator is designed using low sensitive dual operational amplifiers. The addition and impedance matching is taken care by the amplifiers. The integrator is a low pass filter. The gain can be improved by adding a FET in resistive mode in parallel with the capacitor.

3.4. Four Quadrant Multiplier

To four quadrants multiplier swings between positive and negative makes suitable for analog multiplication. The voltage mode four quadrant multiplier implemented in MOSFET is shown in Figure 5.

The adaptive filter structure configured as a low-pass filter is shown in figure 6. The LMS algorithm is designed using the low pass filter, analog delays and coefficients update blocks. The summer block takes the buffered input of the transfer elements.

IV. RESULTS AND DISCUSSION

The implementation was carried out using HSPICE. The structure of the adaptive filter has delay line, analog adaptation unit based on CMOS, Integrators, adders and multipliers. The implementation was done using CMOS and FINFET. The table 1 shows the performance of the op-amp implemented using CMOS and FINFET.

Table 1. Performance of the op-amp implemented using CMOS and FINFET

<table>
<thead>
<tr>
<th>OPAMP</th>
<th>Average Current (A)</th>
<th>Average Power (W)</th>
<th>Average Energy (J)</th>
<th>Delay (sec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMOS</td>
<td>140.85x10^-6</td>
<td>58.934x10^-6</td>
<td>3.2134x10^-1</td>
<td>250.81x10^-1</td>
</tr>
<tr>
<td>FINFET</td>
<td>1.1236x10^-9</td>
<td>53.214x10^-1</td>
<td>1.2236x10^-2</td>
<td>999.38x10^-1</td>
</tr>
</tbody>
</table>

Table 2. Performance of the Multiplier block implemented using CMOS and FINFET

<table>
<thead>
<tr>
<th>MULTIPLIER BLOCK</th>
<th>Average Current (A)</th>
<th>Average Power (W)</th>
<th>Average Energy (J)</th>
<th>Delay (sec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMOS</td>
<td>156X10^-6</td>
<td>73X10^-6</td>
<td>6.3X10^-12</td>
<td>360.81X10^-1</td>
</tr>
<tr>
<td>FINFET</td>
<td>3.8X10^-9</td>
<td>49X10^-12</td>
<td>3.7X10^-21</td>
<td>1.38X10^-9</td>
</tr>
</tbody>
</table>

It can be observed that the FINFET based circuit. Table 2 shows the results observed on the design of four quadrant multiplier using CMOS and FINFET. Here also the FINFET based performance is better. The op-amp and multiplier forms the part of the various locks of the adaptive filter.

V. CONCLUSION AND FUTURE WORK.
The design of adaptive filters using FinFET circuit is addressed in this paper. The adaptive estimator using methods like ABC and PSO to be implemented in future are investigated and the basic blocks were implemented. The opamp and four quadrant analog multiplier was designed and implemented using CMOS and FINFET in this paper. The results were compared and the FinFET based design was found to be advantages and efficient when compared to the CMOS counterpart. The adaptive estimation can be extended to the multichannel signal inputs. The evolutionary methodology approach using Artificial Bee Colony and Particle swarm optimization efficiency can be improved if the adaptive filter implemented using FinFET.

REFERENCES


AUTHORS PROFILE

First Author Dr. Udara Yedukondalu currently working as a Associate Professor, Department of ECE, Sri Vasavi Engineering College, Tadepalligudem, A.P. He received B.Tech from CR Siddhartha Engineering College, Vijayawada, M.Tech from JNTUCE Kakinada. He awarded Doctorate in the area Low Power VLSI from Acharya Nagarjuna University, in the year 2017. He had 20 international publications.

Second Author VijayaSri Bolisetty currently working as a Associate Professor, Department of ECE, Aditya College of Engineering & Technology Surampalem, A.P. She had 8 international Publications.

Third Author Udana. Srinivasarao currently working as a Associate Professor, Department of ECE, STJHT, Ranebennur, Karnataka. He had 13 international Publications.