A FinFET Based Adaptive Filter Design Using Evolutional Algorithm for Noise Suppression

Udara Yedukondalu, V Vijayasri Bolisetty, Udara Srinivasarao

Abstract: ***This paper presents the implementation of an adaptive filter component using FINFET. The proposed is an analog adaptive filter based on CMOS algorithm. The existing CMOS based circuits suffer from short channel effects below 35nm. The proposed circuit reduces the power by reducing the leakage current. A FINFET based op-amp and four quadrants multiplier becomes the part of the adaptive filter. When compared to CMOS the FINFET based op-amp and four quadrants multiplier reduces the power. The evolutionary methodology approach using Artificial Bee Colony and Particle swarm optimization for the optimization of multichannel adaptive filter.***

Index Terms: CMOS, FINFET, adaptive filter, LMS, four quadrant multiplier, Op-amp.

I. INTRODUCTION

The advancement in VLSI design have made the electronics products as smaller as possible. This has happened due to the reduction of device size in nanoelectronics. Eventhough CMOS circuits are found to be efficient below 35nm the technology is troublesome. In biomedical and communication systems adaptive filters (Xinwang, 2010) plays a vital role in removal of noise and identification of signals. Evolutionary algorithm based filter design were investigated in past (Julian Miller,1999). Programmable filters have evolved in recent past to replace the conventional chips (Seo, 2018). A new approach to design a adaptive filter using evolutionary algorithm is implemented in FinFET.

For Noise cancellation adaptive filters were used due to its self-learning process. The filter coefficients are updated adaptively with respect to the noise strength. By adjusting the coefficients adaptively the error is minimized. The existing optimization techniques for adaptive filters are based on Least Mean-Square (LMS), gradient-based techniques., and Recursive Least-Square (RLS) method. The algorithms belongs to the gradient based techniques. These LMS and RLS based algorithm plays a vital role in designing digital noise cancellers in various applications like speech processing, extraction (Ravindrakumar and Bommannaraja (2014)) and speech enhancement (Goswami et al, 2014). But in literature several other optimization algorithms are presented. The methods are based on the particle swarm optimization, Artificial Bee Colony (Gao et al, 2013, Karaboga, 2010)), etc. methods. These optimization techniques were more suitable for adaptive equalization (Cheded et al, 2011). Zhao et al (2013) used the bee colony algorithm to design the digital filter design. The method was suitable for DSP application. Real parameter optimization was done using the ABC algorithm(Akay, B. and Karaboga, D. 2012). The global optimization increases when these optimization is used.

II. BACKGROUND METHODOLOGY

The block diagram of ANC filter with ABC is shown in Figure 1.

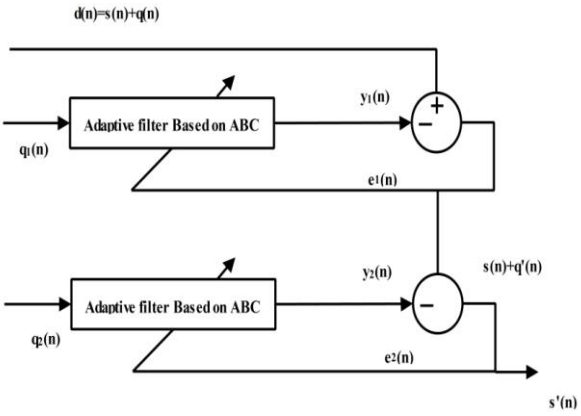

Figure 1. Adaptive filter using ABC.

2.1. ABC ALGORITHM

In ABC adaptive algorithm the position the bee position is equavated to the coefficient of the adaptive filter. The initial random population or the filter co-efficients are generated according to equation below

$$x_{ij} = x_{min,j} + rand(a) * (x_{max,j} - x_{min,j}) \quad (1)$$

'a' takes the value between -1 to +1.'i' is the colony size and j is the dimension value in the colony which represent the filter coefficient of the adaptive filter. The probability of optimized position or coefficient value is determined by the equation

$$p_i = \frac{fit_i}{\sum_{n=1}^{SN} fit_n} \quad (2)$$

Once new location are generated probability selection process is carried out with the fitness value fit and SN chosen index value.

To optimize the coefficient value the ABC algorithm uses a scaling factor (sf) which produces the

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minimum or zero error function. The best filter coefficient is found using the equation

$$x_{i,j} = \begin{cases} x_{min,j} + \phi_{i,j} * (x_{max,j} - x_{min,j}) & \text{for sf} \\ x_{min,j} & \text{otherwise} \end{cases} \quad (3)$$

The magnitude of perturbation is controlled by the scaling factor. The adaptive filter co-efficients are updated using the evolutionary methods. The algorithm can be applied to any number of channels. The LMS optimization of uses instantaneous estimation of vectors based on input d (n) and error e(n) using the below equation.

$$\nabla(n) = -2e(n)[d(n)] \quad (4)$$

In conventional methods the filter coefficients are updated as

$$[h(n+1)] = [h(n)] + \mu e(n)[d(n)] \quad (5)$$

Which is a gradient estimation.

The estimation requires the knowledge of data x(n) alone and not the knowledge of cross correlation.

$$e(n) = [h(n)] + \mu e(n)[d(n)] \quad (6)$$

In gradient vector estimate for multichannel system can be coined by the equation

$$d(n) = q_1(n)[F(n) + M(n) + q_2(n)] \quad (7)$$

Where d is the input and N is the noise representing low and high frequency component. The coefficient of the filter is estimated based on the data input and previous stage output.

2.2. PSO Algorithm for multichannel system

The PSO algorithm can be used to solve any nonlinear equations. Here a random swarm is initiated, velocity and position updates are made. The particle fitness is evaluated based on selected fitness function. The position is updated in each training update. The inertia weight parameters provides better efficiency and convergence.

In this method, for the best possible positions with least swarm is optimized.

$$p(n+1) = W(n) + \mu(n).O(error_c(n), d(n), \phi(n)) \quad (8)$$

2.3. **Modular structures**

The modular structure for a analog adaptable filter is shown in figure 2 (Jose,2008, Carusone and D.A. Johns,2000). The elements are transfer functions, integrators, multipliers and summers.

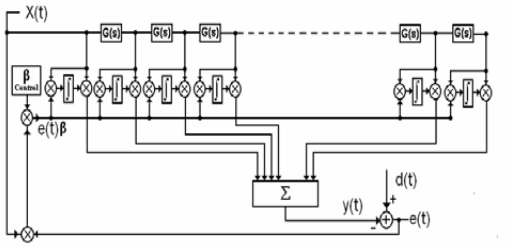


Figure 2. Adaptive Modular filter

The other modules are delay line and velocity control of convergence (Manish et al,2015).. Several architectures for on chip was also developed in literature (HyunMi et al,2018)(Kuan, 2018)

2.4. FinFET Device Structure

In the advancement of nanometer technologies the chip density and operating frequency have increased. The usage of power through battery is a main problem if the number of features is increasing in the application. The power supplies in non portable devices have different challenges in the design of cooling system and alternate power options. The other major concern is problems occurring due to high package density. Within the power budget the main design goal for VLSI is to be meeting with the required performance. The Fin type Field Effect Transistors (FinFET) replaces the bulk CMOS in 32 nm. The second order effects are troublesome when scaling of transistors are adopted (Prateek Mishra et al. 2011) for addressing the challenges posed by continued scaling. The fabrication of FinFET's is compatible with the CMOS which helps in rapid deployment.

New Integrated circuits are emerging in market using FinFET technology. Especially in computational and communication integrated circuits manufactured using advanced technologies like 65 nm and 45 nm.

Figure 3.(a) & (b) shows the FinFET transistor device layout and structure formed on Silicon On Insulator fabrication technique. It is a single gate stacked on top of two vertical gates. The device has very good control over current when compared to CMOS.

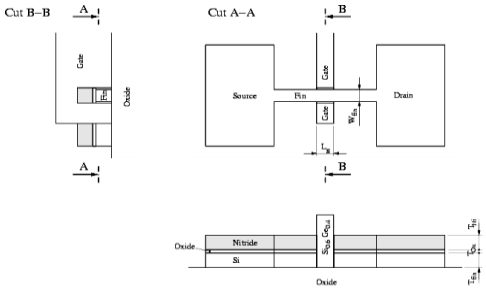
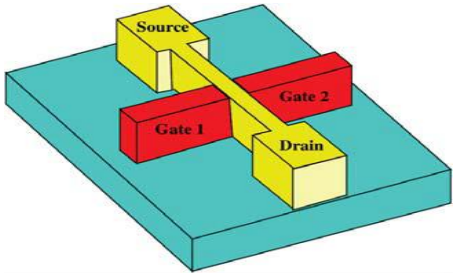


Figure 3 (a) Views of the FinFET Layout



(Source: Choi et al. 2002)

Figure 3 (b) FinFET device structure

III. PROPOSED METHOD

The different blocks of the adaptive identifier has the opamp and multiplier as the major blocks. The different blocks of the adaptive filter identifier is given below.

3.1. Analog Delay Line: The analog delay is a second order low-pass filter. The cut off frequency is fixed at 100 KHz and belongs to type Butterworth. To improve the rejection ratio the order can be increased but the bandwidth will reduce.

3.2. Operational Amplifier:

To improve the gain and CMRR, a operational amplifier based low-pass filters is designed. In figure 4 shows the internal structure of operational amplifier using the CMOS technology in 32nm.

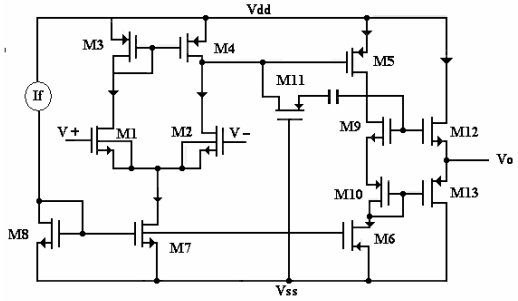


Figure. 4 Internal structure of operational amplifier.

3.3. Integrator

An integrator is designed using low sensitive dual operational amplifiers. The addition and impedance matching is taken care by the amplifiers. The integrator is a low pass filter. The gain can be improved by adding a FET in resistive mode in parallel with the capacitor.

3.4. Four Quadrant Multiplier

To four quadrants multiplier swings between positive and negative makes suitable for analog multiplication. The voltage mode four quadrant multiplier implemented in MOSFET is shown in Figure 5

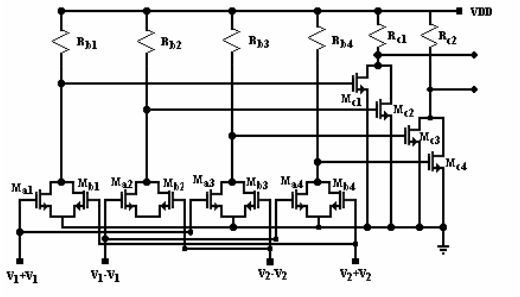


Figure 5. Four Quadrant Multiplier

The adaptive filter structure configured as a low-pass filter is shown in figure 6. The LMS algorithm is designed using the low pass filter, analog delays and coefficients update blocks. The summer block takes the buffered input of the transfer elements.

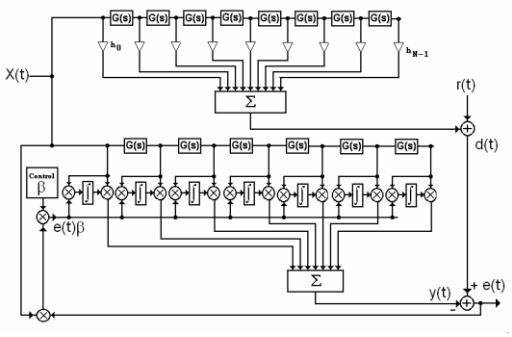


Figure 6. Adaptive filter used as identifier

The Proposed Opamp and Multiplier are designed using the FinFET device. The CMOS and FinFET based adaptive filter as a identifier is designed in 32nm technology. Since the fabrication is compatible with CMOS the cost factors are minimized. One such proposed design is this work where the circuit is adopted and implemented using FinFET. This eliminates the short channel effects, threshold voltage variation etc occurring in single Gate devices. The FinFET working is carried out in Short Gated Mode. The other modes independent and low power mode are not used in this work .

IV. RESULTS AND DISCUSSION

The implementation was carried out using HSPICE. The structure of the adaptive filter has delay line, analog adaptation unit based on CMOS, Integrators, adders and multipliers. The implementation was done using CMOS and FINFET. The table 1 shows the performance of the op-amp implemented using CMOS and FINFET.

Table 1. Performance of the op-amp implemented using CMOS and FINFET

OPAMP	Average Current (A)	Average Power (W)	Average Energy (J)	Delay (sec)
CMOS	140.85X10-6	58.934X10-6	3.2134X10-12	250.81X10-12
FINFET	1.1236X10-9	53.214X10-12	1.2236X10-21	999.38X10-12

Table 2. Performance of the Multiplier block implemented using CMOS and FINFET

MULTIPLIER BLOCK	Average Current (A)	Average Power (W)	Average Energy (J)	Delay (sec)
CMOS	156X10-6	73X10-6	6.3X10-12	360.81X10-12
FINFET	3.8X10-9	49X10-12	3.7X10-21	1.38X10-9

It can be observed that the FINFET based circuit. Table 2 shows the results observed on the design of four quadrant multiplier using CMOS and FINFET. Here also the FINFET based performance is better. The op-amp and multiplier forms the part of the various locks of the adaptive filter.

V. CONCLUSION AND FUTURE WORK.

The design of adaptive filters using FinFET circuit is addressed in this paper. The adaptive estimator using methods like ABC and PSO to be implemented in future are investigated and the basic blocks were implemented. The opamp and four quatrant analog multiplier was designed and implemented using CMOS and FINFET in this paper. The results were compared and the FinFET based design was found to be advantages and efficient when compared to the CMOS counterpart. The adaptive estimation can be extended to the multichannel signal inputs. The evolutionary methodology approach using Artificial Bee Colony and Particle swarm optimization efficiency can be improved if the adaptive filter implemented using FinFET.

REFERENCES

1. Julian F. Miller, "Digital Filter Design at Gate-level using Evolutionary Algorithms", in proceedings of GECCO'99 - 1st Annual Conference on Genetic and Evolutionary Computation, Orlando, Florida, pp. 1127-1134, 1999.
2. Jose E. Perez-Carmona, Hector M. Perez-Meana and Juan C. Sanchez-Garcia, "Analog adaptive filter LMS algorithm using CMOS 0.5 µm technology", World Scientific and Engineering Academy and Society Transactions On Circuits And Systems, vol. 7, no. 9, pp. 839-848, 2008.
3. H. Seo, B. Kim, J.-H. Chun, S.-J. Kim and J. Choi, "CMOS depth sensor with programmable filter circuits for environment-adaptive noise suppression", ELECTRONICS LETTERS, vol. 54, no. 19, pp. 1122-1124, 2018.
4. A.Carusone and D.A. Johns, "Analogue adaptive filters: past and present", in proceedings of IEE Proceedings - Circuits, Devices and Systems, pp. 82-90, 2000.
5. Manish Jaiswal, Sandeep Sharma and Anuj Sharma, "Implementation of high-speed–low-power adaptive finite impulse response filter with novel architecture", The Journal of Engineering, vol. 2015, no. 3, pp. 86-91, 2015.
6. HyunMi Kim, JeongGil Ko and Seongmo Park, "An Efficient Architecture of In-Loop Filters for Multicore Scalable HEVC Hardware Decoders", IEEE Transactions on Multimedia, vol. 20, no. 4, pp. 810-824, 2018.
7. Kuan-Yueh Shen, Syed Feruz Syed Farooq, Yongping Fan, Khoa Minh Nguyen, Qi Wang, Mark L. Neidengard, Nasser Kurd, and Amr Elshazly, "A Flexible, Low-Power Analog PLL for SoC and Processors in 14nm CMOS", IEEE Transactions On Circuits And Systems, vol. 65, no. 7, pp. 2109-2117, 2018.
8. Xinwang Zhang, Sina Balkır, Michael W. Hoffman and Nathan Schemm, "A Low-Power CMOS Continuous-Time LMS Adaptive Filter With Robust DC-offset Cancellation", in proceeding of 53rd IEEE International Midwest Symposium on Circuits and Systems, pp. 977-980, 2010.
9. Akay, B. and Karaboga, D. (2012) 'A modified artificial bee colony algorithm for real-parameter optimization', Information Sciences, Vol. 192, No. 1, pp.120–142.
10. Cheded, L., Zidouri, A., Al-Awami, A.T., Zerguine, A. and Saif, W. (2011) 'A new modified particle swarm optimization algorithm for adaptive equalization', Digital Signal Processing, Vol. 21, No. 2, pp.195–207.
11. Gao, W., Liu, S. and Huang, L. (2013) 'A novel artificial bee colony algorithm based on modified search equation and orthogonal learning', IEEE Transactions on Cybernetics, Vol. 43, No. 3, pp.1011–1024.
12. Goswami, S., Bardoloi, B., Deka, P., Dutta, D. and Sarma, D. (2014) 'A novel approach for design of a speech enhancement system using auto-trained NLMS adaptive filter', International Journal of Information and Communication Technology, Vol. 6, No. 3, pp.326–338.
13. Karaboga, D. (2010) 'Artificial bee colony algorithm', Springer Biomedical Engineering Letter, Vol. 5, No. 3, pp.69–75.
14. Krusienski, D.J. and Jenkins, W.K. (2003) 'Adaptive filtering via particle swarm optimization', Conference on Signals, Systems and Computers, Vol. 1, pp.571–575.
15. Ravindrakumar, **S** & Bommanna Raja, K, (2016), 'A Multi-Stage Adaptive Singular Value Decomposition Approach for Fetal ECG Signal Extraction in Multichannel Input System for Prenatal Health Monitoring', Asian Journal of Information Technology, vol. 15, no. 6, pp. 1049-1055.
16. Rodrigo P. Monteiro, Gabriel A. Lima,J. P. G. Oliveira ; D. S. C. Cunha ; Carmelo, 2017, 'Accelerating the convergence of adaptive filters for active noise control using particle swarm optimization ', Proceedings of Latin American Conference on Computational Intelligence (LA-CCI) 8-10 Nov. 2017, Peru
17. Zhao, Z., Yin, D. and Jiang, Y. (2013) 'Improved bee colony algorithm based on knowledge strategy for digital filter design', International Journal of Computer Applications in Technology, Vol. 47, No. 2, pp.241–248..

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