Low Power and high Speed Full Adder using new XOR and XNOR Gates

PygastiJuveria, K. Ragini,

Abstract. Six hybrid full adder circuits using new XNOR, XOR gates are proposed in this paper. These circuits are designed to havehigh speed and less power consumption compared to existing circuits. This is possible due to low output capacitance. Each one of the proposed full adder circuit has its own advantages of speed, power consumption and driving ability. Simulations are done in Tanner tool in 45-nm technology. From results, proposed circuits are found to be better thanexisting circuits. Also the performance of proposed full adder circuits is analysed by varying the supply voltage and output load.

Keywords. XOR-XNOR, full adder, transmission gate logic style, hybrid logic style, output driving capability

I. INTRODUCTION

Now a days, the usage of portable electronic devices has been increased enormously. These devices require to have less power consumption and high speed. While designing a system, power consumption is a parameter which is to be optimized for better system performance.In many circuits,which perform arithmetic operations, full adder is a fundamental block[2]. So the performance of full adder affects the performance of complete system [3]. Therefore, the system performance can be enhanced by enhancing the performance of full adder. Many full adder circuits were designed using various logic styles, each of them has its own merits and demerits [4]-[6]. The designs existing till now can be divided into 2 categories. They are static and dynamic styles. The advantage of static full adders is high reliability and they are simple having low power consumption.Dynamic full adders have less on chip area requirement compared to static full adders. One logic style favours one performance aspect whereas another logic style favours another performance aspect. Some important logic design styles are CMOS [5], DPL [6], TGA and TFA . Some full adders are designed using more than one logic style, called hybrid-logic style. These designs include the characteristics of various logic styles so that full adder performance can be increased.

II. PROPOSED XOR, XNOR CIRCUITS

Generally full adders are designed by using XNOR and XOR gates. The major power consumer in full adder is XOR or XNOR circuit. So the power consumption of the full adder can be reduced by minimizing the power consumption of XOR or XNOR circuit. Also, XOR or XNOR gate is used in many other circuits such as parity checking circuits and comparators. High speed and low power XOR, XNOR and simultaneous XOR-XNOR circuits are proposed in this paper.

2.1 XOR, XNOR CIRCUIT

Proposed XNOR, XOR circuits are shown in fig1. For all the input combinations these circuits give full swing output, because of using level restoring transistors, P4, N4 in XNOR, XOR circuits respectively. Because of absence of NOT gates in critical path, these circuits have less delay and low power consumption. Also, these circuits have good driving capability.

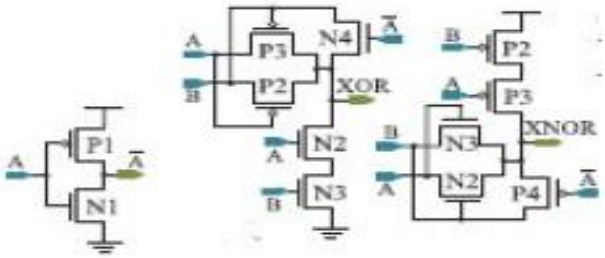

Fig 1. Proposed XOR, XNOR circuits

2.2 SIMULTANEOUS XOR-XNOR CIRCUIT

Proposed simultaneous XOR-XNOR circuit is obtained by combining both the circuits shown in fig 1. This circuit has 12 transistors. Fig 2 shows the circuit. This circuit has no NOT gates in critical path and it has small output capacitance. So the proposed simultaneous XOR-XNOR circuit has low power consumption and it is fast. The advantages are good driving capability and full swing output.

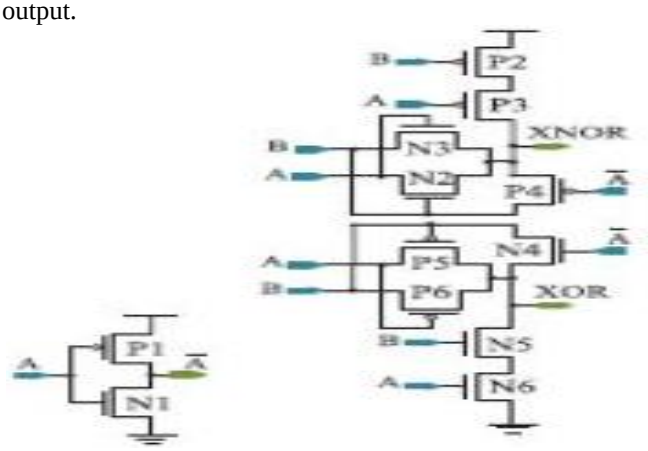

Fig 2. Proposed simultaneous XOR-XNOR circuit

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PygastiJuveria, student, G. Narayanamma institute of technology and science (for women), Hyderabad, Telangana, India.

Dr. K. Ragini, Professor, ECE Dept, G. Narayanamma institute of technology and science (for women), Hyderabad, Telangana, India.

III. PROPOSED FULL ADDERS

Using the proposed XOR, XNOR circuits, six new hybrid full adders are proposed. Fig 3 shows the proposed full adders. These circuits use hybrid logic style. Each proposed full adder use the proposed XOR or XNOR or simultaneous XOR-XNOR circuit and 2to1 multiplexer structure. Fig 4 shows the 2to1 multiplexer structure. This MUX uses transmission gates and has four transistors. This MUX circuit does not has static and short circuit power consumption. First full adder which is proposed is HFA-20T. Fig 3(a) shows the circuit of HFA-20T. It uses the simultaneous XOR-XNOR circuit shown in fig 2 and two 2-1-MUX structures. This full adder has 20 transistors. High power consuming NOT gates are not present on the critical path of this full adder. So it has high speed and less power dissipation. It gives full swing output and it is robust to supply voltage scaling. This circuit when used in the cascaded structures, its output driving capability reduces.

Fig 3(b) shows the second proposed full adder, HFA-17T. This uses XOR circuit of fig 1 and a NOT gate is used to generate XNOR signal from XOR circuit. Because of less number of transistors, HFA-17T has less power consumption than HFA-20T. But, the short circuit power consumption increases because of NOT gate on the critical path. So decrement in total power consumption of HFA-17T is not significant. HFA-17T has more delay than HFA-20T, because of NOT gates in the critical path of HFA-17T. The output driving capability of HFA-17T is improved a little because of this NOT gate.

Fig 3(c) shows third proposed hybrid full adder HFA-B-26T. It has 26 transistors and has buffers on sum and carry outputs. The XOR-XNOR circuit of fig 2 is used in this full adder.This has XOR-XNOR circuit, one 2to1 multiplexer structure and NOT gates in its critical path. The NOT gates that are placed at the outputs, prevent driving the output nodes by the circuit inputs. Also these NOT gates decrease the resistance from output node of circuit to sources (VDD and ground). HFA-B-26T has less speed and more power consumption compared to first two proposed full adder circuits.

Another proposed full adder, HFA-NB-26T, is shown in fig 3(d), in which buffers are kept at data input lines of 2to1 multiplexer. If the data inputs, A and C_i, for the multiplexer are generated from buffer, then for any input combination, the outputs will not be driven by circuit inputs. An XOR-XNOR circuit and a 2to1 multiplexer structure are present in thecritical path of HFA-NB-26T so it has high speed compared to HFA-B-26T.

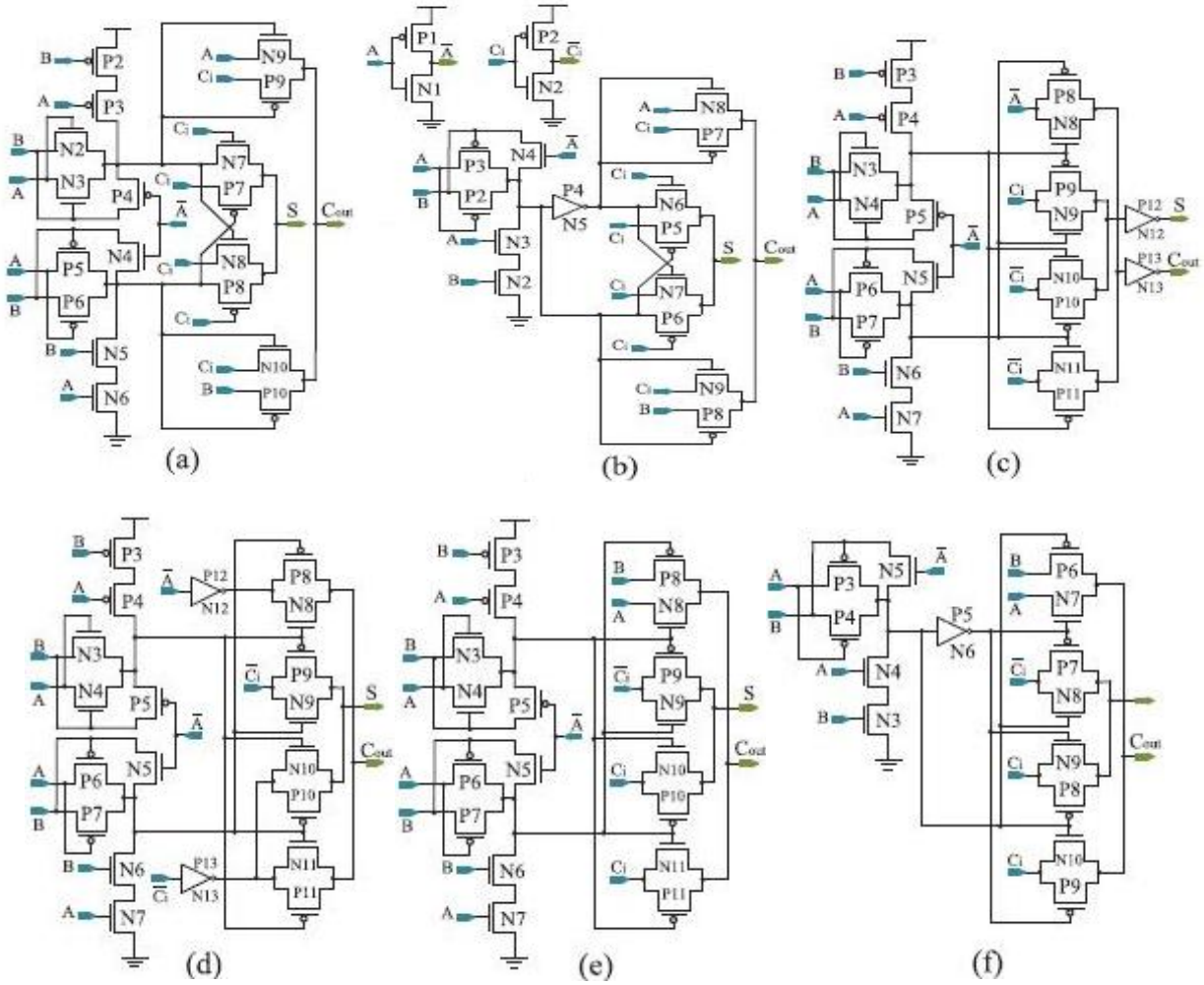

Fig 3. Proposed hybrid full adders

Fig 4. Structure of 2-1-MUX

But HFA-NB-26T has less driving capability than HFA-B-26T, because of existence of 2to1 multiplexer structure between output node and buffer.

Two more full adders HFA-22T and HFA-19T, shown in fig 3(e) and (f) respectively, are designed by modifying HFA-20T and HFA-17T respectively. In these circuits, sum output is generated by using$C_i$bar signal. Sum output is not driven by XOR and XNOR signals through transmission gate multiplexer because they are connected to the data select lines of multiplexer. Therefore, XOR and XNOR node capacitance reduces and circuit delay improves. So HFA-19T has less delay and power consumption compared to HFA-17T and HFA-22T has less delay and power consumption compared to HFA-20T. By using $C_i$bar signal, HFA-22T has better driving capability compared to HFA-20T and HFA-19T has better driving capability compared to HFA-17T respectively.

IV. SIMULATION RESULTS AND DISCUSSION

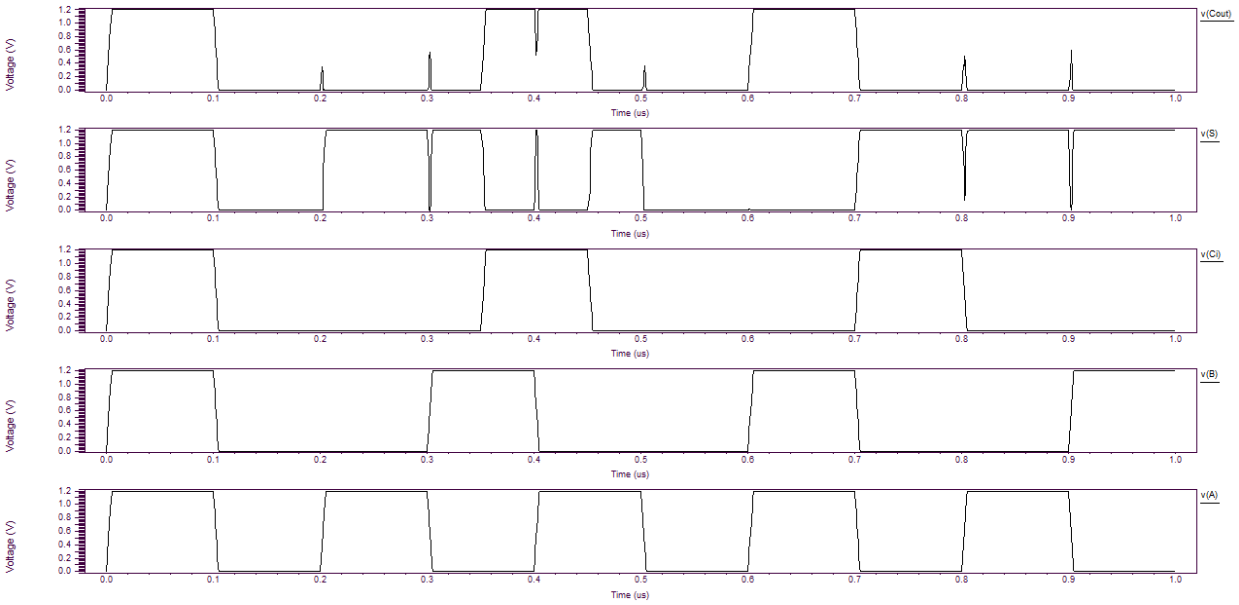

Fig 5. Simulation waveform of HFA-20T

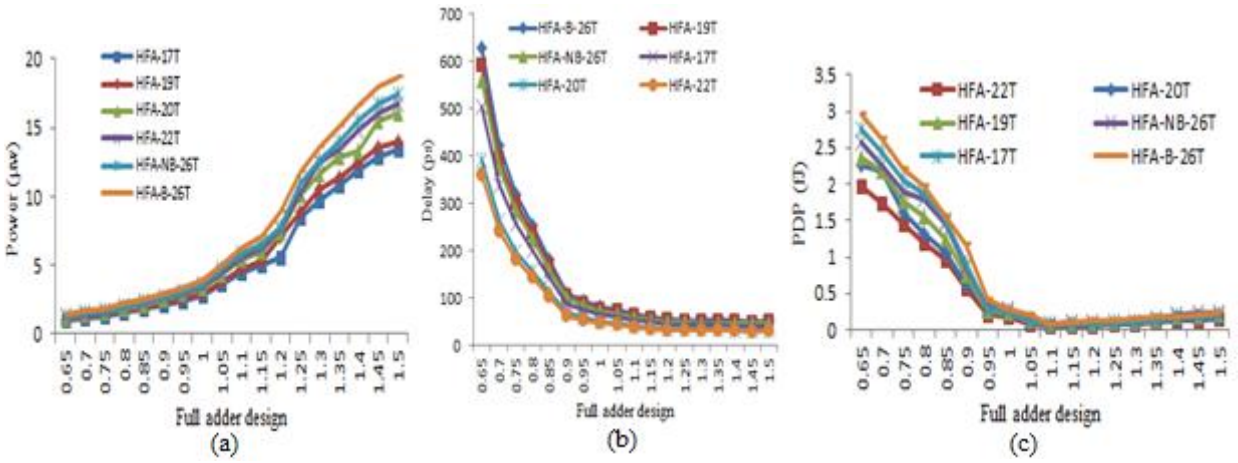

Fig 6. Simulation results of the proposed full adders by varying VDD (a) power consumption (b) delay (c) PDP

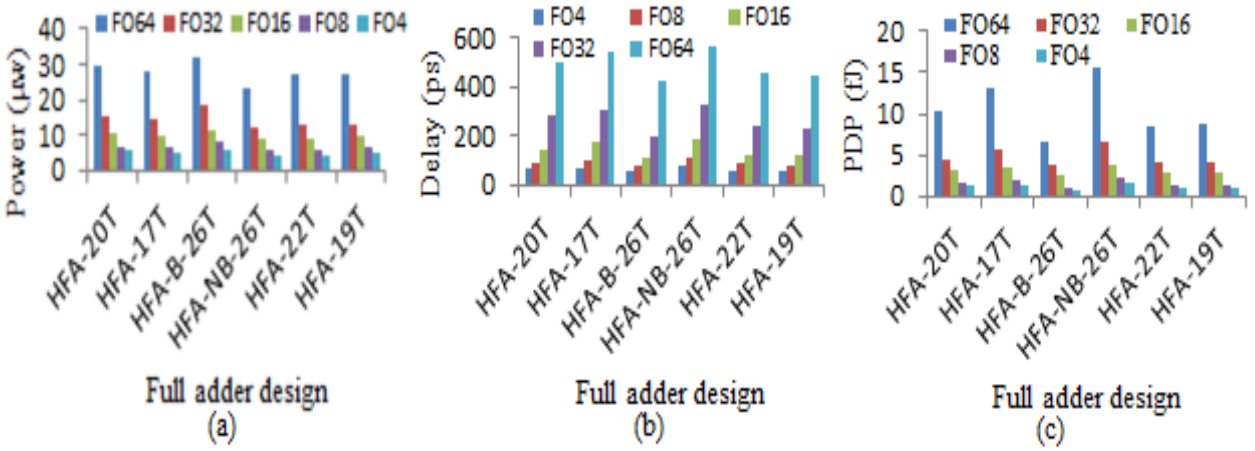

Fig 7. Simulation results of proposed full adders with output load variation(a) power consumption (b) delay (c) PDP

All simulations are done in Tanner tool in 45nm technology. The power supply used for simulations is 1.2v. Fig 5 shows thesimulation waveform of HFA-20T and table 1 shows the simulation results of proposed full adders. HFA-22T has minimum delay and PDP.

Table 1. Simulation results of proposed full adder circuits

Circuit	Power consumption (µw)	Delay (ps)	PDP (fJ)
HFA-20T	5.72	8.75	0.050
HFA-17T	5.66	8.96	0.052
HFA-B-26T	14.62	11.83	0.173
HFA-NB-26T	14.32	11.19	0.160
HFA-22T	8.26	5.79	0.048
HFA-19T	8.18	6.85	0.056

4.1 **Performance Analysis Of Proposed Full Adders By Varying Vdd:**

The proposed full addersperformance is analysed by varying VDD from 0.65 to 1.5v. The results of the simulation for proposed full adders by varying the supply voltage are shown in fig 6. All the proposed full adders work well even for small supply voltage of 0.65v.

4.2 **Performance Analysis Of Proposed Full Adders By Varying Output Load:**

By varying the output load from fan out 4 to fan out 64 (FO4 to FO64), the proposed full adders performance is analysed. The supply voltage of 1.2v is used for simulations. The simulation results of proposed full adders by varying the output load are shown in fig7. For the output load of FO64, HFA-NB-26T has the highest PDP.

V. CONCLUSION

The proposed full adders have high speed and less power consumption because of using new proposed XNOR, XOR circuits. The proposed full adders have good driving capability and less output capacitance. From simulation results, the proposed full adders have low power consumption, less delay and best power delay productcompared to existing circuits. The proposed full adders work reliably at various VDD values from 0.65-1.5v. And also the proposed full adders work reliably at various output loads.

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