A Novel Symmetrical & Asymmetrical Reduced-Switch Topologies for Grid Tied PV Systems

Ch. Punya Sekhar, P. V. Ramana Rao, M. Uma Vani

Abstract*:Multi-level Inverter topology sustains the emergence of modish power-electronic converter as an expressive substitute to the formal two-level inverters in the area of high power mid-voltage energy conversion systems. Multilevel inverter recommends the most outstanding solution for high-power applications particularly in grid-integrated distributed generation scheme; there has been key interest in establishment of novel multilevel inverter structures with fewer switching components. This paper introduces the novel symmetric five-level and Asymmetric seven-level reduced-switch multilevel inverter topologies and administered by novel advanced multi-carrier pulse-width modulation scheme. The proposed multilevel inverter topologies are highly offered in distributed generation applications. For generation of three phase 7-level output voltage, the traditional topologies requires 36 switches and the proposed topology needs only 18 switches acquires the fewer switching elements, low gate drive circuits, low cost, minimum space requirement, low voltage dv/dt switch stress, low switching loss and high efficiency. The performance analysis of proposed symmetric five-level and Asymmetric seven-level reduced-switch inverter topologies has been carried-out by using Computer Simulation tool; the respective simulation results illustrates the RMS voltage quality, low THD, low LC filter units.

***Index Terms*: Distributed Generation, Grid-Connected System, Multi-Level Inverter, Multi Carrier Pulse Width Modulation, Renewable Energy Sources, Total Harmonic Distortion.**

I. INTRODUCTION

Recent days, the Distribution Generation (DG) plays a vital role in remote areas to acquire the power demand by utilizing renewable energy sources where the utility grid is non-presence [1]. Renewable energy sources (RES) have immense development due to increased energy demand, clean energy, and reduced fossil fuels. Several energy sources like solar, fuel cell and wind energy conversion systems (WECS) are interfaced to grid/load by utilizing power conditioning units. In that power conditioning units, DC-AC inverter topology plays a crucial role in modern set-up of Distributed generation scheme and also used in many mid-voltage high power range applications. The DC-AC inverter structure is appointed by smart power-semiconductor switches/diodes, commonly MOSFETs and IGBTs are used in DC to AC conversion topologies. Schematic block diagram of renewable energy conversion scheme is depicted in Fig.1. Based on nature of outcome voltage waveform, inverters can be categorized as square-wave VSI, quasi-square wave VSI. These inverter structures have more harmonic distortions at output voltage waveform, which affects the grid code standards and requires high range filter circuitry, greater switching stress, etc.

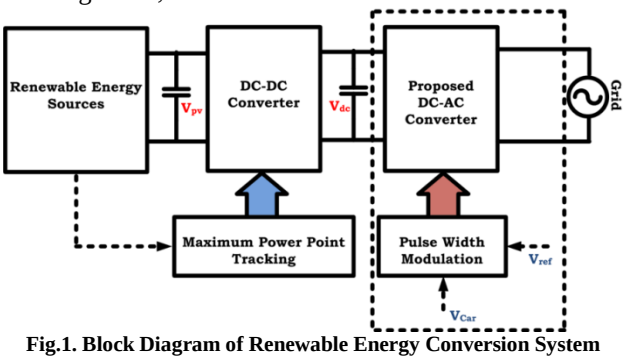

Fig.1. Block Diagram of Renewable Energy Conversion System

The appearance of modern power-electronic devices, a multilevel inverter (MLIs) is getting more favourable to enhance the performance of DG based renewable power generation scheme and also other futuristic power semi-conductor utilities in high-power medium voltage applications [2]. Generally,multilevel inverters furnishes the stair-case outcome voltage with respect to superior quality of RMS voltage/current waveform under the desired spectrum, low THD content, minimized voltage stress over the switches, low electro-magnetic compatibility, incredible efficiency, etc [3].The acquired outcome voltage is unified by significant switching of various DC-link voltages, which deals to reduce the dv/dt stress on switches and enhances the quality waveform [4], [5]. Traditionally, MLI structures are categorized as diode-clamped type [6], flying capacitor type [7] [8], as well as cascaded H-bridge MLI type [9]-[11], which can be comprised of dual strategies such as symmetrical and asymmetrical topologies. Over the other MLI topologies, the cascaded H-Bridge MLI is sovereign by many years for several industrial and commercial applications. Moreover, the traditional CHB-MLI is un-popular due to requirement of more switching devices for greater number of voltage levels. The main motivation of proposed concept is to minimize the switching elements, low cost, low size, reduced gate-drive circuits, low switching loss, and influences the high efficiency, reliability.

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Along with the anatomy of the traditional MLI topologies, several researchers render the prominent effort to evolve novel MLI topologies with low number of switches with good harmonic profile [12]. Multi-level inverter topologies are driving by both voltagepulse method and multi-carrier controlled methods [13], [14]. The multi-carrier modulation techniques are used to acquire the qualitated RMS voltage/current waveform with the requirement of low rated filter units, low total harmonic distortions (THD) [15]. The importance of study is carried on several multi-carrier pulse-width modulation techniques are sinusoidal reference based Phase-shifting modulation (PSPWM) technique, Level-shifting modulation (LSPWM) technique [16] and Space-Vector modulation (SVPWM) technique [17] are reviewed by so many researchers to control the MLI output waveform.

This paper proposes, the novel symmetric 5-level single/three phase MLI topologies are validated and implemented by advanced multi-carrier pulse-width modulation technique. The major need of proposed asymmetric inverter topology is to reduce the fewer switches and have favourable benefits are low gate drive circuits, reduced size, low cost, low switch stress and high efficiency can be attained over the formal inverter topologies. The detailed simulation analysis of proposed 5-level& 7-level Reduced-Switch Multilevel Inverter (RSMLI) performance is carried out by using computer simulation tool, results are illustrated.

II. PROPOSED SYMMETRIC & ASYMMETRIC RSMLI TOPOLOGIES

The proposed 5-level symmetric and 7-level Asymmetric RSMLI topology requires equal DC sources, equal switches, gate drive circuits, but the difference is input DC source as equal and Non-equal DC source. The proposed 5-level topology requires equal DC-link voltage as (V_{dc1}=V_{dc2}) and coming to asymmetric 7-level topology requires un-equal DC-link voltages as (V_{dc1}≠V_{dc2}), ultimately the final outcome voltage is attained by series action of two DC-link voltages as (V_{dc}=V_{dc1}+V_{dc2}). The proposed MLI topologies are clearly explained with respect to operating modes.

A. Proposed Symmetric RSMLI 5-Level Topology

The proposed 5-level symmetric RSMLI topology is comprised of six MOSFET switches, two equal DC sources, switching sequences and one resistive load. The definite DC voltage is transformed to the output terminals and the required five output voltage levels (0V_{dc}, V_{dc}, 2V_{dc}, -V_{dc}, and -2V_{dc}) are generated by switching the appropriate switches as a certain manner. Appropriate 5-level AC output voltage is acquired at load with respect to gate drive pulses, the switching sequences are clearly illustrated in Table.1. In Table.1, the "H" represents the Conduction of respective switch and "L" represents the Non-Conduction of switch, the operating modes of proposed symmetric 5-level RSMLI topology is illustrated in Fig.2.

To produce a voltage level of V_0=0, the switches S_3, S_4 and S_5 are conducted, then the respective voltage across the load point is zero V_{dc} because of short-circuit as shown in Fig.2 (a). To produce a voltage level of V_0=Vdc, S_1, S_6 and S_5 are conducted at the positive half-cycle, pertained voltage is furnished by the V_0=V_{dc1} and the voltage across the load terminal is Vdc as shown in Fig.2 (b).

Table.1. Switching Sequences of Proposed 5-Level Symmetric RSMLI Topology-1

Outcome Voltages	S_1	S_2	S_3	S_4	S_5	S_6
V_{dc}	H	L	L	L	H	H
$2V_{dc}$	H	L	H	L	H	L
$-V_{dc}$	H	H	H	H	L	L
$-2V_{dc}$	L	H	L	H	L	H
$0\ V_{dc}$	L	L	L	H	H	H

To produce a voltage level of V_0=2Vdc, S_1, S_5 and S_3 are conducted at the positive half-cycle, pertained voltage is furnished by the V_0= (V_{dc1}+V_{dc2}) and the voltage across the load terminal is 2Vdc as shown in Fg.2(c). To produce a voltage level of V_0=-Vdc, S_2, S_3 and S_4 are conducted at the negative half-cycle, pertained voltage is furnished by the V_0= V_{dc1} and the voltage across the load terminal is –Vdc as shown in Fig.2 (d). To produce a voltage level of V_0=-2Vdc, S_2, S_6 and S_4 are conducted at the negative half-cycle, pertained voltage is furnished by the V_0= (V_{dc1}+V_{dc2}) and the voltage across the load terminal is -2Vdc as shown in Fig.2 (e).

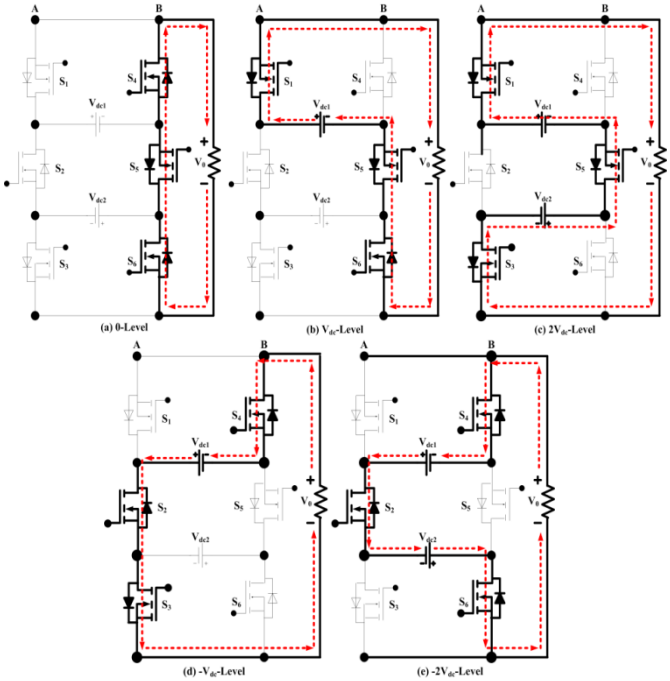


Fig.2. Operating Modes of Proposed 5-level Symmetric RSMLI Topology

Several multi-carrier switching pattern schemes are used in multi-level inverters to control the output voltage waveform at load terminals. Generally, modulation strategies are comprised into three objectives, such as voltage PWM technique, multi-carrier PWM techniques, space-vector PWM technique [18]-[20].

Out of all, the multi-carrier based PWM technique is most favourable due to its low complex control function, good controllability, low switch stress, low EMI compatibility and highly suitable for more number of levels. This paper employs the advanced multi-carrier PWM scheme requires sinusoidal reference signal (V_{ref}) were compared with a dual carrier signals (V_{car1}, V_{car2}).

All the carriers had high switching frequency with a little difference in peak

magnitude which is vertically disposed. The reference signal coming from control objective is compared with dual carrier signal to generate the switching states of A and B. These switching states A and B are controlled by additional pulse generated switching state C. The generation of optimal pulses to the proper switches is defined by mathematical notation which is depicted in Eqn. (1) to Eqn. (6). The switching sequence of the proposed symmetric 5-level symmetric MLI is depicted in Fig.3.

$$S1 = \bar{A}C + \bar{C} \quad (1)$$
$$S2 = C \quad (2)$$
$$S3 = \bar{B}C + \bar{A}\bar{C} + B\bar{C} \quad (3)$$
$$S4 = AC \quad (4)$$
$$S5 = \bar{C}A \quad (5)$$
$$S6 = BC \quad (6)$$

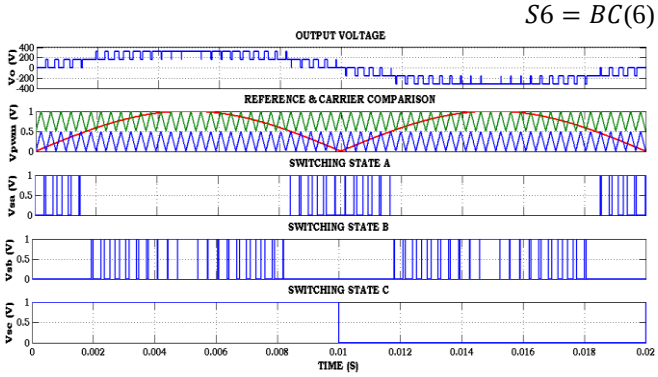


Fig.3. Switching Pattern Scheme

B. Proposed Asymmetric RSMLI 7-Level Topology Using Same Switches

The proposed 7-level Asymmetric RSMLI topology is comprised of six MOSFET switches, two un-equal DC sources, switching sequences and one resistive load. The definite DC voltage is transformed to the output terminals and the required seven-level output voltage are ($0V_{dc}$, V_{dc}, $2V_{dc}$, $3V_{dc}$ $-V_{dc}$, $-2V_{dc}$, and-$3V_{dc}$) generated by switching the appropriate switches as a certain manner. Appropriate 7-level AC output voltage is acquired at load with respect to gate drive pulses, the switching sequences are clearly illustrated in Table.2. In Table.2, the "H" represents the Conduction of respective switch and "L" represents the Non-Conduction of switch, the operating modes of proposed Asymmetric 7-level RSMLI topology is illustrated in Fig.4.

Table.2. Switching Sequences of Proposed 5-Level Symmetric RSMLI Topology-1

Outcome Voltages	S_1	S_2	S_3	S_4	S_5	S_6
V_{dc}	H	L	L	L	H	H
$2V_{dc}$	L	L	H	H	H	L
$3V_{dc}$	H	L	H	L	H	L
$-V_{dc}$	L	H	H	H	L	L
$-2V_{dc}$	H	H	L	L	L	L
$-3V_{dc}$	L	H	L	H	L	H
$0\ V_{dc}$	L	L	L	H	H	H

To produce a voltage level of V_0=0, the switches S_3, S_4 and S_5 are conducted and the voltage across the load point is zero because of short-circuit as shown in Fig.4 (a). To produce a voltage level of V_0=Vdc, S_1, S_6 and S_5 are conducted at the positive half-cycle, pertained voltage is furnished by the V_0=V_{dc1} and the voltage across the load terminal is Vdc as shown in Fig.4 (b). To produce a voltage level of V_0=2Vdc, S_4, S_5 and S_3 are conducted at the positive half-cycle, pertained voltage is furnished by the V_0= (V_{dc2}) and the voltage across the load terminal is 2Vdc as shown in Fg.4(c). To produce a voltage level of V_0=3Vdc, S_1, S_5 and S_3 are conducted at the positive half-cycle, pertained voltage is furnished by the V_0= (V_{dc1}+V_{dc2}) and the voltage across the load terminal is 3Vdc as shown in Fg.4 (d).

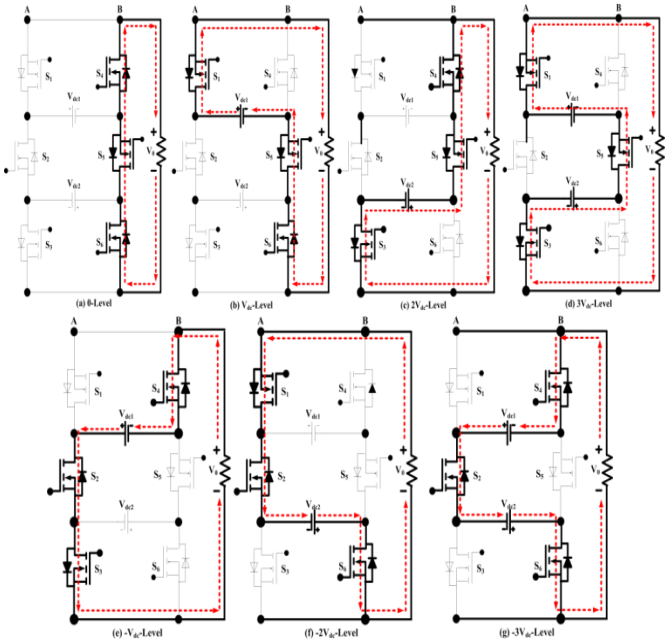


Fig.4 Operating Modes of Proposed 7-level Asymmetric RSMLI Topology

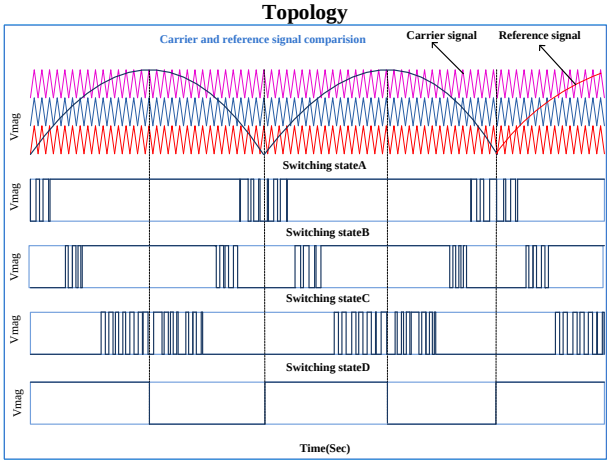


Fig.5. Switching Pattern Scheme

To produce a voltage level of V_0=-Vdc, S_2, S_3 and S_4 are conducted at the negative half-cycle, pertained voltage is furnished by the V_0= V_{dc1} and the voltage across the load terminal is –Vdc as shown in Fig.4 (e). To produce a voltage level of V_0=-2Vdc, S_2, S_6 and S_1 are conducted at the negative half-cycle, pertained voltage is furnished by the V_0= (V_{dc2}) and the voltage across the load terminal is -2Vdc as shown in Fig.4 (f). To produce a voltage level of V_0=-3Vdc, S_2, S_6 and S_4 are conducted at the negative half-cycle, pertained voltage is furnished by the V_0= (V_{dc1}+V_{dc2}) and the voltage across the load terminal is -3Vdc as shown in Fig.2 (g).

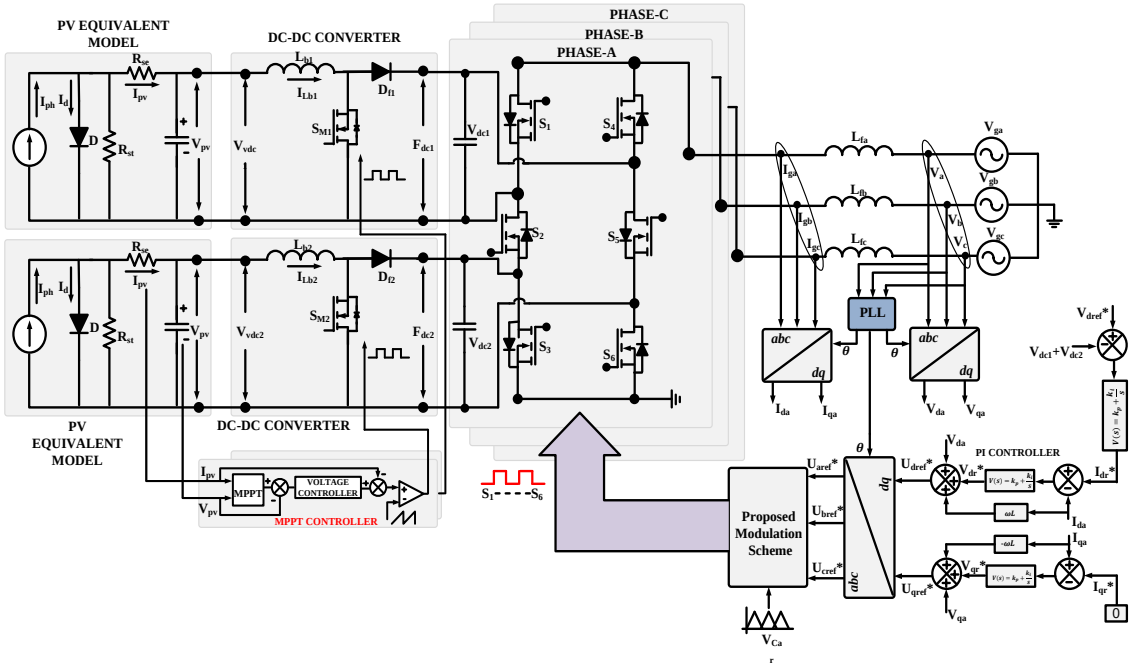


Fig.6. Schematic Representation of Proposed Three Phase Asymmetric 7-Level RSMLI Topology for Grid Integrated DG System

The generation of optimal pulses to the proper switches is defined by mathematical notation which is depicted in Eqn. (7) to Eqn. (11). The switching sequence of the proposed Asymmetric 7-level Asymmetric MLI is depicted in Fig.5.

$$S_1 = \bar{A}D + B\bar{C}D + \bar{B}\bar{D} + C\bar{D} \quad (6)$$

$$S_2 = D \quad (7)$$

$$S_3 = \bar{B}D + \bar{A}\bar{D} + B\bar{D} \quad (8)$$

$$S_4 = \bar{B}DA + CD + B\bar{C}\bar{D} \quad (9)$$

$$S_5 = A\bar{D} \quad (10)$$

$$S_6 = BD + A\bar{B}\bar{D} \quad (11)$$

The schematic representation of proposed three-phase Asymmetric 7-level multi-level Inverter topology for grid integrated DG system is depicted in Fig.6. The proposed grid-integrated DG application is driven by renewable energy by assisting the power-conversion equipments like MPPT controlled DC-DC converter and proposed DC-AC MLI topologies. The energy coming from PV arrays is directly interacted to DC-link capacitors (V_{dc1}) & (V_{dc2}) by utilizing DC-DC boost converter. It transforms low-level DC voltage into high level voltage with a high step-up ratio with help of Maximum-Power Point Tracking (MPPT) controller to attain constant DC-link voltages. The DC-link capacitors acts as primary sources of proposed MLI topologies for generation of optimum switching states for acquiring certain voltage levels by utilizing the Synchronous-Reference-Frame (SRF) control theory [21]. The *dq* control or SRF control scheme is shown in above schematic diagram; generally the outcome current is in-line with grid-voltage, to represent unity power factor. The phase-angle (θ) used by *abc-dq* transformation is obtained from the utility grid voltage (V_{gabc}), the phase-information of utility-grid is adopted by Phase-Locked Loop (PLL) to transform the *abc* quantities into *dq* frame or vice-versa [22]. The dual PI regulators are appointed to regulate the i_d and i_q currents concurred to the reference current components i_{dr}* and i_{qr}* which influences the active and reactive power exchanging with utility grid respectively. The reference i_{dr}* is generated by differentiating both actual and reference DC-link voltages (V_{dc1}& V_{dc2}) and (V_{dcref}*), then getting outcome error [23]. The outcome error is attained when compared and regulated by PI controller attains reference current component i_{dr}* and the i_{qr}* is set as '0'. This reference i_{dr}* & i_{qr}* currents are again compared to actual line currents in *dq* frame and the error is regulated by PI controllers to attain reference voltage vector in *dq* frame. The reference voltage vector V_{dr}* & V_{qr}* is combined with actual grid voltage vectors in *dq* frame is V_{da}&V_{qa}, for getting final reference voltage signal in *dq* frame is U_{dref}* &U_{qref}*. These reference voltage vectors is re-transformed into *abc* quantities by using inverse-transformation process, the final reference voltage signals in *abc* frame is U_{aref}*, U_{bref}*, U_{cref}*. An attractive proposed Pulse-Width Modulation (PWM) scheme utilizes reference voltage signal for generation of optimal switching states to symmetric and Asymmetric MLI topologies under grid-connected scheme.

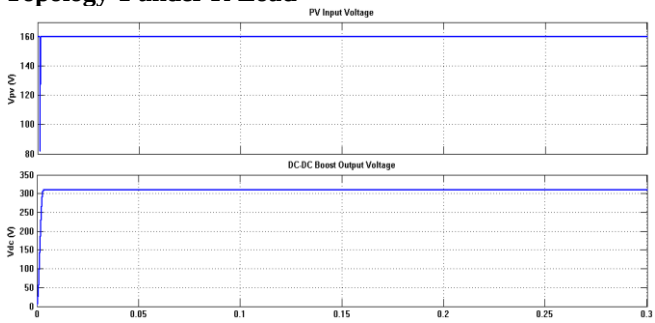
III. MATLAB/SIMULINK RESULTS

The simulation analysis is conveyed by proposed three-phase symmetric 5-Level & Asymmetric 7-level RSMLI topologies under proposed multi-carrier PWM techniques. The simulation analysis is carried-out under R-load connected system and grid connected scheme, the system specifications are illustrated in Table.3.

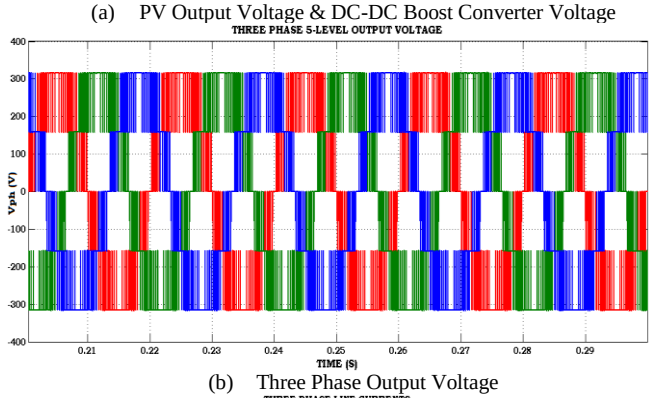
Table.3 Operating Specifications

S.No	Parameters	Values
01	PV Input Voltage	150 V
02	PV Output Power	2.5 KW
03	DC-Link Voltage	Symmetrical: V_{dc1}= V_{dc2}=160V
		Asymmetrical: V_{dc1}=133.3 V V_{dc2}=266.6V
04	Switching Frequency	5KHz
05	Inductors	L_{abc}=25µH;
06	Capacitors	C_{dc1}= C_{dc2}=1000 µF

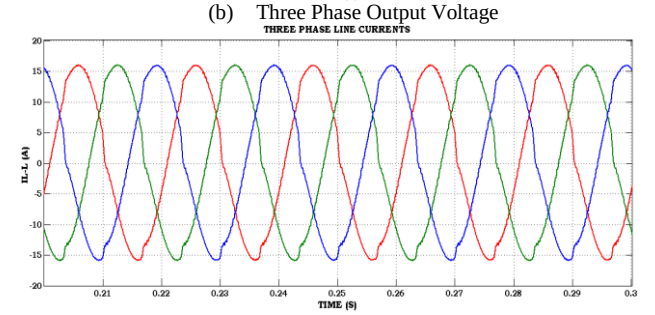
C. Proposed Three Phase Symmetric 5-Level RSMLI Topology-1 under R-Load



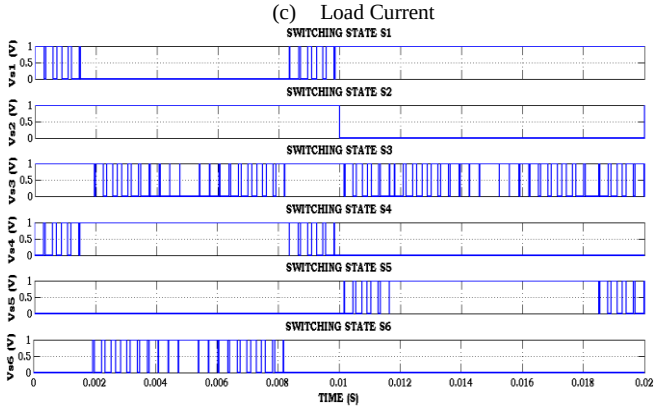
(a) PV Output Voltage & DC-DC Boost Converter Voltage



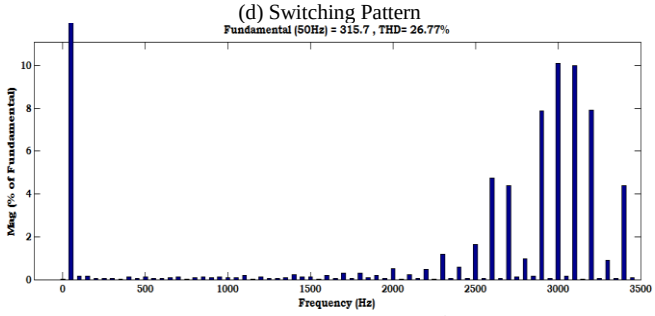
(b) Three Phase Output Voltage



(c) Load Current



(d) Switching Pattern

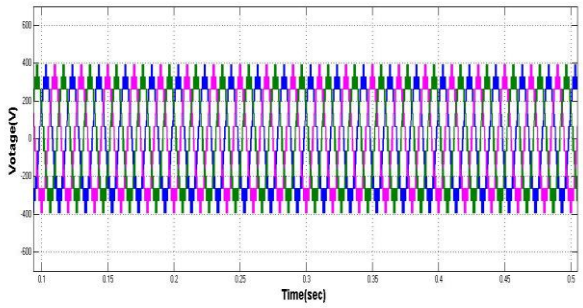


(e) Harmonic Spectrum Analysis of Output Voltage

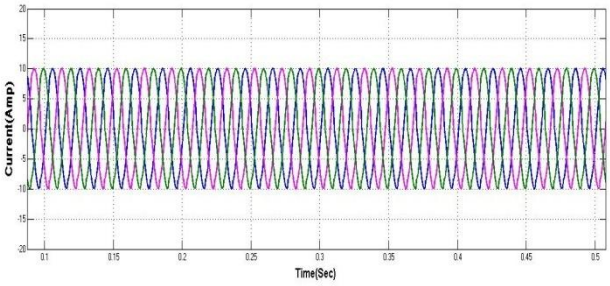
Fig.7. Simulation Results of Proposed Three Phase Symmetric 5-Level RSMLI Topology-1 under R-Load using Multi-Carrier PWM Scheme

The simulation results of proposed symmetric 5-level RSMLI topology-1 under advanced multi-carrier PWM technique are illustrated in Fig.7 and represented as (a) PV & DC-DC Boost Output Voltage, (b) Three phase output voltage, (c) Load current, (d) Switching pattern, (e) Harmonic spectrum analysis of output voltage. The DC-DC converter transforms the low-level input voltage to high-level required voltage from solar PV arrays for achieving load. The output voltage shows the desired 5-level voltage by utilizing 18 switches instead of 24 switches compared to three-phase cascaded H-bridge MLI topology. The exact 120^{o} phase displacement is also attained in proposed 5-level symmetric inverter by requiring the fewer switching devices. The output load current also acquiring the near sinusoidal RMS current wave-shape and harmonic spectrum analysis of output voltage is 26.77%. By using high range switching frequency, the harmonics are shifted from low-order to high order influencing the minimization of the load side filter size.

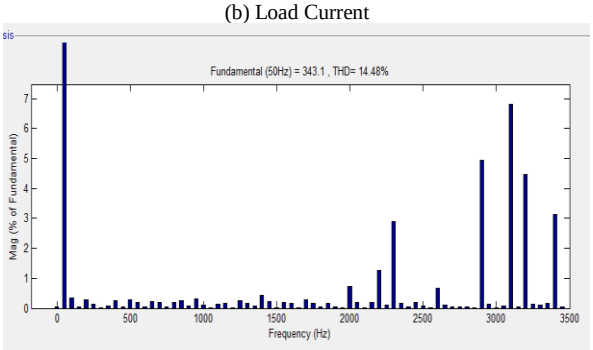
D. Proposed Three Phase Asymmetric 7-Level RSMLI Topology-2 under R-Load



(a) Three Phase Output voltage



(b) Load Current



(c) Harmonic Spectrum Analysis of Output Voltage

Fig.8. Simulation Results of Proposed Three Phase Asymmetric 7-Level RSMLI Topology-2 under R-Load using Multi-Carrier PWM Scheme

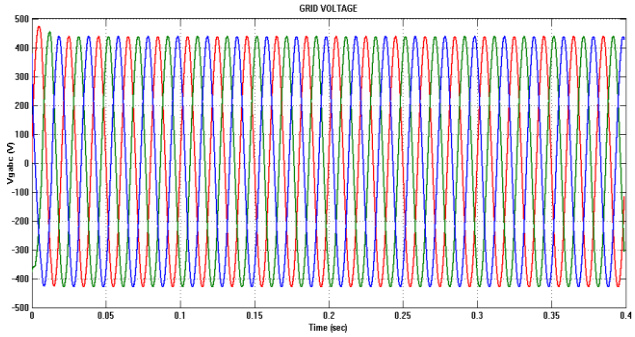
The simulation results of proposed Asymmetric 7-level RSMLI topology-2 under advanced multi-carrier PWM technique are illustrated in Fig.8 and represented as (a) Three phase output voltage, (c) Load current, (d) Harmonic spectrum analysis of output voltage. The output voltage shows the desired seven-level voltage by utilizing18 switches instead of 36 switches over the traditional three-phase cascaded H-bridge MLI topology.The output load current also acquiring the near sinusoidal RMS current wave-shape and the

harmonic spectrum analysis of output voltage is 14.48%. By attaining higher number of output staircase levels which increases the near sinusoidal output voltage, minimized filter size. Table.2 represents the comparison of different aspects of traditional and proposed multi-level inverter topologies. Over the traditional CHB-type, the proposed MLI topology requires low switches and input DC-link terminals for getting same voltage levels. The number of switches is reduced, getting low dv/dt stress, attaining high efficiency, low cost, low space and highly applicable to grid-connected scheme.

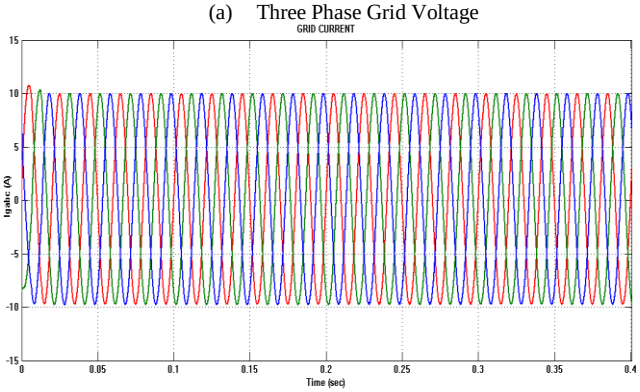
Table.2. Comparison of Traditional & Proposed RSMLI Topologies

	Cascade H-Bridge Topology		Proposed Topology	
	Symmetric 5-level [9]	Symmetric 7-level [10]	Symmetric 5-level	Asymmetric 7-level
Input DC Sources	6	9	6	6
Generalized formula for switch count	$4\left(\frac{Level-1}{2}\right)*3$		$3\left(\frac{Level-1}{2}\right)*3$	$2\left(\frac{Level-1}{2}\right)*3$
Switches (Three-Phase)	24	36	18	18

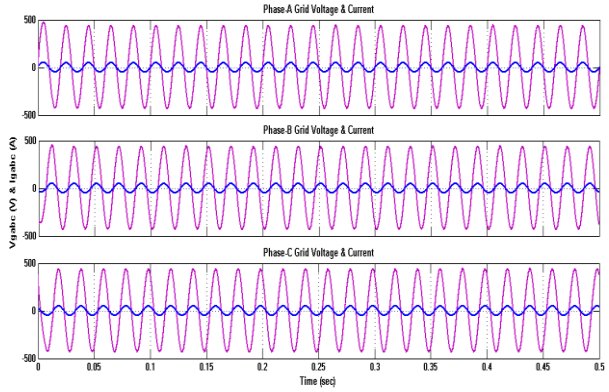
E. Proposed Three Phase Asymmetric 7-Level RSMLI Topology-2 under Grid Connected Scheme



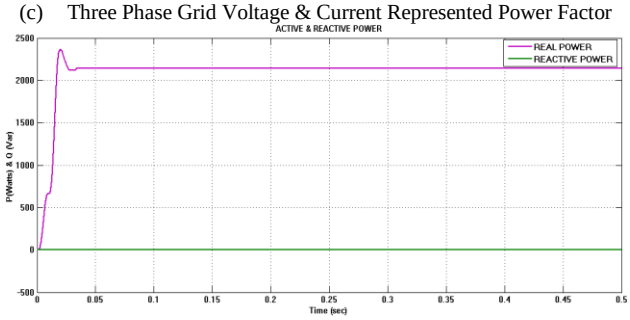
(a) Three Phase Grid Voltage



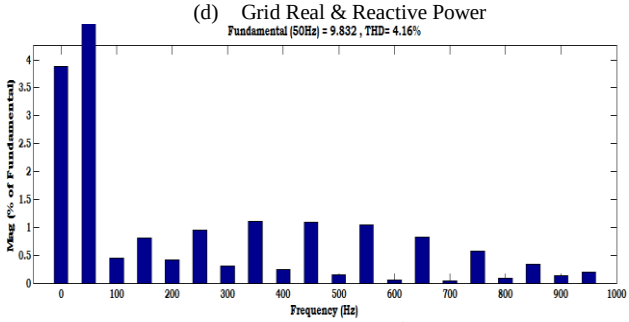
(b) Three Phase Grid Current



(c) Three Phase Grid Voltage & Current Represented Power Factor



(d) Grid Real & Reactive Power



(e) Harmonic Spectrum of Grid Current

Fig.9. Simulation Results of Proposed Three Phase Asymmetric 7-Level RSMLI Topology-2 under Grid Connected Scheme

The simulation results of proposed Asymmetric 7-level RSMLI topology-2 under grid connected scheme are illustrated in Fig.9 and represented as (a) Three phase grid voltage, (b) Three phase grid current, (c) Three phase grid voltage & current represented power factor, (d) Grid real &reactive power, (e) Harmonic spectrum of grid current. The grid voltage shows the pure sinusoidal voltage with a 120^{o} phase displacement and the output load current also acquiring the near sinusoidal RMS current waveform. The grid voltage and grid current is combined to represent power-factor, both the voltage and current are in-phase sequence as shows the unity power factor (for clear representation of power factor the grid current is increased by 5-times). The real & reactive power as maintained constant and achieves the grid standards and harmonic spectrum of grid current is 4.16%, it is under the IEEE standards limits.

IV. CONCLUSION

This paper proposes the novel three-phase symmetric 5-level & Asymmetric 7-level MLI topologies for designing renewable energy based DG applications under multi-carrier PWM techniques. The proposed MLI requires only six switches for generation of 5-level & 7-level voltages over the traditional cascade H-bridge type MLI topology.

The characterization of proposed RSMLI topologies are driven by introducing a novel advanced pulse width modulation technique which requires only two carriers instead of four carriers and requires low complex control gate drive circuitry. Proposed RSMLI topology offers fewer switches, gate drive circuit, reduced size; low cost, low switch stress and high efficiency can be attained over the traditional inverter topologies. The detailed simulation analysis of proposed symmetric 5-level & Asymmetric 7-level RSMLI topologies performance under R-load connected & grid connected scheme is carried out by using Computer Simulation tool. The feasibility of proposed 7-level modern inverter topology have favourable advantages and highly applicable to several applications. The further discussion carried on several types of faults are studied on proposed reduced switch topology by using wavelet-transforms.

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