Asic Implementation Of High Speed Discrete Integrator Using Vedic Mathematics

R. Anitha., V. Bagyaveereswaran

Abstract: ***Vedic Mathematics is an ancient Indian mathematics which has unique technique for arithmetic computation. An ASIC based discrete integrator is designed in this paper. This is a novel architecture employs less numbers of multipliers when compared with the conventional one. The architecture could be used in 16-bit ALU. This research used cadence ncsim, rc compiler tool and 90nm technology for synthesis. This paper reveals the study of Vedic multiplier for 16, 32 & 64 bits which is totally unconventional method than shift add. A single architecture also can be used for squaring, cubing as well as Reimann Integral Theorem up to order 4.***

Keywords: ***Discrete Integrator, Vedic mathematics, ALU, High Speed, Accuracy, Reusabilty***

I. INTRODUCTION

The Ancient Indians (Rishis) are popular all over the world for their Vedic knowledge. Their research in the various fields like astronomy, astrology, Ayurvedas (the study of medicines), mathematics and many more have astonished many researchers. All the research has been composed in Sanskrit language which is an ancient language of India and the composed scripture is known as the Vedas. There are four main Vedas known as the Rigveda, the Yajurveda, the Samveda and the Atharvaveda. Vedic mathematics is a part of Atharvaveda which elaborates high speed or more convenient approach for mathematical calculations. There 16 main formulas [1] in Vedic mathematic which could be useful in different branches of mathematics such as arithmetic, geometry, trigonometry, algebra, calculus, differential, integral. India is the country of diversity, every state has their own tone and word But Sanskrit language is the base of all Indian regional languages. After middle the centuries, Indians renounced communicating in Sanskrit hence the legacy discontinued due to language barrier. In the late 20th century, a Vedic mathematician HH Jagadguru Sankaracarya Sri Bharti Krsna Tirthaji Maharaja (1884-1960) has revived this legacy by discovering Vedic mathematics. He has explained all the formulas in his book [1]. All the formulas have been described in the decimal system, hence the same formula can't be applied to binary or any other radix in frequent cases. There are some ways by which we can make these formulas useful for binary also. But it is not guaranteed that we can transform every rule from decimal to binary.An ALU unit consists of multiply function, division, function, addition, subtraction and logical function. This illustrates the design of an Integrator, which will add more functionality to the ALU. This single architecture is enough for calculating square, cube and series functions. The architecture could be employed in Reimann Integral Theorem or trapezoidal rule.

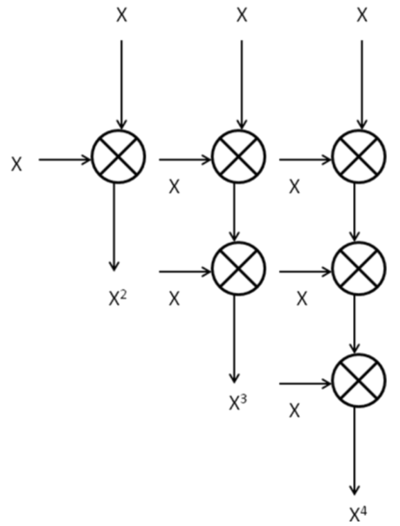

Fig. 1. An unbalanced multiplier tree for x^2, x^3, x^4

An Integrator consists of multiplier many multipliers. These multipliers are required to get squares, cubes and so on. There are some constraints through which a design must pass. Hence, the multiplier has to be efficient, delay should be matched, less power consumption and the use of minimum hardware. The Fig. 1 shows an unbalanced multiplier for which we could not match delay.

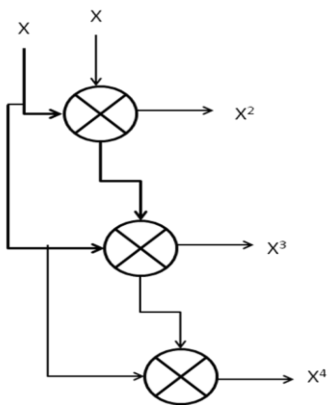

Fig. 2. An efficient array of multipliers

On other hand Fig. 2 shows same the functionality with minimum multipliers. Fig. 2 is a more efficient design when compared to Fig. 1. It saves the cost of the area and the number of multipliers. From the Fig. 2, we can deduce that since Fig. 1 takes a higher power than figure 2, as the number of multipliers. There is a significant reduction in power and area.

II. URDHVA TIRYABHYAM

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The Urdhva Tiryabhyam is the 3rd formula from the main sixteen Vedic formulas. The word itself reveals the meaning which is "vertically and crosswise". The following Fig. 3 [2] shows the operation of 2 bit multiplier.'

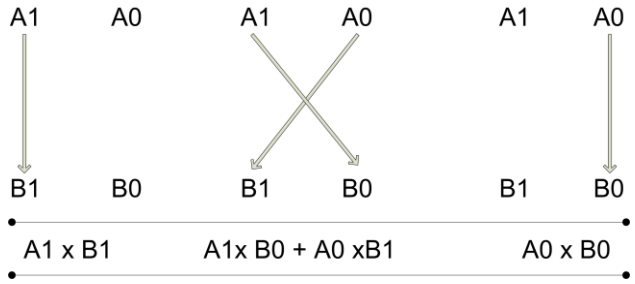


Fig.3 Example: Two bit multiplication method using Vedic mathematics

Let say, we have two bit numbers A1 A0 and B1 B0.Both numbers are to be multiplied using vertically and crosswise theorem. A1 and B1 are MSB of both numbers. A0 and B0 are LSB of numbers.
Step 1: A0 and B0 are multiplied using AND gate.
Step 2: A1 and B0 are multiplied using AND gate.
Step 3: A0 and B1 are multiplied using AND gate.
Step 4: A1 and B1 are multiplied using AND gate.
Step 5: add the result of step 2 and step 3 using OR gate.
Step 6: concatenate the result, in order as shown in Fig. 4
Similarly, the same logic can be applied for 4 bit, 8 bit, 16 bit and so on.

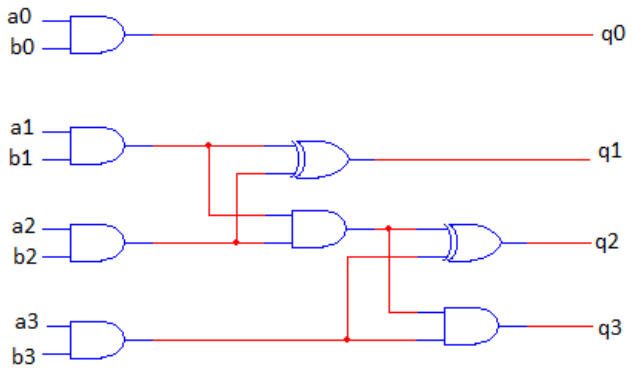
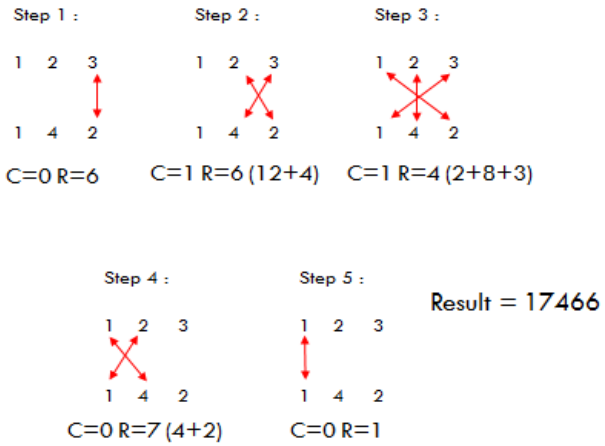


Fig 4 Two bit Vedic multiplier

This 2 bit Vedic multiplier is implemented using four AND gates and 2 half adders. It is found that is there is not much seen difference in delay when compared with conventional one, But when we increase the order of multiplication up to 64 bit Vedic the results were astonishing.

The following example will clearly explain the method of this sutra.
123 * 142 =17466.



By using this sutra, the number of partial products generated by the multiplier got reduced, because the calculation of partial products is performed in a single step. This causes less delay so that the speed increases even though the number of bits is more when compared to the conventional method.

III. PROPOSED ARCHITECTURE

The architecture consists of Controller, data enable, Vedic multiplier and ripple carry adder. There are three multipliers in this design 16 bit, 32 bit and 64 bit. There are five ripple carry adders in the design 16 bit, 33 bit, 65 bit, 130 bit and 200 bit.

The design is suitable for 16 bit input, which varies from 0 to 65536 in decimal. The architecture is very efficient to calculate squares, cubes in addition to integrate. It has four control signals which are responsible for selecting the order. The reset signal enables to control data flow. There are four control inputs for selecting the order and one mode input signal to switch its function. Hence totally 64 possible equations could solve using this architecture. Some of the possible combinations are shown in table 1 and table 2.A 200 bits of the register is used to save the result and to add with next result, also it responds to finish signal by clearing values from register so it can start for new task. The design handles up to order 4.The control signal control[1] is responsible for x, control[2] is responsible for x^2, control[3] is responsible for x^3 and control[4] is responsible for x^4.

A. Controller:

The counter has a clock input, mode and 16-bit start value, end value and x digit input. The clock is used for timing reference. At the positive edge output values are changed. The mode used to choose an operation as shown in table. 1 and table 2. If Mode signal sent as logic 1 then it will act as a discrete Integrator. Once it enters into mode 1 it will start counting until the value reaches equal to the end value. Once the start value becomes equal to the end value, the module generates a finish signal to the adder module. The finish signal will generate final result and also it will clear all registers.

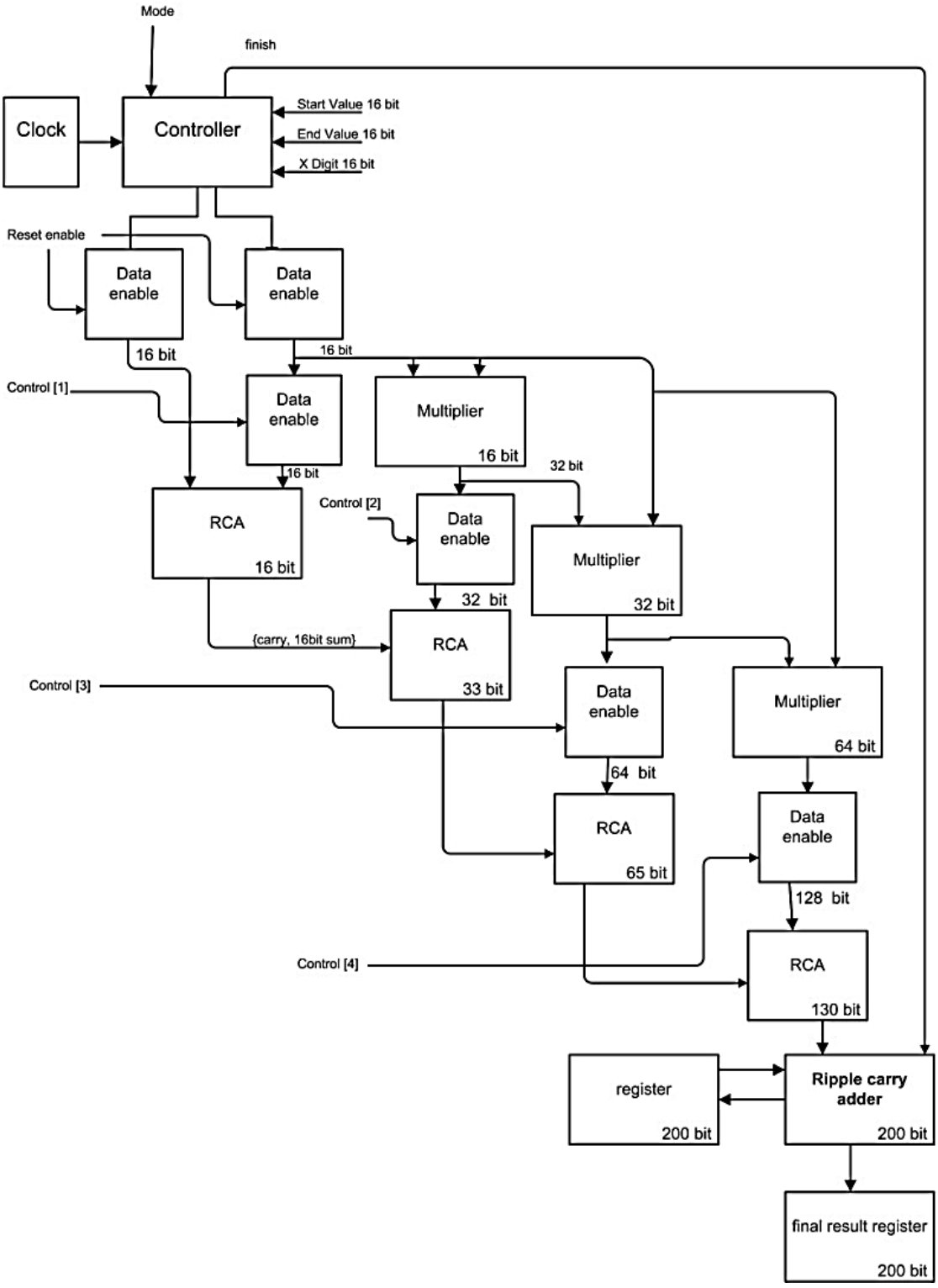


Fig 5. The proposed architecture of discrete Integrator

The figure 5 shows an universal architecture for Vedic multiplier. For an example, if we want architecture for 32 bit multiplier then select value k=5. We used four 16 bit multiplier to design 32 bit multiplier. The A_{LSB} and A_{MSB} are the parts multiplicand which divided into equal number bits on both sides. Likewise the B_{LSB} and B_{MSB} are the parts multiplicand which divided into equal number bits on both sides.

The OR gate has no computational importance, but it is used to match delays, unless both RCA completes their operation

The final RCA won't start execution. It helps to match delay problem and gives accurate result.

B. Ripple carry adder:

Ripple carry adder has better performance than carry skip adder, carry look ahead adder, carry save adder in all aspects [5].

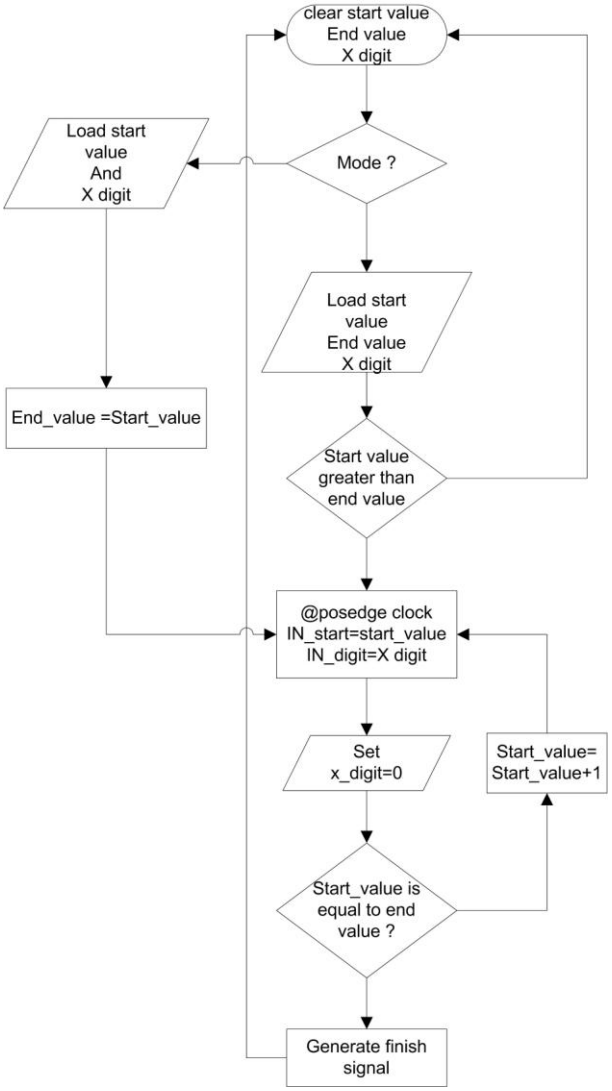


Fig 6 Flow chart for controller

RCA stands for Ripple carry adder which is responsible for the addition of binary bits using an array of full adder. The RCA propagates a carry after an addition of 1 bit binary number.

Each multiplier owns 3 ripple carry adder. If the multiplier is 32 bits, then 32 bits RCA should be used, likewise if the multiplier is 64 bit, then 64 bit RCA should be used.

C. Control signals and mode:

Let the start value be m, end value be n and x digit value be c. When mode is equal to 1.Following table 1shows some examples of control signal when mode is equal to 1.

Mode=1

Table I. Few examples, when Mode=1

Control [4:1]	Function
4'b1111	$\sum_{m}^{n} x+x^2+x^3+x^4+c$
4'b1100	$\sum_{m}^{n} x^4+x^3+c$
4'b1001	$\sum_{m}^{n} x+x^4+c$
4'b1000	$\sum_{m}^{n} x^4+c$

Mode=0

When mode is equal to logic zero. Following table 2.shows some examples of control signal when mode is equal to 0

Table II. Few examples, when Mode=0

Control [4:1]	Function
4'b1111	$m^4+m^3+m^2+m+$
4'b1100	m^4+m^3+c
4'b1001	m^4+m+c
4'b0100	m^3+c

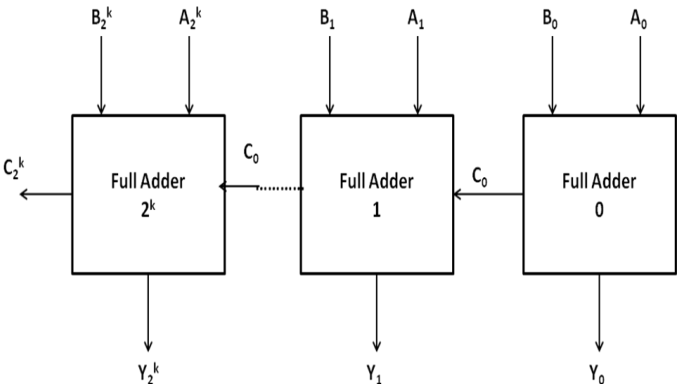


Fig 8 ripple carry adder

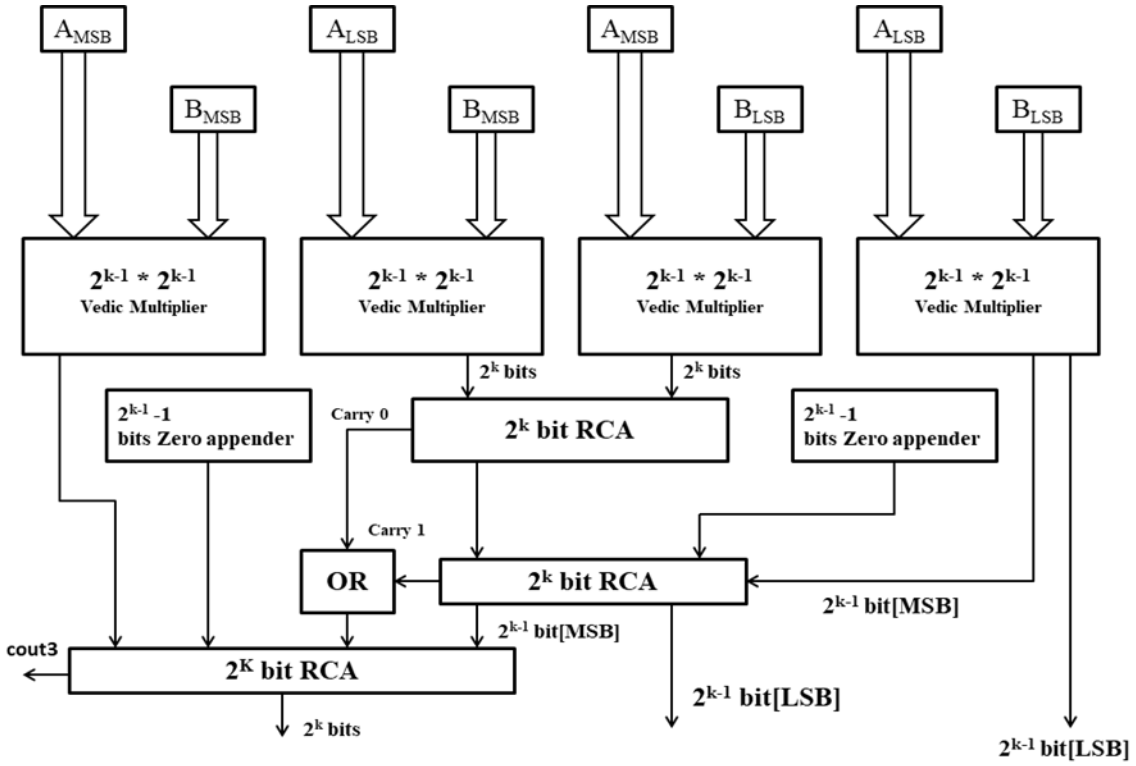


Fig 7 Architecture of 2^k bit Vedic multiplier

IV. RESULT & DISCUSSIONS

The synthesis result is grouped in table 3 for Vedic multipliers of different size.It shows the difference between different multiplier schemes for 4x4, 8x8, 16x16, 32x32 and 64x64 bit multiplication.We have studied multipliers and analyzed their results as follows.

The 4 bit multiplier is implemented with the Vedic Matematics Logic. And the simulation graph is shown in the Fig. 9. a[3:0] and b[3:0] are the input bits and the result is shown in the c[7:0].

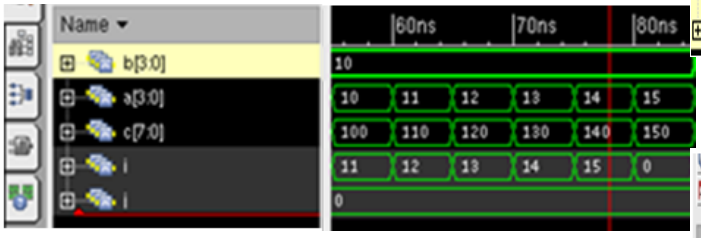


Fig 9 Simulation results for 4 bit multiplier

Then by using the 4 bit multiplier block designed the 8 bit multiplication circuit and simulated. The simulated the results are shown in the Fig. 10. Taken with the 20 ns dealy for each inputs.

Fig 10. Simulation results for 8 bit multiplier

Similar way 16, 32, and 64 bits multiplier is designed and the results are in Fig. 11, 12 and 13 respectively.

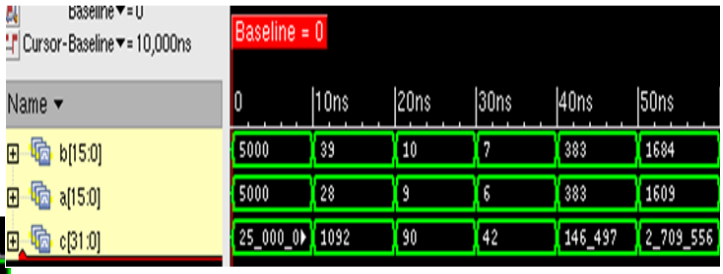


Fig 11. Simulation results for 16 bit multiplier

Fig 12. Simulation results for 32 bit multiplier

Fig 13. Simulation results for 64 bit multiplier

Using the NCSIM we simulated the design and the synthesis has been done using 90nm and the parameters like area, dealy , power and number of gates needed for the circuit implementation are calculated for the various number of bits. And the comparaitive table for 4 bit, 8 bit, 16 bit, 32 bit and 64 bit are shown in the table III.

Table III. Synthesis results for multipliers using 90nm.

Multiplier bits	Delay	Area (um^2)	Power(nW)	Gates
4x4	1100.90ps	575	1263625	89
8x8	1868.40ps	2192	3738570	312
16x16	3194.60ps	7847	13393267	1008
32x32	5508.5ps	30947.62	50608893	3679
64x64	9814.60ps	116768	195269238	14773

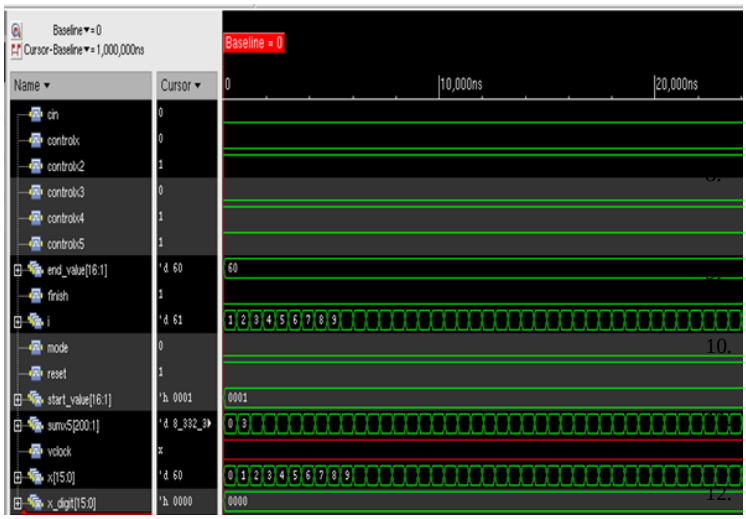


Fig 14. Simulation results for discrete integrator

$$\sum_{0}^{60} x^2 + x^3 = 3422710$$

Table IV. Synthesis result of the proposed architecture (discrete integrator)

Area	62777.94um^2
Delay	9072ps
Power	71198383nw

V. CONCLUSION

The main focus of this paper is to introduce a novel architecture for discrete integrator using Vedic multipliers.This novel architecture employs only 3 numbers of multipliers As compared to the conventional unbalanced tree of multiplier shown in figure 1 which uses 6 numbers of multipliers.Due to the parallel structure of Vedic multiplier, we are able to reduce its delay. We took the advantage of simple design, its accuracy and reusability of Vedic multiplier. There is an increase in the delay by 71% when input bits are double with respect to previous one. The design is highly efficient and optimized for 90nm technology. We used a cadence simulator for the simulation of an integrator.

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