Design of High Speed Comparator using DTMOS Technique with low Power Consumption

Ujjayini Debnath, Shobha Sharma, Amita Dev

Abstract: ***The comparator circuits are used to compare signals whether it is analog or digital signal. We use of Comparators in Analog-digital-convertors (ADC) as one of its basic elements. Nowadays semiconductor industries are demanding for powers as less as possible and with faster operation. The paper represents a double tail comparator by using DTMOS operation. This type comparator design of a double tailed structure consists basically of two stages. First one is preamplifier stage and another one is latching stage. The conventional comparator circuit designing is improved with a dynamic comparator (double tailed) to decrease the power consumption and the voltage in the mean time increasing the speed, keeping frequency at 500 MHz Scaling of Technology of the MOS transistor in semiconductor industry provides low power consumption by applying ultra low input voltage which minimizes the timing delay. This design in this paper has been simulated in using CADENCE virtuoso in 90 nm CMOS technology. Main purpose of this topic is to alleviate the switching delay of the comparator as well as ADCs for small supply voltage.***

Keyword– clock gating, Delay, Dynamic Comparator, Low voltage, Preamplifier latch, DTMOS, Analog to Digital Convertor (ADC),

I. INTRODUCTION

Comparators, one of the main favorable elements to compare in integrated circuit design for digital, analog and mixed signals. The main task of the comparator is to compare two signals; either it is a digital signal or an analog signal. The comparator basically comprises of two steps, primary one can be said as reset stage and the second one can be said as a comparing stage. The one of most prominent criteria for deducing power consumption is that is to scale the input voltage supply. This is because of that, due to the complementary-MOS digital circuits, delivery of average value of power is always directly proportional to the whole square of the input voltage supplied

$$P = C_L Vdd^2 Fd$$

Where, the consumption of power is P for a single gate, C_L is capacitance (switching) of a single gate, voltage supply is Vdd, the cooperating freq. (avg.) of a single gate is Fd.

These main phases in a double tailed comparator are as follows. These are pre-amplifier stages, reaction phase, and decision-making phase.

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The very first phase, the pre-amplifying the input signals is given to the input of the comparator. This is being amplified. Then the next phase is a reaction phase. This stage mainly identifies the input signal, that it is low or high. The second next or the last step is the decision- making phase after then the buffer phase at the output. The main concept of buffer phase is to increase the output signals stability. Any comparator circuit design consideration are the input common-mode-range (ICMR), dissipation of power, diffusion delay etc. A comparator was implemented with 4 steps and integrated motors. In this 1.2 voltage CMOS technology was using 10GHz 4-stage comparator, then that was being used to get each 4 bit Stream of data. With input voltage is 1 V, slightly error rate was there, less than around 10 to 12. All comparators design, with the help of supply-enhancing techniques, these are mainly dependent on static or dynamic or switching voltage sources such as diode, capacitors etc. These comparator designs are further improved by different techniques such as with an additional SoC (silicon on-chip) circuit, the timing delay for a comparator was measured and the comparator output time difference was found to be lower. Additional circuits have been added to the comparator so that it can give an improved version of delay at very minimum supply. The improved version of comparator can works at very low the supply voltage such 0.5V, which is the double tailed comparator's proposed version, this consumes very less power. One thing should always be noted that the mismatch of circuit components designed in the extra circuit should be kept in mind, though the approach is effective.

II. COMPARATOR

As conventional comparator circuit, the double-tailed comparator also compares any two input signal such as currents and voltages which are able to produces digital output. The double-tail comparator also made up of PMOS and NMOS transistors. This CMOS comparator functions as comparing element for a signal with the other fixed signal, which is called as reference signal. This comparator comprises of a very high gain stage differential type amplifier. In analog to digital converter circuits (ADCs) the basic building block is a comparator, which performs the conversion of data from analog to digital or digital to analog vice versa.

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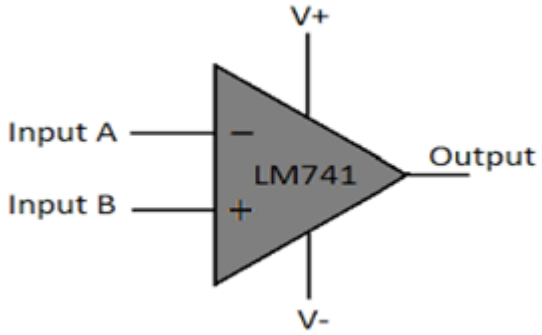

Fig (a): Symbol Diagram of Comparator

Generally the double-tailed comparator circuits are very faster, usually faster than the conventional ones. Mostly the higher speed ADCs, such as we can say flash type ADCs, are required high in speed, these Comparators consumes also less power. To speed up the power trade, the comparator circuit is not immune. The flash type ADC has high speed as very low delay that uses large aspect ratio MOS transistors and therefore consumes high power. Therefore, a comparator should be selected based on special application. Therefore in ultra-deep submicron/deep submicron technology CMOS techniques, the designing of such high speed comparator circuits are the most problematic when input voltage supply kept small.

Due to this, a positive feedback in the regenerative latch is generated; thus a clock is also generated, the clocked regenerative comparators are making decisions increasingly. An analysis of the designing structure and the work of both double tailed comparator (traditional and proposed) and presented in this paper.

III. CONVENTIONAL COMPARATOR: SINGLE TAILED

This Section explains about the single tail comparator and its operation. This single tailed circuit has a clock Regeneration stage, which is used in various high accuracy and high-speed analog to digital (ADC) circuits.

This circuit (fig.2) is called single tail because it has only one tail of NMOS transistor at the bottom. This whole diagram has two inverter connected back to back. These inverters are working as latch circuit showed in fig.2 [1].The clock Regeneration (gating) technique is especially used for reducing the dissipation of power. A common comparator is also represented as Single tail structure. The circuit (figure 2) of that traditional single tail comparators can be being employed in many digital converters. This type comparator design is having two types of operation, one is reset; the other is evaluation. Single tail comparator works at input voltage supply at 0.8 V. This is implemented on 90 nm CMOS. At first clk has kept at 0 V, so Clock = 0 is known as the reset step and when clk is zero the tail MOS is non-conducting i.e. the NMOS is OFF. So the outputs will be turned up towards Vdd. Again for second step (evaluation) if we take Clk as high or Vdd, i.e. the clk =1 V, then the tai; NMOS is in conduction, i.e. it is ON. This depends upon the input signals. If positive input(INP) is larger than negative input(INN), the output p(OUTP) will discharge prior to output N(OUTN). After OUTP is fully discharged, then M5 starts getting ON, then M5 pulls OUTN towards Vdd.

Reset: if clk = 0, the tail Off. M7 / M8 are ON. Outputs on Vdd

Evaluation: clk = 1, M7 / M8 are OFF. Tail MOSFET On. Now OUTN and OUTP, who were charged before Vdd, they seem to be discharged. Discharge rating varies depending upon signal input voltage at INN and INP. The OUTP gets discharged faster than OUTN, so the output voltage, which was precharged in VDD, starts discharging; depends on the respective voltage at INN and INP. At node INP, Voltage is larger. But Voltage at INN is smaller than that. The output OUTP discharges faster than OUTN, (by transistor M2 drain current), then Vdd goes below Vtp (threshold w.r.t INP) before the OUTN (which has been drawn by drain current of M1). INP node voltage, is less than INN node Voltage , then output OUTN is discharged very fast than compared to OUTN, vice versa. Delay means the capacitive charge or discharge at the load capacitance. If, the input voltage INN is lower of INP (i.e., VINP is larger), due to drain current of the M2the OUTP discharges. Prior to the OUTN. The drained current at M2 is comparatively less than the M1. The single Tail structure has high input impedance. This structure has prominent advantages, that no static electricity consumption is drawn. It has other advantages such as: rail to rail swing, noise immunity etc. Parasitic capacitance of the input transistor does not have any direct affect on the switching speed of the circuit output signals. There large input transistors can be designed to alleviate the offset. On the other hand, there are some disadvantages. One of them is that there in this structures several stacked transistors are being used. Due to this the latch time is delayed, which consumes too much supply voltage, hence more power consumption. But power consumption in this structure is less than other conventional comparators

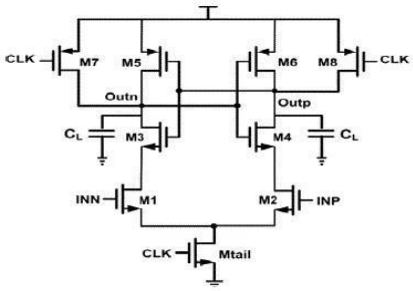

Fig 2: Design of Single Tail Conventional Comparator [1].

The other drawback of this kind comparator structure is such, that "tail" transistor defines the voltage inter amplifier alone. Because of that the routing to the ground is becoming congested. So some timing delay is there in the route from any node to the ground. Hence current drifting is a bit complex.

IV. Design of DOUBLE TAILED COMPARATOR

The double tail comparator structure also consists of comparative latch circuit. The difference between the conventional single stage comparator structure and this structure is that, this structure has two MOSFET at the top (VDD) and at the bottom (GND). That is why the name double tailed had given. This structure improves the drawback form the conventional single stage had. This structure gives two different current draining paths through two tails. Thus it abates the delay time.

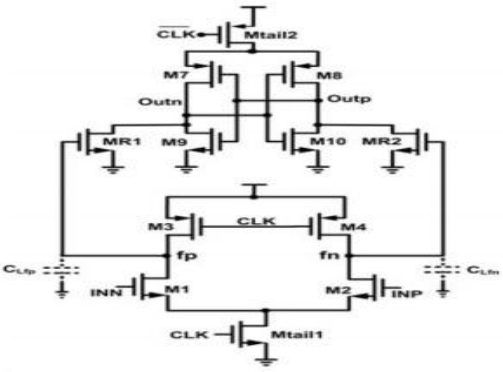

Fig 3: Structure for Comparator (common Double Tail)

The circuit functioning is explained as below; alike in single tail structure the initial stage was clk at 0 V, i.e. clk=0 V. Thus both tails (Mtail1&Mtail2) OFF. So M3&M4 ON. Fp & Fn are charged at Vdd. This gets MR1/MR2 turned ON. Thus outputs OUTP and OUTN both are plled down towards GND. Due to this M7/M8 both are ON.

Again when clk at Vdd, i.e. clk=1 V, then both tails are ON. M3/M4 both are OFF. The both outputs get charged to Vdd. Now for comparison stage input signals are to be compared. For INP higher than INN, the node Fn will be discharging prior to Fp. At this time OUTN is charging towards VDD. OUTN gets charged more higher rate than OUTP. Now if Fn gets discharged, then MR2 is ON, due to this OUTP is grounded.

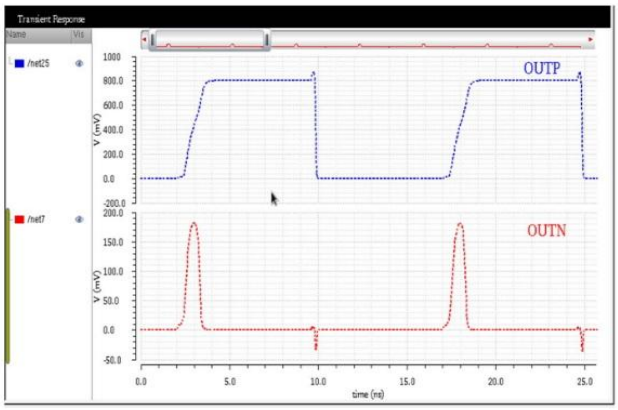

Fig 4: Transient Analysis of Double Tailed Comparator

Now for its modified version of double tailed, again we have to keep once clk at 0 for reset phase and at 1 for set phase. When clk=0,it will work as same as the previous structure(figure 2). But when clk is at 1, then Fn/Fp both gets discharged depending upon the input signal values.

Now when INP is larger than INN, Fn discharges prior to Fp. Now MC1 is ON, the node Fn went back to Vdd. Mean while MC2 is OFF. This is cause static power consumption. To abate this problem, in modified version of comparator one couple of transistors used, Msw1/Msw2. This structure has shown in figure 3. Msw1/Msw2 both are operating as switch. The clock gating technique can be used to hold all clock signals for a particular period of time. During this period there will be no Power consumption. This is also a technique to reduce the power consumption. Clk is at 1, NMOS conducts i.e. ON. PMOS transistor OFF.

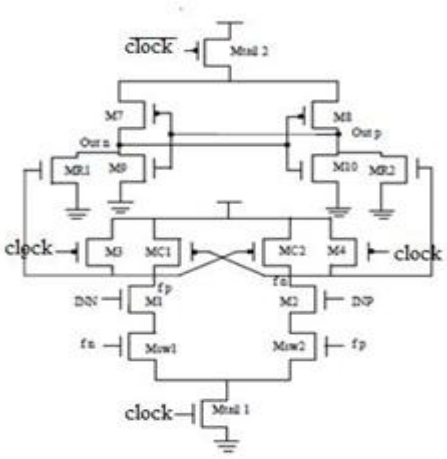

Fig: Double Tailed proposed Comparator

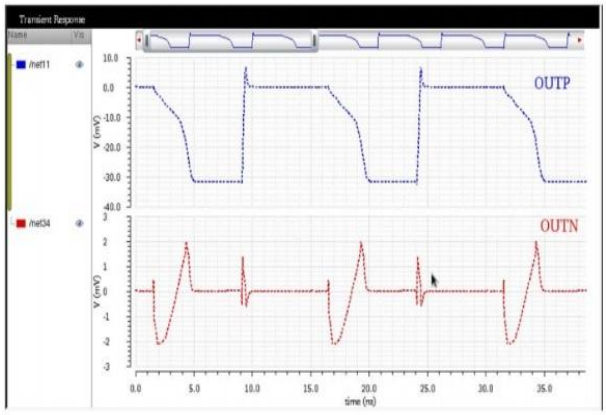

Fig: Transient Analysis for improved Double Tailed Comparator

There are three main constraints for analog, digital or mixed signal circuit designing. These are area, power, and delay. As we know there are trades off between design constraints. Here in this paper power and delay can be improved by compensating the chip area.

As a control transistor is started conducting, Vdd is pulled towards the ground through the tail MOSFETs .this situation causes the power consumption, which is static. Couple of NMOS switches is used such as Msw1 and Msw2, to overcome that drawback.

In the first stage both the Fn/Fp are already already charged to the Vdd (at the reset stage),

The control transistors (MC1/MC2) will work as to rise its voltage difference, so that as one of the nodes Fp/ Fp is being discharged rapidly.The transistor with the switch controls the entire operation of the latch.

All schematic designs are simulated using 90 nm CMOS technology, resulting in a decrease of delay with the supply of 0.8 v.

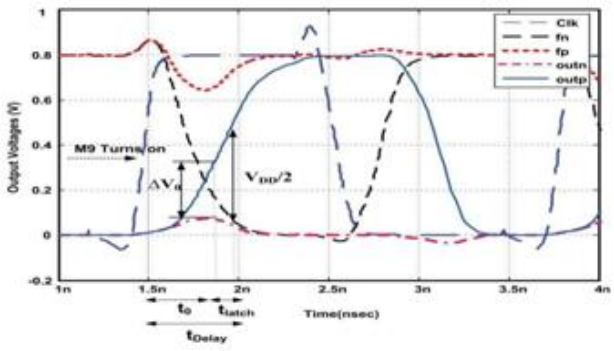

Fig.3. Transient simulations

In the analysis of simulation parameters, design layout of simulation will be taken to the CADANCE virtuoso 90nm CMOS technology results. The primary concept of this proposed double tailed comparator idea is to abate the power and as well as delay.

VII. DTMOS TECHNIQUE: DOUBLE TAILED COMPARATOR

The lower value of power supply is to be around 0.6 V . A Dynamic Threshold Voltage MOSFET (DTMOS) has been depicted in this paper. In 1994 the first DTMOS technique was introduced. In DTMOS technique the gate and bulk terminal are connected together. This technique enhances the current driving property of the circuit. DTMOS provides very less delay, hence high speed.

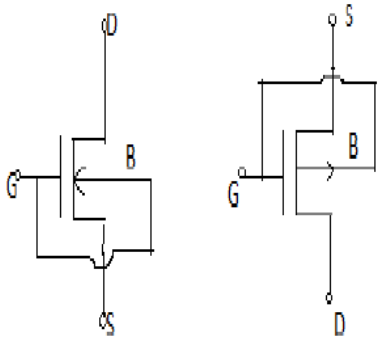

Fig (a): n-MOSFET **Fig (b): p- MOSFET**

Fig: Structure of DTMOS

These two figures show the DTMOS structures for NMOS and PMOS. When DTMOS are in conduction, its threshold voltage gets decreased. Thus the driving current increases and the propagation delay decreases. On the other hand, if a DTMOS transistor is OFF, that means if it is not conducting, then the threshold voltage increases. As well as the leakage current of the MOS is also minimized. Thus due to low leakage current power consumption is also reduced.

In this paper, double tail comparator designed with DTMOS, such for all amenities. The design is simulated using 90 nm CMOS technology. The low voltage improved version comparator circuit has less power and minimized delays. Some control transistors gives less delay. Due to this the output propagation delay is minimized. The power consumption has been lessened even in low supply voltage of 0.8 v. The application of new version comparator is in such faster speed applications such as ADCs where fast decision-making tools are required.

VI. EXPECTED OUTPUT

By comparing the comparative comparison of traditional comparator and double tail comparator to literature, it has been found that delay in the promotion, speed of the circuit is high. In this paper all four structure comparisons are shown. The power and delay analysis with other parameters for all simple comparator and proposed DTMOS comparator has been depicted. The result of circuit simulation in 90 nm CMOS technology showed. The delay and power have been simulated through cadence virtuoso. The power consumption by conventional comparators was app. 39 uW. The estimated delay was 9.12 nS. In this paper the purpose of using DTMOS is justified as the POWER and DELAY has been drastically minimized.

VIII. SIMULATION IN CADENCE

The simulation parameters, design layout of simulation will be done to the CADANCE® virtuoso 90nm CMOS technology results.

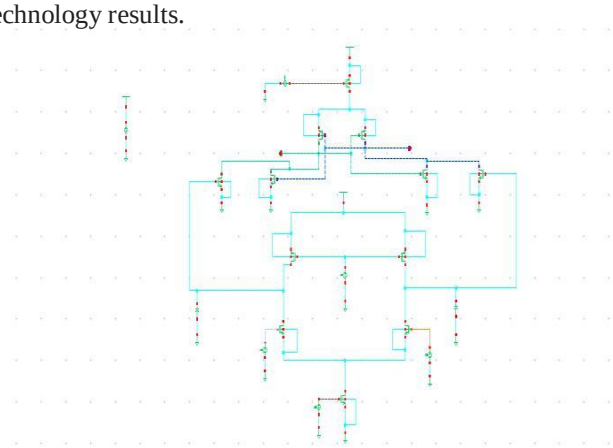

Fig: Double Tailed Comparator Circuit

Power supply (Vdd) palliation below the three times the threshold voltage (3t) will cause the degradation the circuit speed, as well as leakage current. Due to the scaling of semiconductor industries the power supply is also getting scaled or getting reduced very rapidly. But with decreasing of power supply the threshold voltage cannot be compensated with. If gate voltage is less than the threshold voltage there might be some leakage current occurs. Hence, the lower limit for threshold voltage, which is depending leakage current. Ideally this should not be less than 0.4 V. The standby power consumption causes dynamic circuits failure. Due to this reason in memory arrays there the leakage currents arrives.

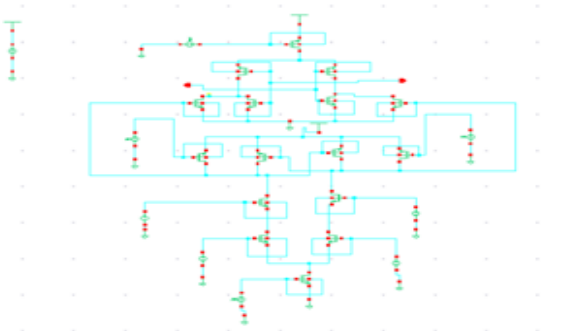

Fig: Proposed Idea using DTMOS

These simulation parameters, design layout of simulation will be taken to the CADANCE® virtuoso 90nm CMOS technology results.
The first stage is reset phase, fn/fp nodes are already charged to the Vdd (at reset phase) as shown in fig 2/3.
High-speed ADCs are several applications areas of comparators. They have a latch with positive feedback. Many implementations have been presented about this topic recently. But this paper shows has shown the modified version of comparator circuit using DTMOS, which shows very high performance. Comparators structures also has different parameters, such as noise immunity [11], offset [12] , [13], and [14], random decision errors [15], and kick-back noise [16] etc.

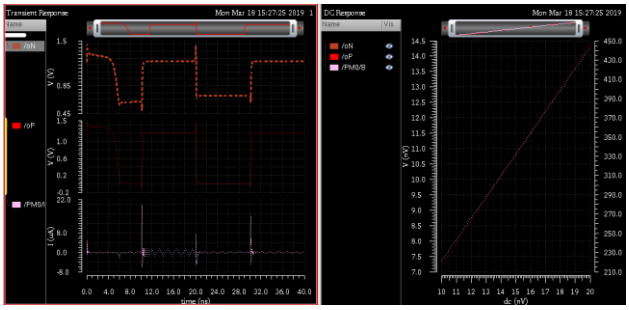

Fig: Transient/DC response

The threshold independent type comparator gives zero offset voltage. The double tailed comparator has many advantages compared to other comparator versions. Yet, however, application and its requirements are i based on the selection of any topology.

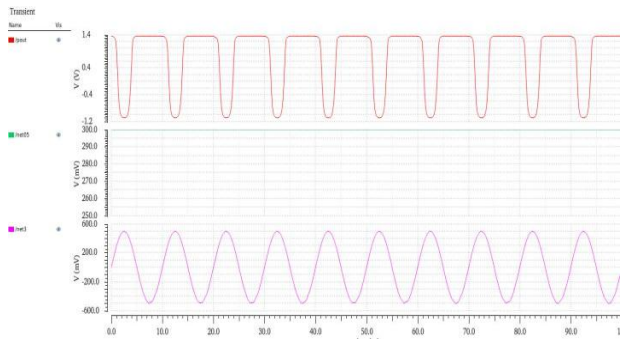

Fig 6: Output Wave form: Proposed Double Tailed Comparator

Parameter	Conventional Comparator	Double Tail Dynamic Comparato r	Using DTMOS
CMOS Technolog y	90nm	90nm	90nm
Power Supply	0.8 V	0.8 V	0.8 V
Average Power	12.65 uW	7.85 uW	2.921 uW
Delay	1.77 ns	367.2 ps	261.7 ps

Table : Table of Parameter

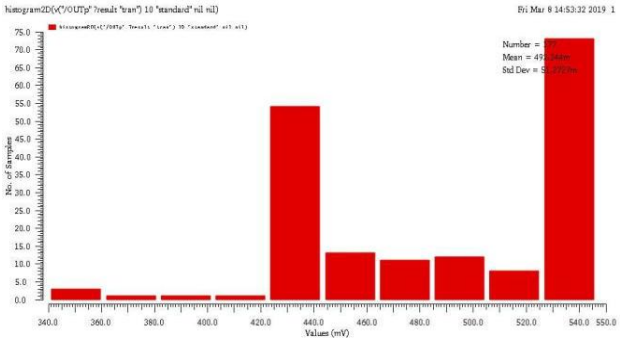

Fig: Histogram for Dynamic Biased Comparator

VIII. CONCLUSION

The above proposed double tailed comparators using DTMOS were designed and simulated using cadence GPDK 90nm technology which shows less power 2.921 uW, with VDD 1 volt. Amongst all preamplifier based comparators the low power consumption and also less delay. Table showed the different parameter value of the simulations. The table also showed the values of the parameter for ne DTMOS verson comparator. The appropriate design can be selected based on the need of technology can be chosen. Dynamic threshold MOS (DTMOS) has some attributes such higher carrier mobility in comparison to standard MOSFET. Moreover, whenever voltage of DTMOS at its gate is raised, the threshold voltage drops. That results much higher driving current as compared to common bulk or SOI MOSFET. This technique enhances the current driving property of the circuit. DTMOS provides very less delay, hence high speed. We can see by using a new technique does improve the power consumption and also minimized the delay time. So the speed of the comparator circuit has been drastically reduced.

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