Comparative Analysis on Designs of Comparators with Different Techniques and Technologies

Ujjayini Debnath, Shobha Sharma, Amita Dev, Preeti Singh

Abstract: ***Comparators are used in Analog to digital convertors (ADC) as their basic element. There are several types of comparators, some of them are preamplifier based comparator, latch based comparator, dual tailed etc. Nowadays in semiconductor industries there is demand for very less power consumption, as well as high operating speed. The purpose of the paper here, is to analyses several comparators circuits and analysis on their power consumptions and delays, and further the proposed version. The design of double tailed comparator consists of two stages. First one is preamplifier stage and another one is latching stage. Basically the proposed versions of comparators are modified for high speed operations and of course for low power consumption with low power supply. For higher speed, NAND structures (latch) have not been used instead of NOR gate. Because NOR are generally slow. This paper depicts some of parameter comparison. These comparator circuits are being improved day by day to specify some attributes depending upon the criteria and of course by using new techniques such as boot strapping, offset elimination, noise reduction, clock gating etc.***

Index Terms**: Analog to Digital Comparator, delay, dynamic comparator, *preamplifier latch, low power.***

I. INTRODUCTION

Comparators are one of the favorable elements in designing of integrated circuits like for digital, analog, and mixed signal as well. The comparator does compare two signals, either it be digital signal or analog signal. The comparator basically based on two phases of operations, reset phase is primary phase, and set stage is the second one (for clocked input type). The one of most prominent criteria for deducing power consumption is that to scale the input voltage supply. This is because of the reason that, due to the complementary-MOS digital circuits, delivery of average power is always proportional to the whole square of the input voltage supplied.

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Ujjayini Debnath, Electronics and Communication, Indira Gandhi Delhi Technical University for women, Delhi, India.

Dr Shobha Sharma, **Corresponding Author**, Faculty, Electronics and Communication, Indira Gandhi Delhi Technical University for women, Delhi

Prof Amita Dev, Pro VC, Indira Gandhi Delhi Technical University for women, Delhi, INDIA

Preeti Singh, Electronics and Communication, Indira Gandhi Delhi Technical University for women, Delhi, India

$$P = C_L V_{dd}^2 F_d$$

Where, the consumption of power is P for a single gate, C_L is capacitance (switching) of a single gate, is the supply-voltage; F_d is the cooperating frequency (avg.) of a single gate.

II. RELATED WORK

As conventional comparator circuit, the double-tailed comparator also compares any two input signal such as currents /voltages, produces digital output. The double-tail comparator also made up of PMOS and NMOS transistors. This CMOS comparator functions as comparing element for a signal with the other fixed signal, which is called as reference signal. This comparator comprises with a differential type amplifier, which has very strong gain stage. The basic component block in analog-digital converters (ADCs) is comparator, which performs the data conversion from analog to digital or digital to analog vice versa

Ultra Low Power convertors are using to enhance the power efficiency and the speed which is used as regenerative stage comparators. This Paper depicts expression and analysis of delay and power of the comparators. This approach is developed for Low-power Low-voltage and quick speed operation. These simulations are based on 180nm, 90 nm, 250 nm, 130nm CMOS Technology etc.

To speed up the power trade, the comparator circuit is not immune. The flash type ADC has high speed as very low delay that uses large aspect ratio MOS transistors and therefore consumes high power.

Therefore, a comparator should be selected based on special application. Hence in ultra-deep submicron/deep submicron technology CMOS techniques, the designing of such high speed comparator circuits are the most problematic when input voltage supply kept small.

Table 1: Parameters and their value for 180 nm CMOS technology [1]

Sl. No.	Parameters	Values
1	Technology	180nm CMOS
2	Power Supply	1.2 V
3	Power Dissipation	329uW

4	Delay	550 Ps
5	Frequency	500 MHz

Table 1 shows some parameter values for a conventional type comparator (figure 1), Generally the double-tailed comparator circuits are very faster, usually faster than the conventional ones. Mostly the higher speed ADCs, such as we can say flash type ADCs, are required high in speed, these Comparators consumes also less power

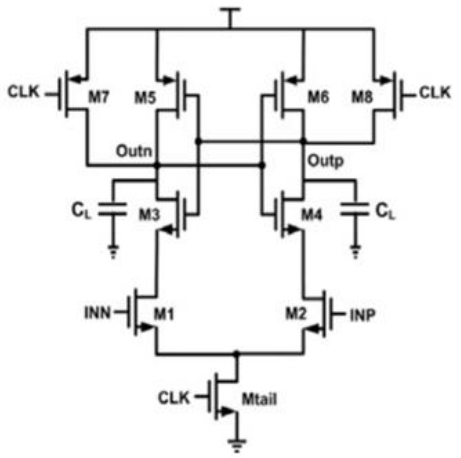

Fig 1: Schematic for a Dynamic Conventional Comparator

The above figure shows Schematic of circuit for a Dynamic Conventional Comparator. In this figure there are two basic parts, which can be divided into phases. One is reset phase, during this CLK is Zero "0", M_{tail} OFF. Another phase is comparison stage. In this CLK is High or CLK=V_{dd}.
Here in this paper [1], compares delays, power consumption between two comparator structures, one is Dynamic and another is Double-tailed. Another paper has shown a Latch Comparator. The proposed technology is executed in 65nm CMOS Technology. In this paper they have shown that he supply voltage taken to simulate the basic circuit is 1.2 V [2],[4].

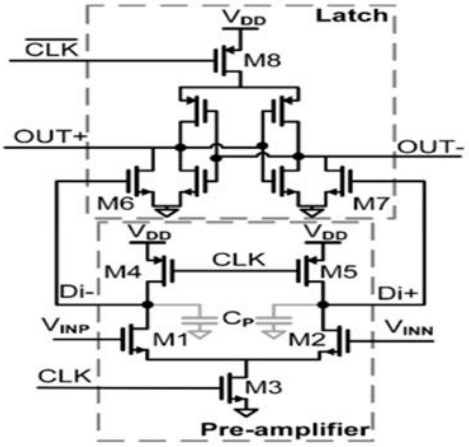

Fig 2: Latch Type Comparator (Double-Tail)

This figure 2 shows Double-tail Latch Type Comparator, which includes capacitors that ensures partial charge and discharge which reduces energy consumption. This approach has no isolation between differential input and regeneration Latch stage, regeneration Latch undergoes some kickbacks. As shown in this picture there are two Tail Capacitors are C_p, the corresponding energy w.r.t. V_{dd} is fixed (2 x C_pV_{dd}). When CLK =V_{dd} . $Ctail$ initialailly charges.
This approach has low overhead, Low-power consumption is only due to partial discharge of capacitors. Comparators are used in ADCs (Analog-to-Digital Comparators). These comparators are made-up of CMOS (PMOS and CMOS) and Bi-CMOS [3]. This paper basically shows offset cancellations. This comparator structure has also two stages Preamplifier and Latch. Here offset is less than 300 microvolt. Power dissipation is 1.8 mw. This paper showed some design techniques which provides some advantages such as High-resolution, improved speed, and very less power consumption with obviously minimum complexity.

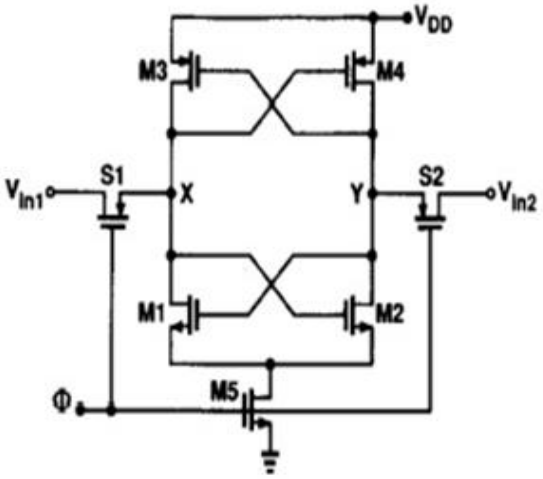

Fig 3: CMOS switching Latch circuit used in comparator

This paper shows offset cancellation techniques for both stages, Pre-amplifier and Latch with Low-Power Dissipation. This paper worked on CMOS current comparator. This type of comparators represents real-time data processing. This paper shows comparators based on current mirror [5].

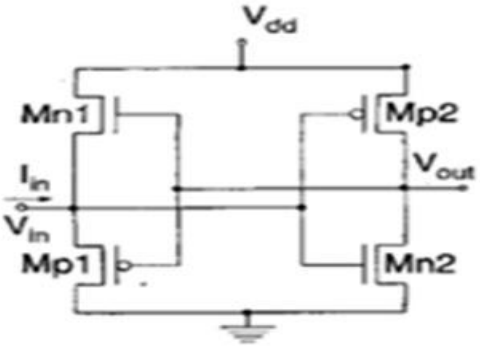

Fig 4: Tarff's circuit.

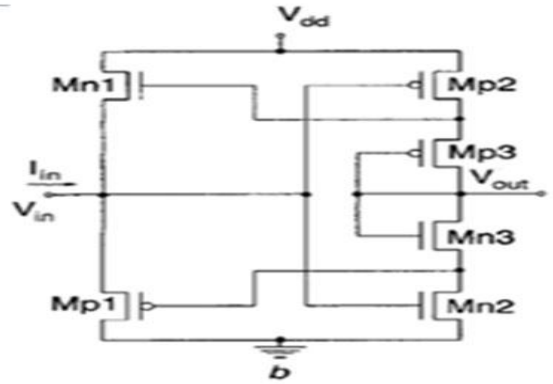

Fig 5: Another of Proposed Circuit

Table 2: parameters for above structure [5]

Sl. No.	Transistors	Width um	Length um
1	Mn1	5	2.5
2	Mp1	24	2.5
3	Mn2	5	4.0
4	Mp2	24	4.0
5	Mn3	20	2.0
6	Mp3	60	2.0

Table 2 is for another paper [6]. This paper worked on 0.13µm or 130nm technology. Voltage supply was 1.2v. Delay .62ns & power dissipation was 1.5nw. Overall purpose of this paper was to reduce power consumption, by minimizing the size of transistors being used [6].

This paper is based on 65nm Technology; purpose of this paper is to increase speed. But, Static power is high though sine is minimized. The paper showed on chip designing of comparator, which produces high frequency signals with 31% higher speed. [7]

Technology node is being used 22nm, this circuits has two advantages- Noise Immunity, Low Leakage Current. Domino logic based Comparator minimizes the parasitic, where two currents are being compared (One Marmoreal Current & another is Leakage) [8]. This paper uses 90nm technology. Here comparator circuit uses cross coupled transistors which improve speed of the circuit [9].

This paper reveals 0.18µm technology using dynamic latch structure. Thus works on high frequency 400MW. It uses a preamplifier stage. This enhances the speed of the comparator circuit [10].This is done on 90nm technology (GPDK). Comparator has various uses, such ADC, level shifter, window detector, relaxation oscillator, null detector. Here in this paper design comprises of some phases divided into three parts such as - (a) Pre-amplifier Stage (b) Decision Making Stage (c) Buffer Stage at the Output, Power supply required is 1 volt. Circuit obtained minimum offset voltage, better noise immunity [12].

Technology used is 0.18µm. Power supply required for successive approximation ADC using SR latch is 1.5V. Clock frequency is 0.1 MHz, Power consumption 191pW. Proper transistor size helps to achieve higher resolution. Output of the comparator should be stable during clock cycle [11].

III. SURVEY ON COMPARATOR

Paper Name	Technology	Power Dissipation	Delay
Analysis/Design of Low-Voltage Low-Power Double-Tail Comparator.	180 nm	1.4 mw	358 ps
Design/analysis of high speed double tailed comparator with isomorphic latch	180/65 CMOS technology	1.3 mw	500 ps
Design a Dynamic latch comparator with reduced kick back	180 nm	1.0049 mw	-
Design of high speed dynamic double tailed comparator	250 nm	0.9307 mw	12.72 ns
Comparator Power Minimization Analysis for SAR ADC Using Multiple Comparators	Theoretical	50–60% less	
A 5 Bit ADC with two comparator	55		50ps
Substrate noise measurement by using noise selective voltage comparator mixed signal IC	50		0.1-1 ns
Concept of superconducting comparator for pipeline ADC			
A 1.2 V dynamic bias latch size comparator in 65 nm CMOS with 0.4 mV input noise	65 nm CMOS		
Understanding the potential and limitation of tunnel FET for low voltage analog/ mixed signal circuits.	10 nm FINFET	10% Improved	
Low power 600 Mhz comparator for 0.5 V supply voltage in 0.12 um cMOS	120 nm CMOS	2.65 mw	11 ns
A 7.65 mW 5 bit 90 nM 1GS/S folded interpolated ADC with calibration	90 nm CMOS	7.65 mw	
Ultra Low voltage high speed flash ADC design strategy based on FoM delay product	90 nm CMOS	4.1 mw	365ps

One comparator counter based controller for synchronous DC/DC converter	MATLAB		30 ms
A current mode Comparator for Digital Calibration of Amorphous Silicon AMOLED Display(AMOLD- AC Matrix organic light emitting diode Display	800nm		
A Mux Based igh performacce single cycle CMOS comparator	350nm		50ps
Design Approach using tunnel diodes for lowering Power in differential comparator		3.5mw	F=100GHZ
Kickback Noise Reduction Techniques for CMOS latched Comparators	180nm (HSPICE)	268mw	
Offset reduction techniques for use with high speed CMOS comparator	1um		
Design of a low power high speed comparator in 0.13um CMOS	130nM	1. 5 mw	0.62 ns

IV. CONCLUSION

Most of these papers have shown the conventional comparators as well as the proposed version and modified versions and explained about the consumption of power and the delay; noise etc. the comparator circuits are implemented in 32nm, 90nm, 180nm CMOS technology. The software used are CADENCE, LTSPICE, and SYNOPSIS, MENTOR GRAPHICS etc. After analyzing all the papers we can come to the conclusion that in today's era of chip scaling (area, power and delay) in Integrated circuit (IC) industry it's highly important to alleviate the Power consumption and to minimize the propagation Delay as well. Thus the several proposed version of these comparators are introduced.

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AUTHORS PROFILE

Ujjayini Debnath is perusing her M. Tech in VLSI Technology (Electronics and Communication Engineering) from Indira Gandhi Delhi Technical University for Women (IGDTUW). Her areas of research include Very Large Scale Integration (VLSI) design.

Dr Shobha Sharma, Faculty, Indira Gandhi Delhi Technical University for Women (IGDTUW). Delhi, India**. Corresponding Author**

Prof Amita Dev Pro-VC Indira Gandhi Delhi Technical University for Women (IGDTUW). Delhi, India.