10-bit 2-stage Time to Digital Converter for Raman Spectroscopy

Mahantesh P Mattada, Hansraj Guhilot

*Abstract***:** *Two stage 10-bit Time to Digital Converter is designed and verified in a commercial VLSI CAD tool. VCO driven counter is used in the first stage as coarse stage, whereas TDC based second stage is used for fine conversion. Each stage will give 5bit resolution and works concurrently during the conversion process. Delay-line/Flash TDC is used in the second stage because of its better conversion speed. Flash TDC will give thermometer code and a binary encoding scheme is required. To make it simple and area efficient, ROM based Thermometer to Binary(T2B) converters are used in the final readout module. Average power dissipation of 1.155mW for overall system is measured.*

*Index Terms***:** *Raman Spectroscopy, Delayed Chlorophyll Fluorescence, TDC, VCO, Delay Line TDC, Time gated Raman Spectroscopy*

I. INTRODUCTION

Time to Digital Converter is the key component in many applications viz. low voltage on-chip measurements, ADPLL, laser range finder, bio-chemical sensors, Raman Spectroscopy etc. Recent trends show that time-based ADCs are alternative data converters in low supply-voltage VLSI circuits. Non-stop scaling in VLSI is the main reason to go for mostly-digital low power data converters. Fig.1.shows our previous work[1] where TDC was used for measurement of delayed chlorophyll fluorescence. Fundamentals and different versions of Raman Spectroscopy are mentioned in[2]. The paper[2] clearly mentions the advantages and applications with respect to agriculture product and food analysis. Whether its Raman spectrometry or Fluorescence spectroscopy TDC is the most essential electronic component. Further differences between these two are elaborated in [3]. The difference in TDC design is only with respect to measurement range. Raman spectroscopy requires short range TDC and the latter requires long range. Present work will have reasonable resolution(116.7ps) and wide range (up to 1μs) to fit in both measurement setup. Time Measurement can be broadly classified as direct method or indirect method. Fig.2 shows detailed classification of TDC architectures. Direct method includes many modern techniques; viz. delay-line, Vernier delay-line, Vernier ring oscillator, Multipath gated ring oscillator, pulse shrinking technique etc. These architectures use reference clock or delay elements during conversion process. Indirect measurement includes time-to-voltage-digital conversion, i.e. converting time to voltage and further using an ADC to get its

digital equivalent. This mixed-signal TDC is called analog TDC or voltage-domain TDC

a)

b)
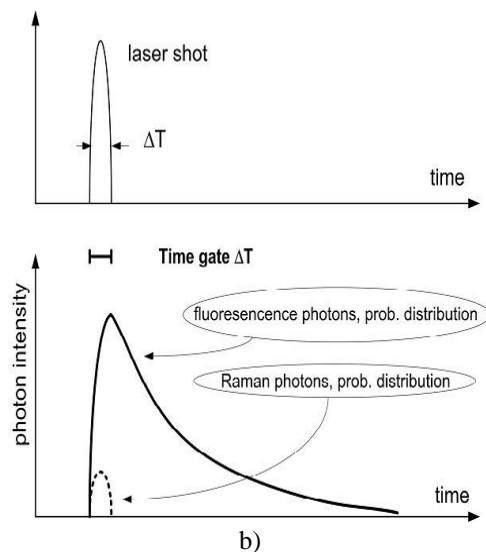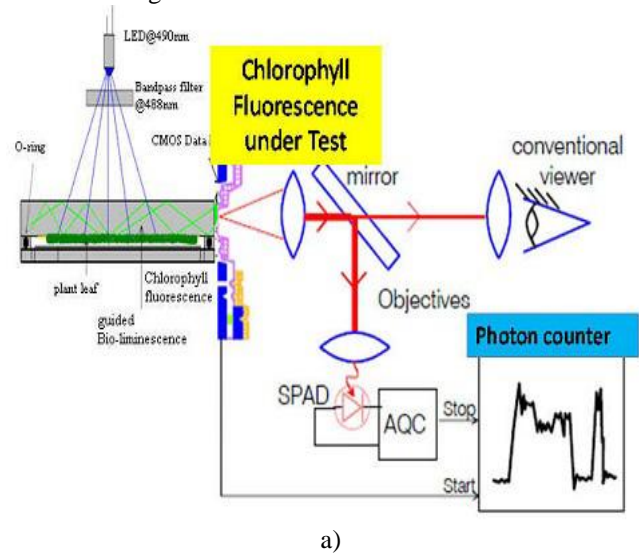
Fig.1 a) Delayed Chlorophyll Florescence Measurement Setup as illustrated in previous work [1] b) Principle diagram of time-gated Raman spectroscopy [4]

Modern designers trying hard to exclude ADC in their design. Few reasons for the same are explained here. Consider, a 10bit ADC with 2V reference which has to be scaled to 1V. Resolution or step size of the 2V reference ADC will be approximately 2mV, whereas 1V ADC will have step size of 1mV. This will pose difficulties in terms of
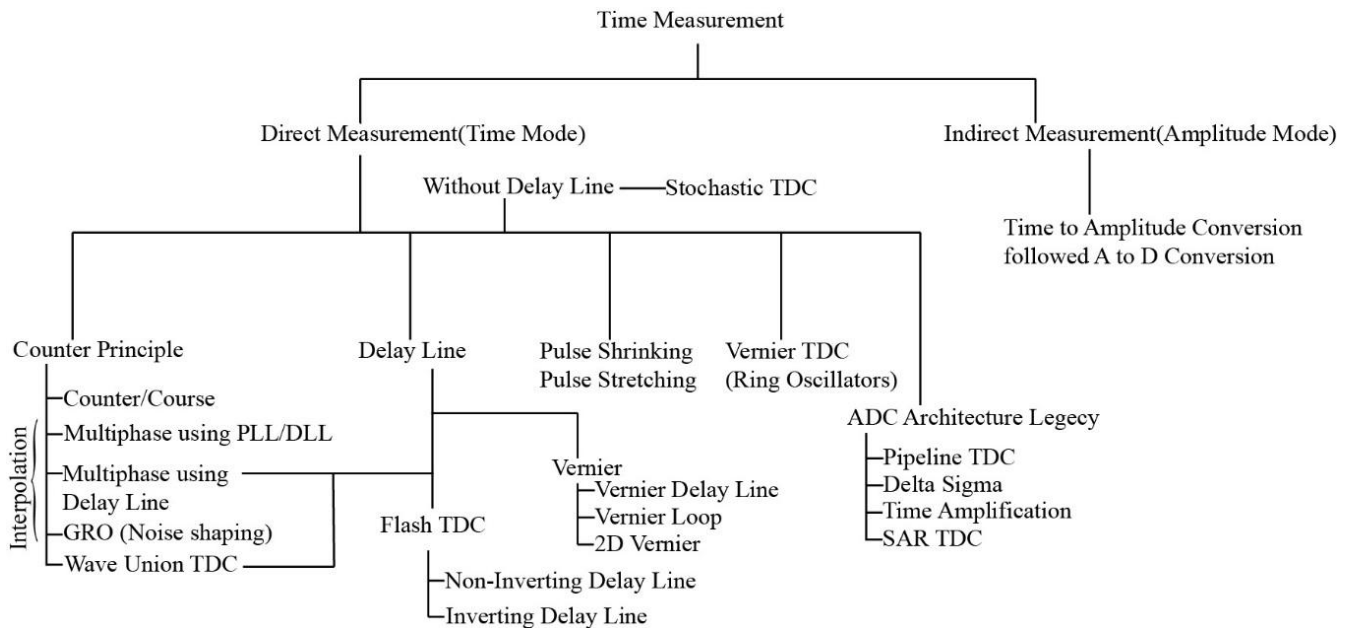
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Fig.2 Classification of Time to Digital Converters

non-linearities (INL and DNL). Hence ADC should be redesigned while scaling. Most on-chip ADCs will have higher reference voltage compared to chip operating voltage. Some designers provide separate pins for external reference voltages to suite this situation. Many modern VLSI systems try to avoid classical mixed-signal approach because of their bad scaling behavior. i.e. whether it is area scaling or voltage scaling, a whole redesigning of the system is required. On the other hand, TDC will measure *time* rather than voltage. So, irrespective of technology scaling, non-linearities will be under designer's control. Most of early architectures of TDCs are prototyped on FPGA because they are completely digital architectures. Fully digital circuits are most suitable for scaling. TDC is considered as future data converter because of above mentioned reasons. Reference [5] will give further understanding of TDC basics, principles and design issues.

The earlier work[6] used for Raman spectroscopy adopts indirect time measurement which is having 5-bit resolution. It is mostly-analog integrated circuit and no dynamic adjustment to enhance the range. Hence works only for fixed source wavelength. The technique is power hungry and suffers from wide deadtime. When it comes to present work, delay line TDC has been adopted. Delay-line TDC is also called as Flash TDC(FTDC). FTDC is well known for its simplicity and conversion speed. One of the drawback of delay-line TDC discussed in[6] is its exponentially increasing area-requirement as the number of bits increases. By incorporating course-fine stages one can overcome area overhead. i.e. course stage is to enhance the range and fine to improve the resolution. The proposed architecture is mostly digital and less power hungry and also suitable for scaling. An additional dynamic arrangement for its range without changing the measurement setup is an added advantage.

II. PROPOSED WORK

Fig.3 depicts proposed two stage TDC, where nutt interpolation method is incorporated. Whole circuitry is designed using TSMC 0.3μm technology and verified using *Spectre* simulator. Here, first stage will be coarse and second stage is the fine conversion. Equation 1 is mathematically expressing the *nutt* interpolation, where *n*Tclk* represents coarse conversion using a counter. This stage will greatly enhance the measurement range. Second stage conversion for *residue* measurement will enhance the resolution. Instead of VCO one can go for fixed crystal oscillator. This will not enable user to change the frequency dynamically. Rather, a control-input option given to change VCO frequency thereby adjustment of measurement range.

$$Tm = n*Tclk \pm T(residues) \qquad (1)$$

III. COARSE STAGE DESIGN AND RESULTS

Three stage current starved inverter chain is used as the VCO for the implementation. Fig.4 shows Current starved VCO with linearization scheme mentioned in[7] which is adapted for the present work. V_{inVCO} is the input which control the delay in each stage; thereby frequency of oscillations. Out of three stages only first stage is shown in the figure. Fig5.a shows the improvement in the linearity with the linearization setup. To choose appropriate value for resistor *R*, a parametric simulation has been carried out and presented in fig.5.b. This allowed us to choose *R* between 4kΩ to 5kΩ for better linearity. Also, eye diagram proves that, period jitter is well within 2.7ps.Also, within the mentioned control voltages, it is possible to double the measurement range. By keeping this option, we made the measurement setup open for different wavelengths and different laser shot widths.
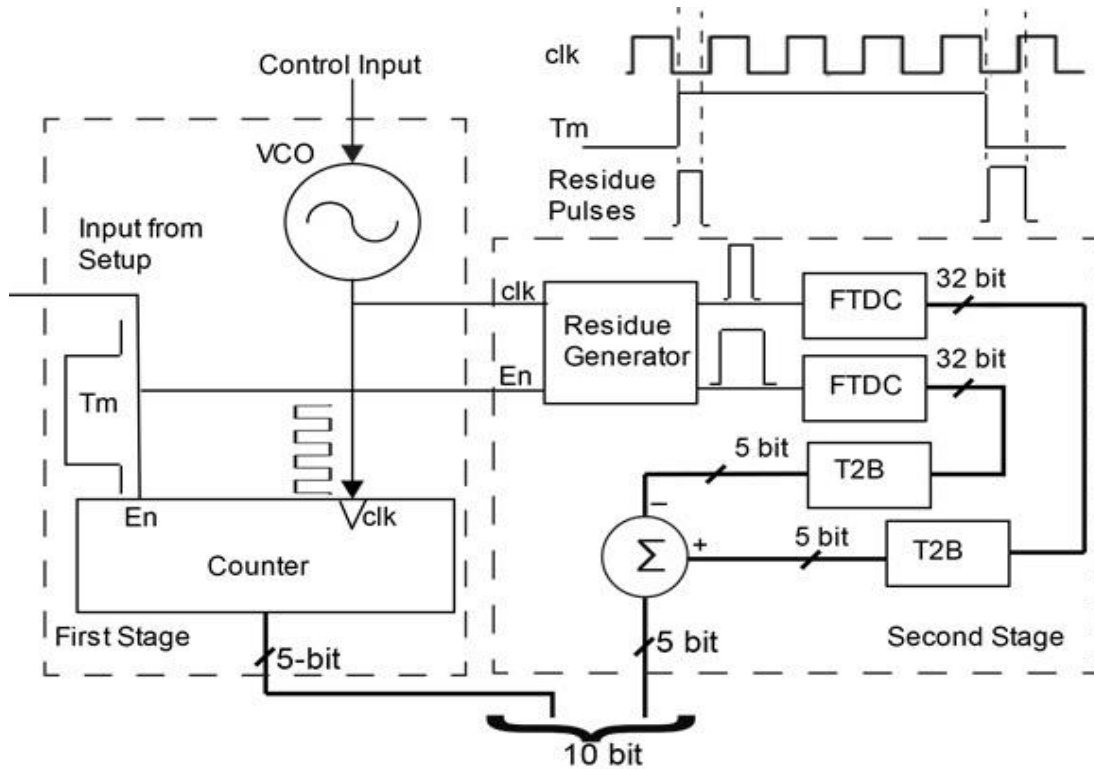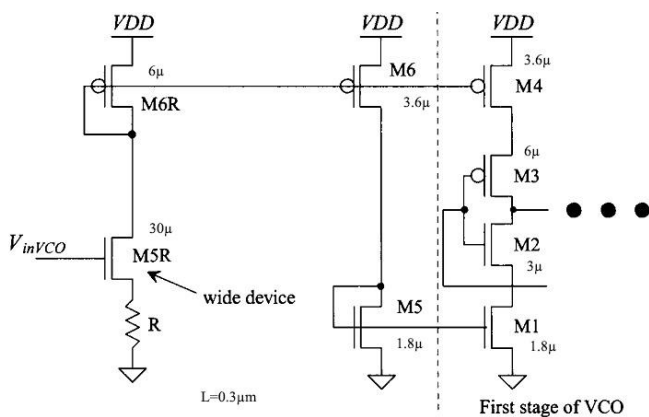
Fig.3 Proposed 2-stage 10-bit Time to Digital Converter

Fig.4 Current starved VCO with linearization scheme mentioned in [7]
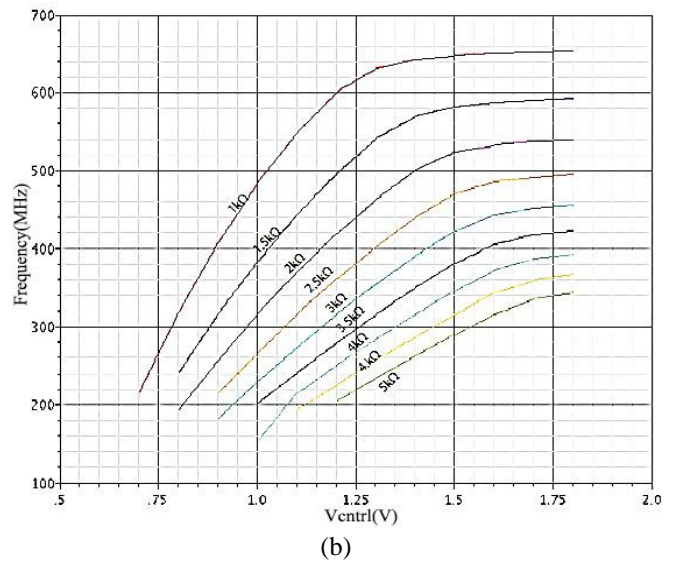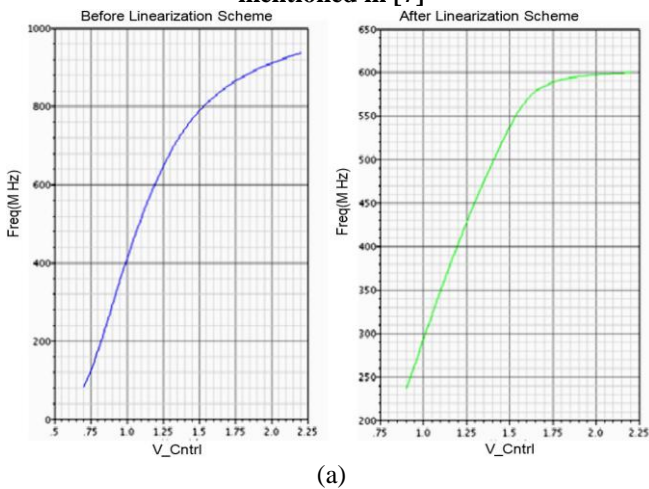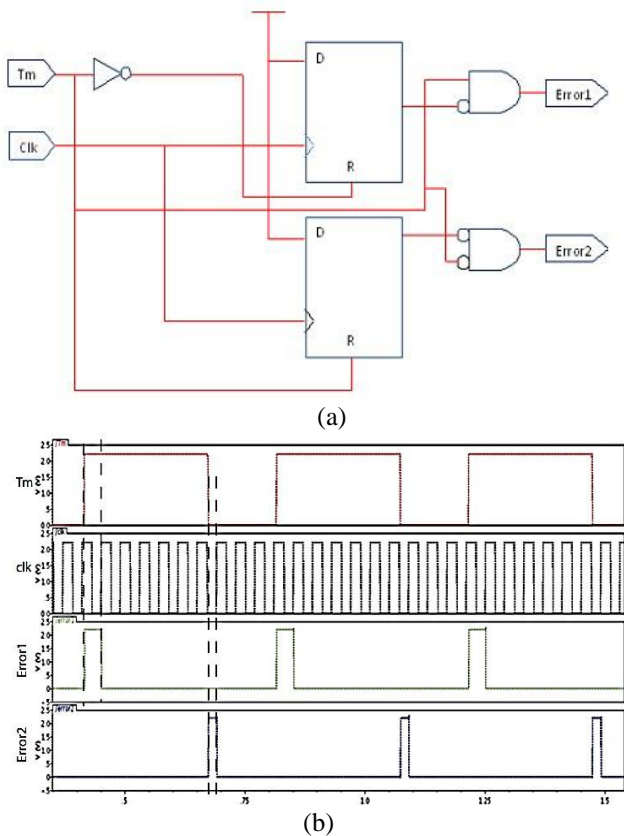

(a)

(b)

Fig.5 a) Linearity of VCO with and without linearity Scheme. b) Linearity of VCO frequency (MHz) with different values of R

IV. RESIDUE GENERATOR

To generate residue of the first stage a circuit shown in fig.6a has been adopted. Simulation results for the same is as presented in fig.6b. Equation 1 can be rewritten with respect to fig.6b as expressed in equation 2. The final calculation of equation 2 done at the front-end.
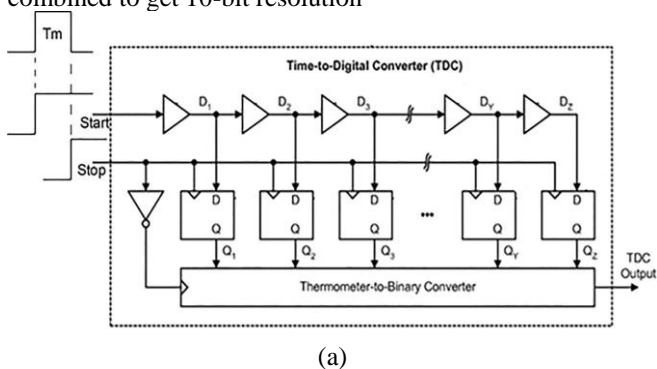
$$Tm = n * Tclk + Error1 - Error2 \qquad (2)$$

(a)

(b)

Fig.6 a) Residue generator schematic b) Simulation results of residue generator

(b)

(c)

Fig.7.a) General architecture of Flash Time to Digital Converter (FTDC)
b,c) Measured DNL and INL plots for 5bit FTDC

V. DELAY LINE TDC

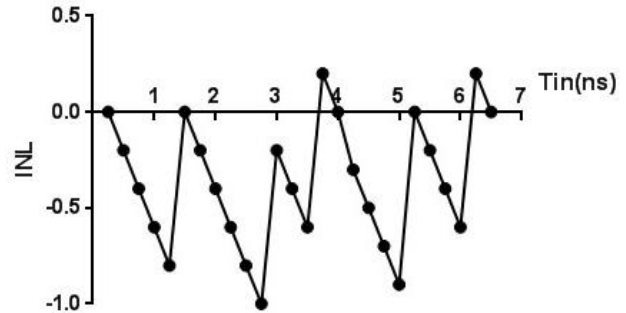Outputs of residue generator are then given to second stage for fine conversion. Fig7.a. shows Flash TDC also known as Delay Line TDC which is used to convert this tiny time residue to its digital equivalent. To decide the number of stages, it is necessary to identify maximum residue. Delay of delay-element (normally buffer) in the delay-line decides the resolution of the TDC. The resolution of the present TDC is 116 ps and it is suitable for the proposed measurement setup. From the calculation we conclude that, 32 delay stages should suffice for worst case. There are different techniques to improve the resolution depends on the application requirement. However, it's a trade-off between resolution and area. Measured DNL and INL plots presented in fig 7.b and both lie within 1 LSB. The TDC output will be thermometer code, hence thermometer to binary code conversion is required. The simplest method will be ROM based Thermometer-to-Binary(T2B) encoder and same is adopted for the present work. Such two FTDCs are used for two residue pulse measurement. Second stage result is then combined to get 10-bit resolution

(a)

VI. RESULTS AND DISCUSSION

Quantization error of the coarse stage is presented in fig 8.a. Further the improvement in the quantization error after fine stage is as depicted in fig.8.b. These measurements are obtained through precise simulations, hence reliable but time consuming. Transfer characteristics of the overall systems is as shown in fig. 9.a. The output is traced back using equation 2 and verified with input. DNL and INL plots of the overall system is as shown in fig. 9.b. DNL lie within 1 LSB, whereas maximum INL went up to -1.9 LSB. One important observation here is, its increase in its non-linearities. This is due to the inherent error introduced by Residue Generator

Power consumptions of different blocks have been depicted in fig.10. For each conversion, an average power consumption of 1.155mW has been recorded which includes static and dynamic power. However, major part of power is consumed by VCO i.e. 929µW, which is part of the course stage. Originally VCO included to replace crystal oscillator and make IC to generate its own clock. So, 5-bit FTDC power consumption is compared with 5-bit TDC from the reference. This comparison chart is also shown in fig.10, where 2 sets of 5-bit FTDCs consumes less power compared to one 5-bit TDC which uses indirect technique. Hence, Indirect measurement and mostly-analog ICs probably consume more power compared to direct and mostly-digital time measurement architectures. Power consumption of the present work can be further improved by implementing the architecture with recent VLSI technology.
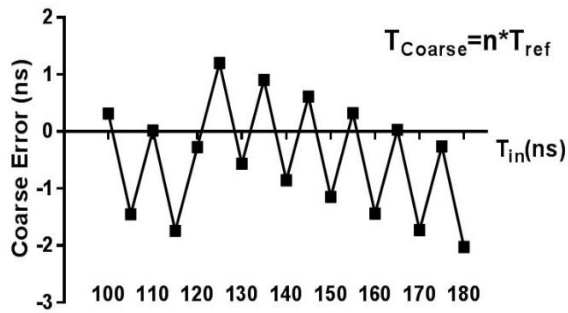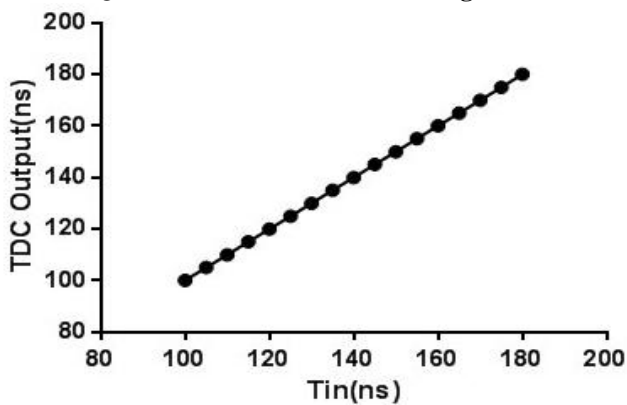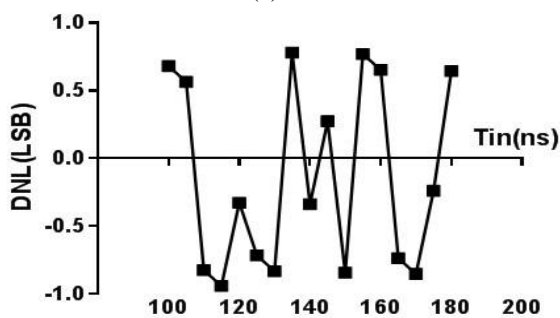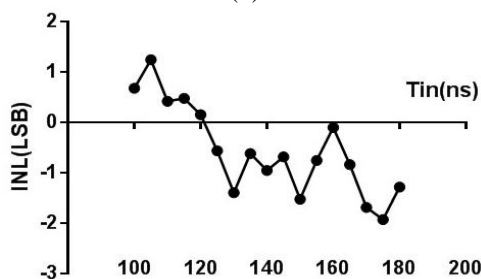
(a)

(b)

Fig.8.a) Quantization error of Coarse stage b) Quantization error at second stage

(a)

(b)

(c)

Fig.9.a) Transfer Characteristics of overall system b,c) Measured DNL and INL plots
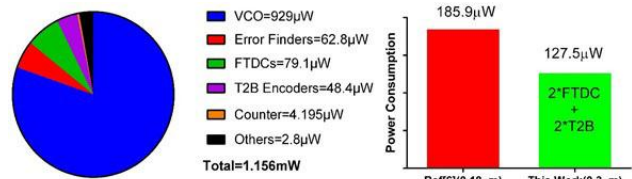

Fig.10 Power consumption chart and comparison

VII. CONCLUSION

Time to Digital Converter architectures are promising techniques for most of the future data converters problems. The current architecture proves simple yet effective way of implementing mostly-digital, area and power efficient system. The proposed work has been designed and verified using a commercial CAD tool with TSMC 0.3µm technology. This work exhibits better resolution and measurement range. Thus, the same architecture can be used for both Raman and delayed fluorescence spectroscopy. The measurement range can be further enhanced by using looped delay line structure. Power consumption chart shows that, present architecture consumes only1.156mW.

REFERENCES

1. Mattad MP, Guhilot H, Kamat RK. "Area efficient time to digital converter (TDC) architecture with double ring-oscillator technique on FPGA for fluorescence measurement application" *IEEE Recent Advances in Intelligent Computational Systems RAICS,* Trivendrum, India; 2011. p.260–263.
2. Yang D, Ying Y. "Applications of raman spectroscopy in agricultural products and food analysis: A review" *Appl Spectrosc* Rev 2011;46:539–60.
3. Li Z, Deen MJ, Kumar S, Selvaganapathy PR. "Raman spectroscopy for in-line water quality monitoring — Instrumentation and potential". *Sensors (Switzerland)* 2014;14:17275–303.
4. Kostamovaara J, Tenhunen J, Kögler M, Nissinen I, Nissinen J, Keränen P. "Fluorescence suppression in Raman spectroscopy using a time-gated CMOS SPAD" *Opt Express* 2013;21:31632-45.
5. Henzler S. *Time-to-Digital Converters.* Springer; 2010.
6. Rezvanyvardom M, Nejad TG, Farshidi E. "A 5-bit time to digital converter using time to voltage conversion and integrating techniques for agricultural products analysis by Raman spectroscopy" *Inf Process Agric* 2014;1:124–30.
7. Baker RJ. *CMOS Circuit Design, Layout, and Simulation*. Wiley; 2010. p.561-5

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Mahantesh P. Mattada was born in Harihar, India in 1986. He received B.E degree in Electronics and Communication, M.Tech degree in VLSI Design and Embedded Systems from VTU, Belagavi, in 2008 and 2011, respectively. He is pursuing PhD at VTU Belagavi.Earlier he was with Department of E&TC, Sanjay Ghodawat Institutes, Kolhapur. Currently associated with the Department of Electronics and Communication, Sanjay Ghodawat University, Kolhapur, India. Presently he is working on design, testing and applications of various Time to Digital Converter architectures. His area of interest includes CMOS VLSI Design and Digital Design using FPGA.

10-bit 2-stage Time to Digital Converter for Raman Spectroscopy

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